that is much larger than I_b (to eliminate effects of β variation). V_b should be much larger than ΔV to reduce the effects of variations in ΔV.

Three additional biasing schemes are presented in **Fig 6.50**. All provide bias that is stable regardless of device parameter variations. A and B require a negative power supply. The circuit of Fig 6.50C uses a second, PNP, transistor for bias control. The PNP transistor may be replaced with an op amp if desired. All three circuits have the transistor emitter grounded directly. This is often of great importance in microwave amplifiers. These circuits may be analyzed using the simple model of Fig 6.49.

The biasing equations presented may be solved for the resistors in terms of desired operating conditions and device parameters. It is generally sufficient, however, to repetitively analyze the circuit, using standard resistor values.

The small-signal transconductance of a common-emitter amplifier was found in the previous section. If biased for constant current, the small-signal voltage gain will vary inversely with temperature. Gain may be stabilized against temperature variations with a biasing scheme that causes the bias current to vary in *proportion to absolute temperature*. Such methods, termed PTAT methods, are often used in modern integrated circuits and are finding increased application in circuits built from discrete components.

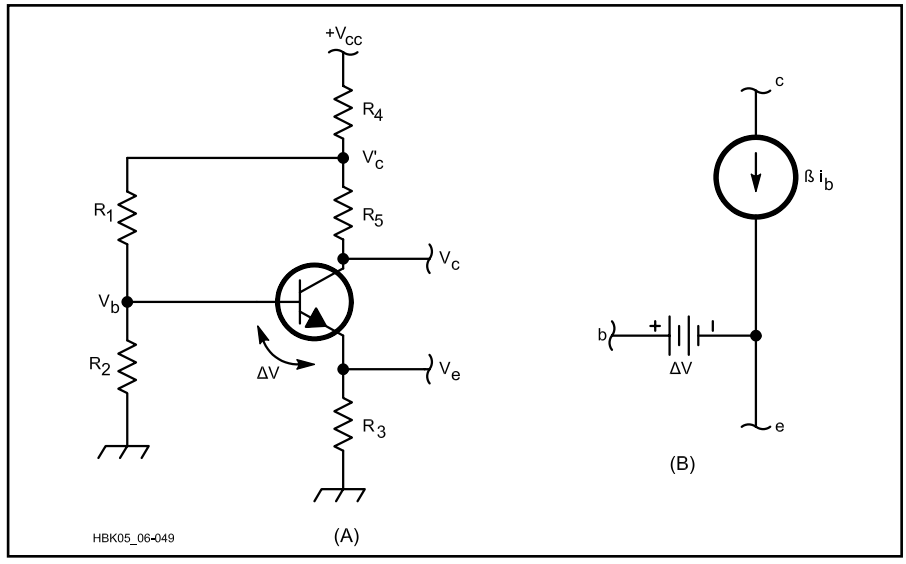

Fig 6.49—(A) Circuit used for evaluation of transistor biasing. (B) The model used for bias calculations.

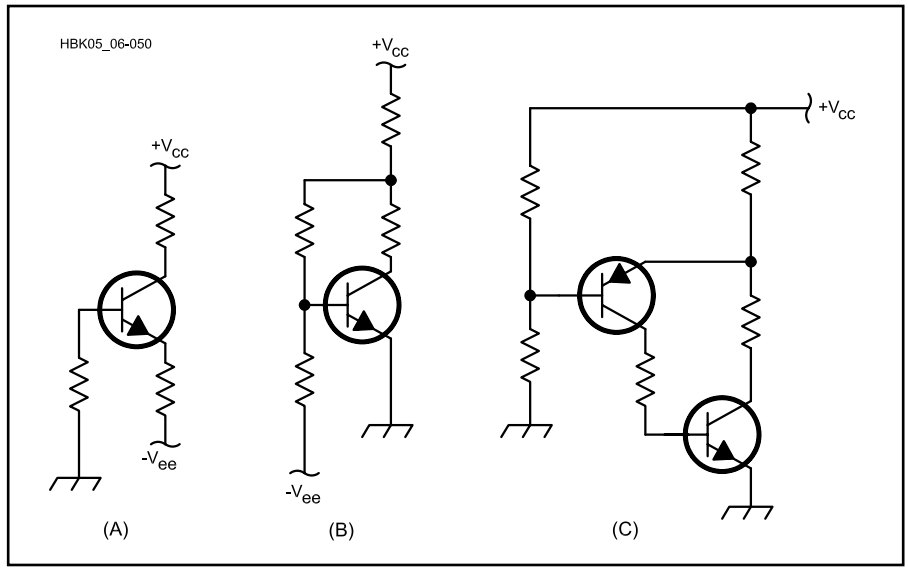

Fig 6.50—Alternative biasing methods. (A) and (B) use dual power supplies, (B) and (C) allow the emitter to be at ground while still providing temperature-stable operation.

Large-Signal Operation

The models presented in previous sections have dealt with small signals applied to a bipolar transistor. While small-signal design is exceedingly powerful, it is not sufficient for many designs. Large signals must also be processed with transistors. Two significant questions must be considered with regard to transistor modeling. First, what is a reasonable limit to accurate application of small-signal methods? Second, what are the consequences of exceeding these limits?

The same analysis of the Ebers-Moll model yields an equation for collector current. The mathematics show that current will vary in a complicated way, for the sinusoidal signal voltage is embedded within an exponential function. Nonetheless, the output is a sinusoidal current if the signal voltage is sufficiently low.

The current of the equation may be studied by normalizing the current to its peak value. The result is relative current, I_r, which is plotted in **Fig 6.51** for V_p values of 1, 10, 30, 100, and 300 mV. The 1-mV case is very sinusoidal. Similarly, the 10-mV curve is generally sinusoidal with only minor distortions. The higher amplitude cases show increasing distortion.

Constant base-voltage biasing is unusual. More often, a transistor is biased to produce nearly constant emitter current. When such an amplifier is driven by a large input signal, the average bias voltage will adjust itself until the time average of the nonlinear current equals the previous constant bias current. Hence, it is vital to consider the average relative current of the waveforms of Fig 6.51. This is evaluated through calculus.

The average relative currents for the cases analyzed occur at the intersection of the curves with the dotted lines of Fig 6.51.

Ready-Made Models

Many manufacturers provide computer models, S-parameter files or other data helpful when including their devices in circuits modeled with *SPICE* and other computer tools. These files are often available from component manufacturers' Web sites, from software providers, or from third parties. Because this information changes, use your favorite Internet search tool to look for information on components of interest.

For example, the dotted curve intersects the V_p = 300-mV waveform at an average relative current of 0.12. If an amplifier was biased to a constant current of 1 mA, but was driven with a 300-mV signal, the positive peak current would reach a value greater than the average by a factor of 1/(0.12). The average current would remain at 1 mA, but the positive peak would be 8 mA. The transistor would not conduct for most of the cycle.

The curves have presented data based upon the simplest of large-signal models, the Ebers-Moll equation. Still, the simple model has yielded considerable information. The analysis suggests that a reasonable upper limit for accurate small-signal analysis is a peak base signal of about 10 mV. The effect of emitter degeneration is also evident. Assume a transistor is biased for r_e = 5 Ω and an external emitter resistor of 10 Ω is used. Only the r_e portion of the 15 Ω total is nonlinear. Hence, this amplifier would tolerate a 30-mV signal while still being well described with a small-signal analysis.

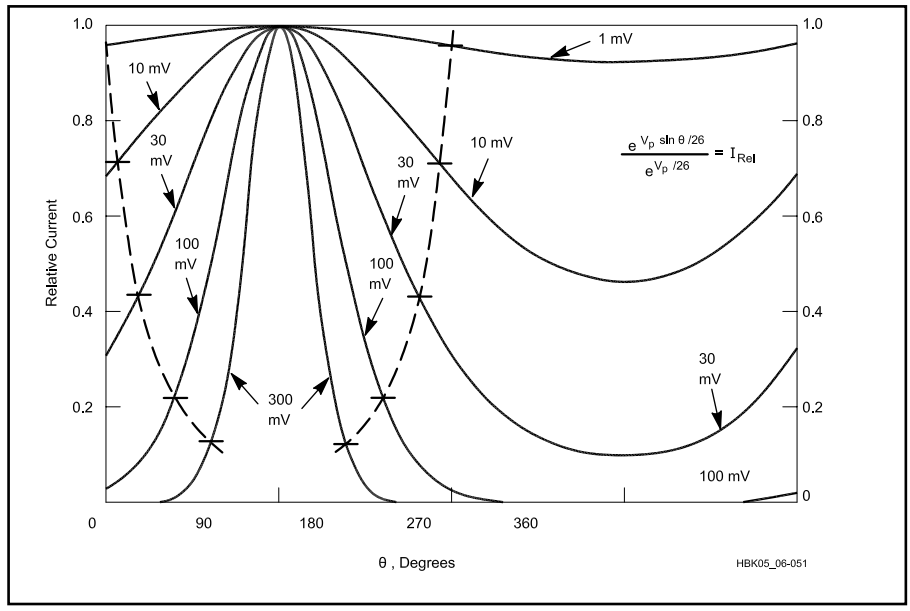

Fig 6.51—Normalized relative current of bipolar transistor under sinusoidal drive at the base.

FETS

An often used device in RF applications is the field-effect transistor (FET). There are many kinds: JFETs, MOSFETs and so on. Here we will discuss JFETs, with the understanding that other FETs are similar.

We viewed the bipolar transistor as controlled by either voltage or current. The JFET, however, is purely a voltage controlled element, at least at low frequencies. The input gate is usually a reverse biased diode junction with virtually no current flow. The drain current is related to the source-gate voltage by:

$$I_D = I_{DSS}\left(1 - \frac{V_{sg}}{V_p}\right)^2 \qquad 0 \le V_{sg} \le V_p$$
$$I_D = 0 \qquad V_{sg} > V_p \qquad (26)$$

where I_{DSS} is the drain saturation current and V_p is the pinch-off voltage. Operation is not defined when V_{sg} is less than zero because the gate diode is then forward biased. Equation 26 is a reasonable approximation as long as the drain bias voltage exceeds the magnitude of the pinch-off voltage.

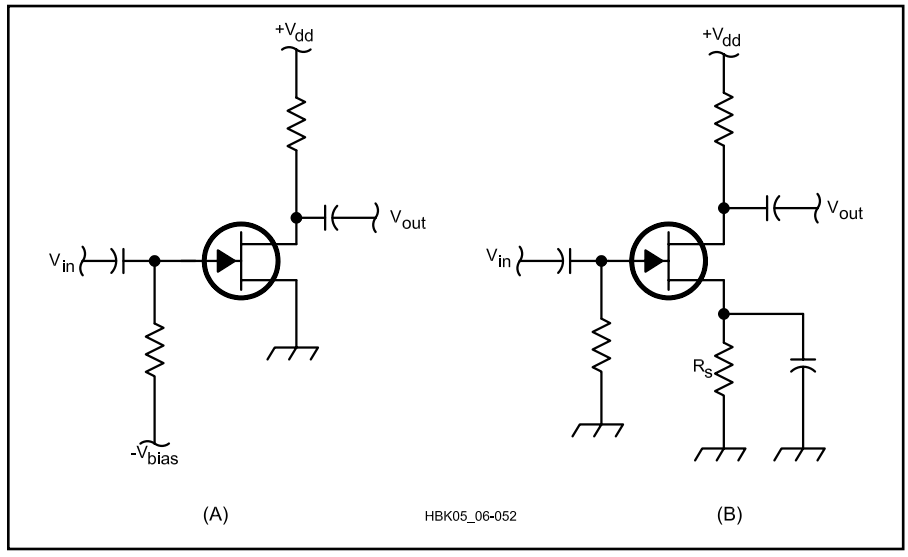

Fig 6.52—Biasing schemes for a common-source JFET amplifier. $-V_{bias}$ is normally adjusted to suit each device; there is a significant spread over a product run. Also note that some FETs can exhibit thermal runaway in some current/temperature ranges.

Biasing FETs

Two virtually identical amplifiers using N-channel JFETs are shown in **Fig 6.52**. The two circuits illustrate the two popular methods for biasing the JFET. Fixed gate-voltage bias, Fig 6.52A, is feasible for JFETs because of their favorable temperature characteristics. As the temperature of the usual FET increases, current decreases, avoiding the thermal-runaway problem of bipolar transistors.

A known source resistor, R_s in Fig 6.52B, will lead to a known source voltage. This is obtained from a solution of equation 26 (see **Eq 27**).

The drain current is then obtained by direct substitution.

$$V_{sg} = \frac{\left[\frac{1}{R_s I_{DSS}} + \frac{2}{V_p}\right] - \left[\left(\frac{1}{R_s I_{DSS}} + \frac{2}{V_p}\right)^2 - \left(\frac{2}{V_p}\right)^2\right]^{0.5}}{\frac{2}{V_p^2}} \qquad (27)$$

Alternatively, a desired drain current less than I_{DSS} may be achieved with a proper choice of source resistor

$$R_s = \frac{V_p\left(1 - \frac{I_D}{I_{DSS}}\right)^{0.5}}{I_D} \qquad (28)$$

The small-signal transconductance of the JFET is obtained by differentiating equation 26

$$g_m = \frac{dI_D}{dV_{sg}} = \frac{-2\,I_{DSS}}{V_p}\left(1 - \frac{V_{sg}}{V_p}\right) \qquad (29)$$

The minus sign indicates that the equation describes a common-gate configuration. The amplifiers of Fig 6.52 are both common-source types and are described by equation 29 except that g_m is now positive. Small-signal models for the JFET are shown in **Fig 6.53**. The simple model is that inferred from the equations while the model of Fig 6.53B contains capacitive elements that are effective in describing high-frequency behavior. Like the bipolar transistor, the JFET model will grow in complexity as more sophisticated applications are encountered.

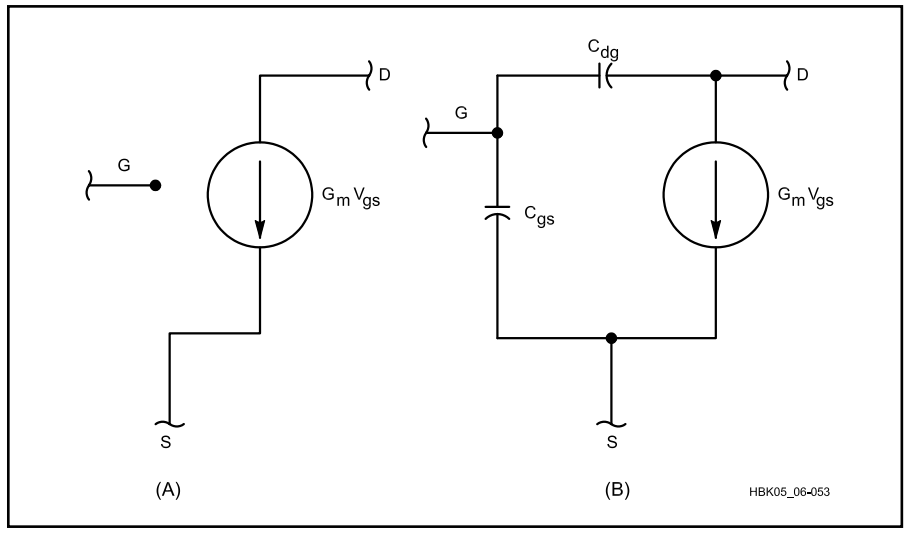

Fig 6.53—Small-signal models for the JFET. (A) is useful at low frequency, (B) is a modification to approximate high-frequency behavior.

Large-Signal Operation

Large-signal JFET operation is examined by normalizing the previous equation to $V_p = 1$ and $I_{DSS} = 1$ and injecting a sinusoidal signal. The circuit is shown in **Fig 6.54**. Also shown in the figure are examples for a variety of bias and sinusoid amplitude conditions. The main feature is the asymmetry of the curves. The positive portions of the oscillations are farther from the mean than are the negative excursions. This is especially dramatic when the bias, v_0, is large, which places the quiescent point close to pinch-off. With such bias and high-amplitude drive, conduction occurs only over a small fraction of the total input waveform period.

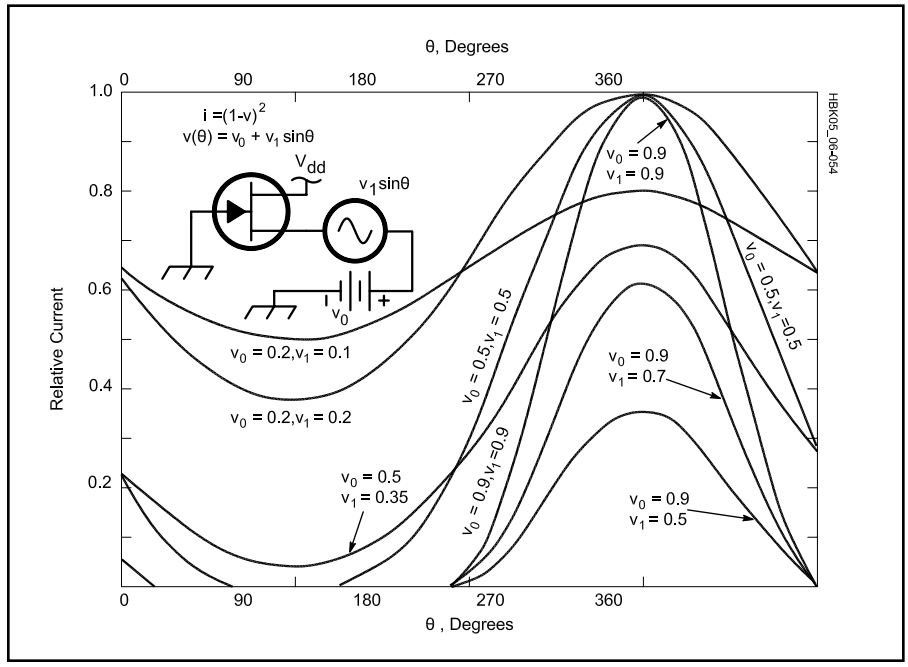

Fig 6.54—Relative normalized drain current for a JFET with constant voltage bias and sinusoidal signals. Relatively "clean" waveforms exist for low signals while large input amplitudes cause severe distortion.

The average current for these operating conditions can be determined by calculus. The average current values obtained may be further normalized by dividing by the corresponding dc bias current, $I_0 = (1 - v_0)^2$. The results are shown in **Fig 6.55**. The curves show that the average current increases as the amplitude of the drive increases. This, again, is most pronounced when the FET is biased close to pinch-off.

Although practical for the JFET, constant-voltage operation in the previous curves is not common. Instead, a resistive bias is usually employed, Fig 6.52B. With this form of bias, the increased current from high signal drive will cause the voltage drop across the bias resistor to increase. This will then move the quiescent operating level

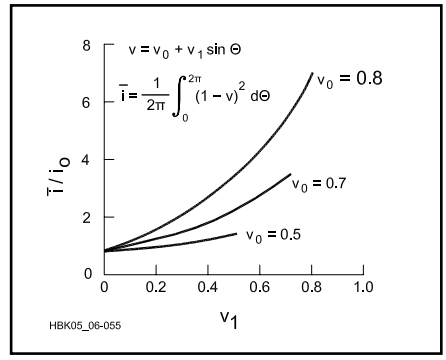

Fig 6.55—Change in average current of a JFET with increasing input signals. The average current with no input signals is I_0, while v_1 is the normalized drive amplitude, and v_0 is the bias voltage.

closer to pinch-off, accompanied by a reduced small-signal trans-conductance. This behavior is vital in describing the limiting found in FET oscillators.

The limits on small-signal operation are not as well defined for a FET as they were for the bipolar transistor. Generally, a maximum voltage of 50 to 100 mV is allowed at the input (normalized to a 1-V pinch-off) without severe distortion. The voltages are much higher than they were for the bipolar transistor. However, the input resistance of the usual common source amplifier is so high and the corresponding transconductance low enough that the available gain is no greater than could be obtained with a bipolar transistor. The distortion is generally less with FETs, owing to the lack of high-order curvature in the defining equations.

Many of the standard circuits used with bipolar transistors are also practical with FETs. Noting that the transconductance of a bipolar transistor is $g_m = I_e$ (dc mA) / 26, the previous equations may be applied directly. The "emitter current" is chosen to correspond with the FET transconductance. A very large value is used for current gain. The same calculator or computer program is then used directly. In practice, much higher terminating impedances are needed to obtain transducer gain values similar to those of bipolar transistors.

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Suggested Additional Reading

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Notes

[1]Superconducting circuits are the one exception; but they are outside the scope of this book.

[2]There are numerous manufacturers of excellent heat sinks. References to any one manufacturer are not intended to exclude the products of any others, nor to indicate any particular predisposition to one manufacturer. The catalogs and products referred to here are from: Wakefield Thermal Solutions, Inc., 33 Bridge Street, Pelham, NH 03076, Phone: (603) 635-2800.