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Transmission Lines in Digital Circuits

The performance of digital logic families covers a wide range of signal transition times. The signal rise and fall times are most important when considering how to construct a circuit. The operating frequency of a circuit is not the primary consideration. A circuit that uses high-speed logic yet runs only at a few kHz can be difficult to tame if long point-to-point wiring is used.

If the path between two points has a delay of more than 1/6 the logic family rise time, some form of transmission line should be considered. We know that waves propagate at 300 million meters per second in air and at 0.66 times as fast in common coax cable. So, in about 5 ns a wave will travel 1 meter or in 1 ns it will travel 0.2 m.

Consider a logic family which has 2 ns rise and fall time. Using the rule mentioned above, if the path length exceeds 0.066 meter or about 2.6 inches we need to use a transmission line. Another way to look at it is the approximate equivalent analog bandwidth is:

$$\text{BW} = \frac{0.35}{\text{rise time}} = \frac{0.35}{2\,\text{ns}} = 175\,\text{MHz}$$

If we were building an analog circuit that operated at 175 MHz, we would have to keep the wire lengths down to a fraction of an inch. So, even if our logic's clock is running at a few kHz, we still need to use these short wire lengths. But, suppose we are building a non-trivial circuit that has a number of gates and other digital blocks to interconnect. In order to reach several ICs from the clock's source, we will need to run wires over several inches in length.

It is possible to build a high speed circuit in breadboard style if small coax cable is used for interconnections. However, if a PC board is designed with *microstrip* transmission line interconnections, success is more likely. **Figure 1** shows the way microstrip transmission line is made. Typical dimensions are shown for 1/16-inch thick FR4 material and 50-Ω line.

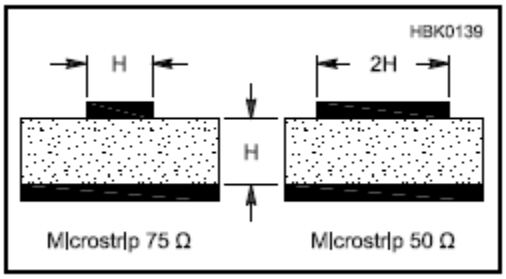

Figure 1 — Microstrip transmission lines. The approximate geometries to produce 75 Ω (A) and 50 Ω (B) microstrip lines with FR-4 PC board material are shown. This technique is used at UHF and microwave frequencies.

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There are several ways that the actual circuit can be configured to assure that the desired signal reaches the receiving device input. To avoid multiple reflections that would distort the signals and possibly cause false triggering, the line should either be matched at the load end or the source end. We know that matching at the load end will completely absorb the signal so that there are no reflections. However, the signal level will be reduced because of voltage division with the source impedance in the sending gate. The dc levels will also shift because of the load, reducing the logic noise immunity. A considerable amount of power can be dissipated in the load, which might overload the source gate particularly if 50-Ω line is in use. It is possible to put a capacitor in series with the load resistor, but only if the waveform duty cycle is near 50%. If not, the dc average voltage will reduce the noise immunity of the receiving gate.

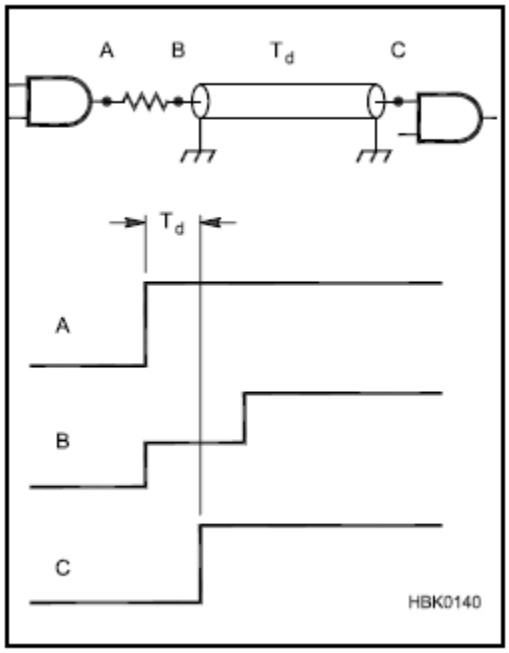

Figure 2 — Reflections in a transmission line cause stepping in the leading edge of a digital pulse at the generator (A). By adding a resistor in series with the gate output, a step is generated at the input to the transmission line (B), but a full-voltage step is created at the high input impedance of the receiving gate.

A better method is to match the transmission line at the signal source as in **Figure 2**. A resistor is added in series with the output of the sending gate, raising the gate output impedance to match Z_0 of the transmission line, which is connected to the resistor at B and has an arbitrary length T_D. No load is required on the receiving end of the transmission line, which is assumed to be connected to a gate with an input impedance much higher than Z_0.

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When the sending output goes high at point A, generating the leading edge of a pulse with voltage V, the load on the output resistor is equal to the Z_0 of the transmission line so a voltage divider is formed and the voltage at point B initially goes to 1/2 V. The pulse travels down the transmission line and after T_D it completely reflects off the open end at the receiving gate. The voltage at C reaches V since the direct signal and the reflected signal add together. When the reflected edge of the pulse returns to point B after a round trip time of $2T_D$, the voltage level at B increases to V.

The receiving end can be terminated in Z_0 if a pair of resistors, each equal to $2 \times Z_0$, are connected from the positive power supply to ground at point C. The transmission line and gate input are connected to the resistor junction. The main problem with this method is the steady-state current required by the resistors. Some logic gates may not have adequate current output to drive this load.