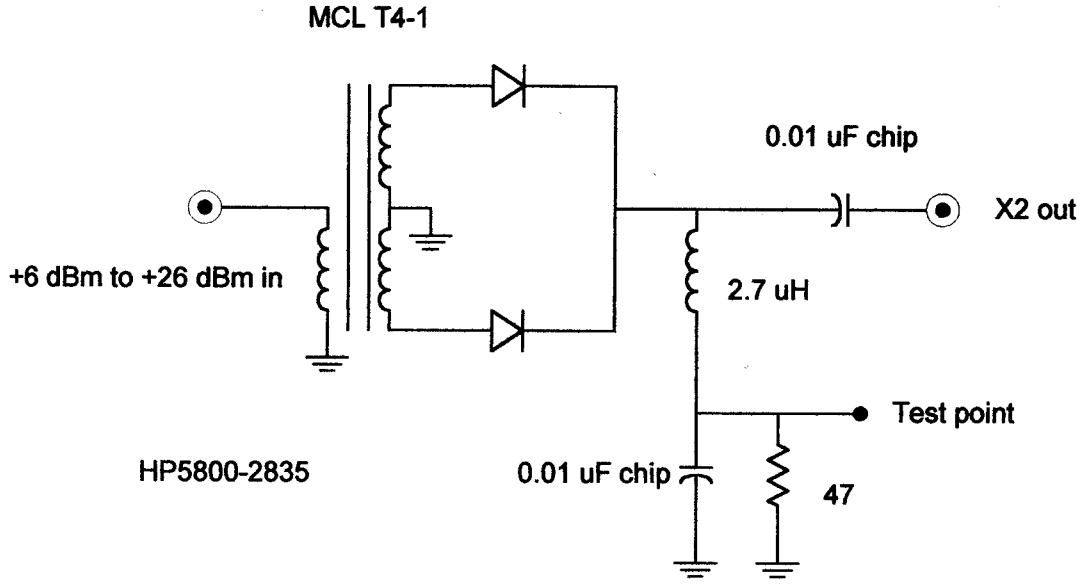
Medium Power Diode Frequency Doublers

Rick Campbell 5/20/99

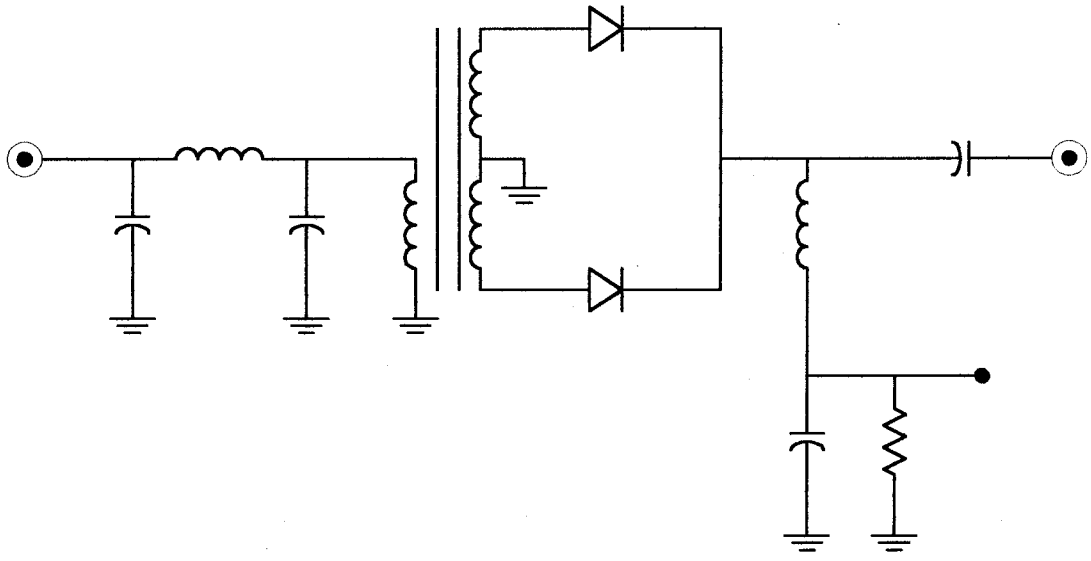
Two types of frequency doublers were simulated in PSPICE, built, and measured in the lab. The first is a traditional full-wave rectifier using a Mini-Circuits T4-1 transformer, but includes a bias circuit consisting of a bypassed DC load. The load permits the drive level to be much higher than would be permitted with the diodes short-circuited to ground, which allows the doublers to be used to obtain very respectable output power (more than 13 dBm) at reasonable conversion efficiency. Loss is approximately 10 dB. The second type of frequency doubler replaces the T4-1 transformer with a half-wave balun of the type often used with folded dipole antennas. This permits the frequency doubler to be constructed for much higher frequencies, limited only by the diode and chip component parasitics. Diode doublers with similar performance have been built and measured for output frequencies as high as 10 GHz.

The first doubler is built using the basic topology shown in figure 1. With the values shown, this circuit works well with input frequencies from 2 MHz to 400 MHz. Optimum performance is between 10 MHz and 100 MHz input, but loss increases only by about a dB at the 2 MHz and 400 MHz points.

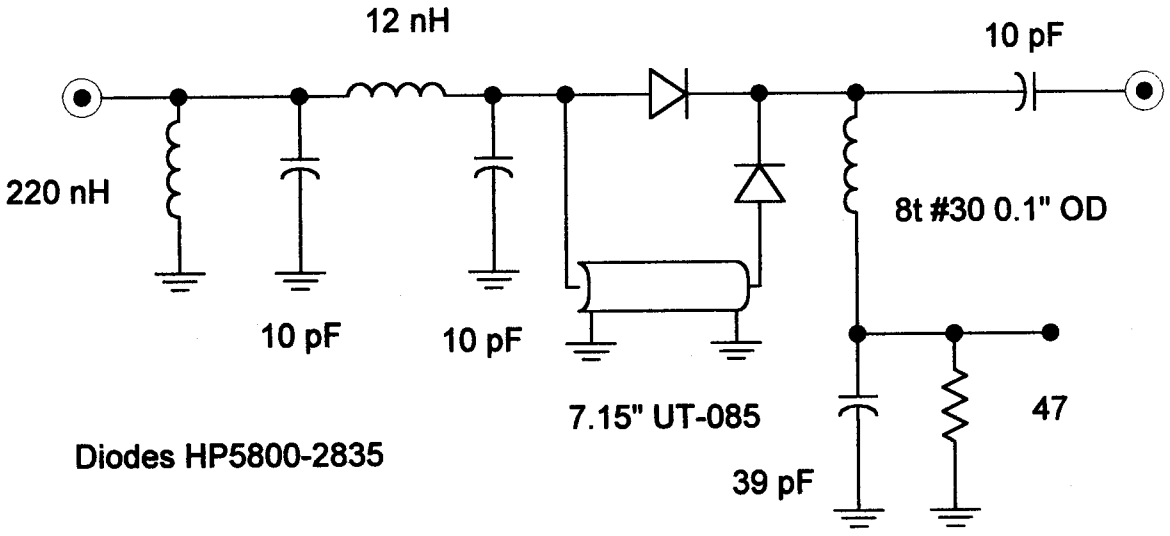


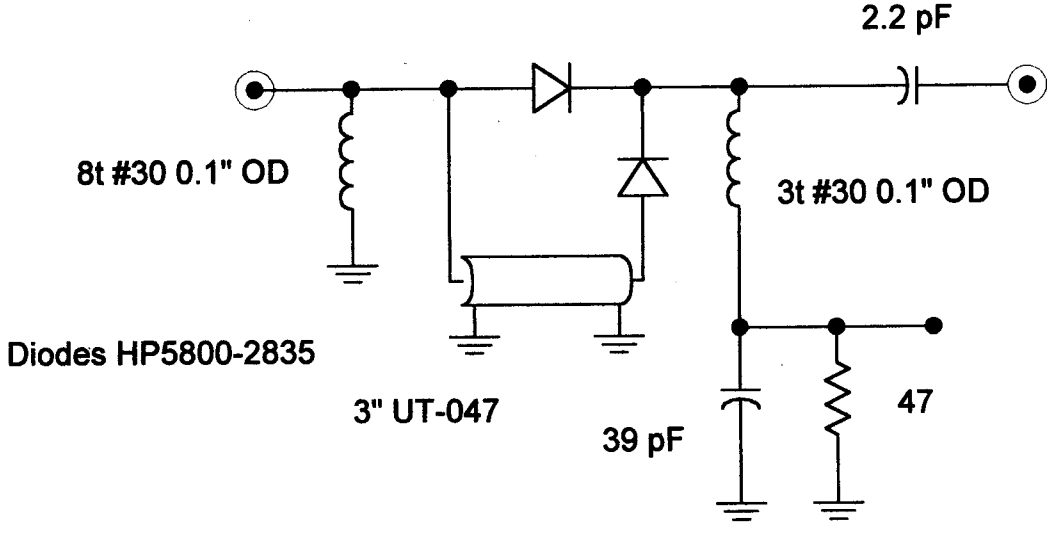
A more general form of doubler is shown in figure 2, which includes a low-pass filter on the input. Balanced doublers require sine wave drive. The presence of even small amounts of even or odd harmonics will dramatically reduce the desired output and increase the undesired outputs. Square wave drive to the circuit in figure 1 (no odd harmonics, 3rd harmonic 9.5 dB down, 5th harmonic 14 dB down, 7th harmonic 17 dB

down etc.) will result in no RF output at all! For best performance, drive to a balanced doubler should have all harmonics 40 dB down or more.

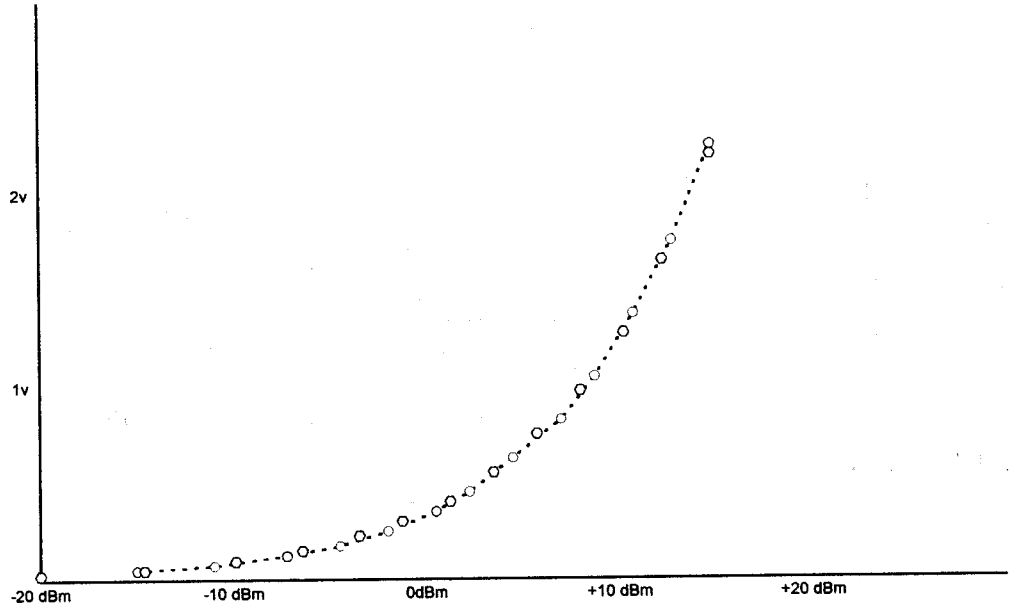


The second type of doubler is illustrated in figures 3 and 4. Use of a half-wave transmission line makes this topology a narrow-band structure. The "narrow bandedness" applies to suppression of the drive frequency and odd harmonics. There is a narrow null in input frequency suppression at the design frequency. The desired output level does not change much as the input frequency goes through the null. Examining the schematic, it is clear that the circuit degenerates to two diodes in parallel at low frequency, so the circuit still doubles, but the drive frequency is no longer suppressed. The upper circuit is optimized for doubling from 576 MHz to 1152 MHz, and the figure 4 circuit is optimized for doubling from 1152 MHz to 2304 MHz. Both circuits have about 10 dB conversion loss, and can provide more than +13 dBm output when driven by 200 mW.





Not only does addition of the bias resistor permit optimizing the doubler for much higher drive levels, the bias circuit provides a built-in test point that provides a calibrated output reading. Two different doublers, one using a T4:1 transformer and the other using a half-wave UT-085 balun were measured, using a 47 ohm bias resistor. The voltage across the bias resistor versus the second harmonic (desired) output level are shown in the figure 5 plot below.

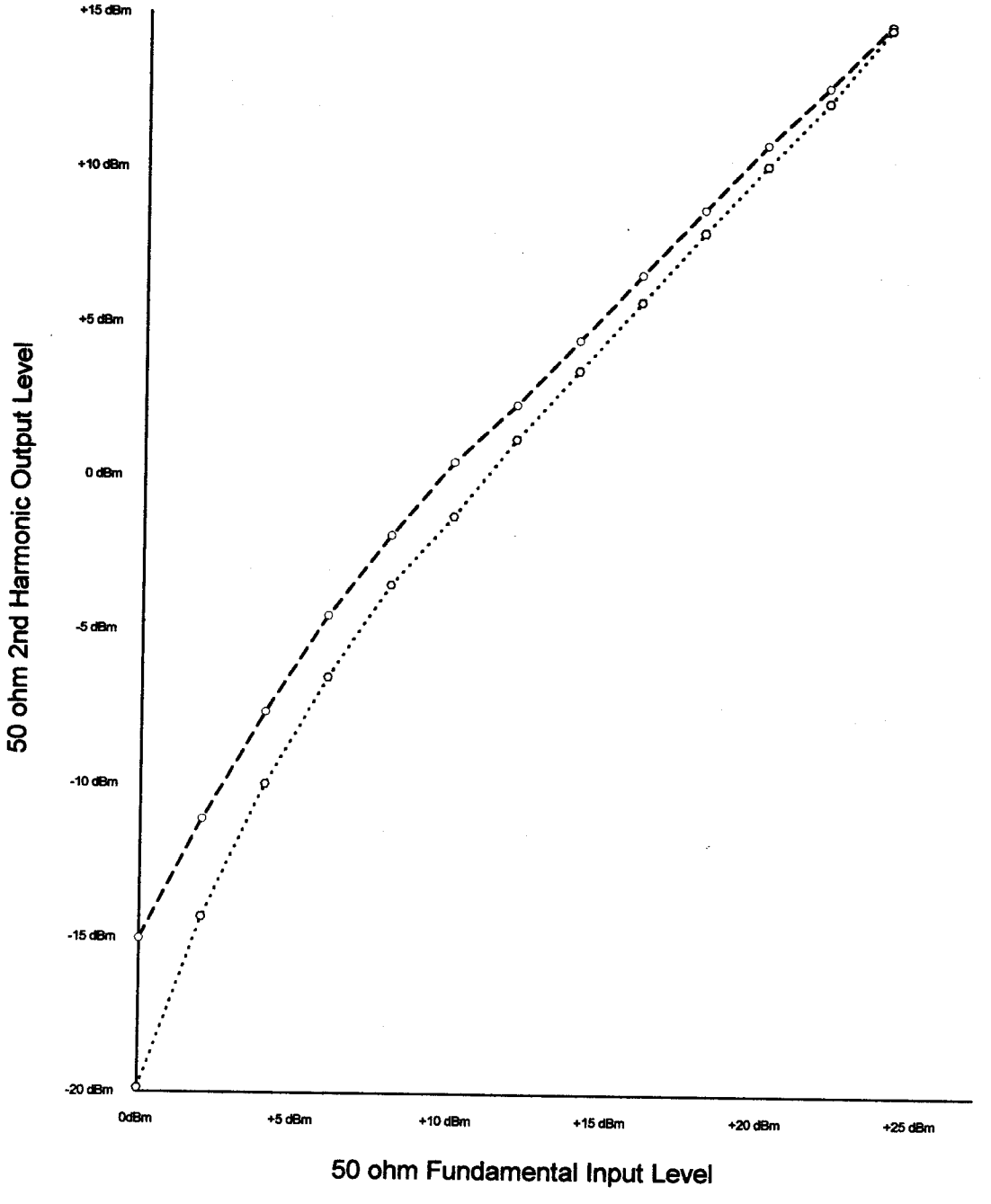


The open circles are from the T4-1 transformer doubler and the filled circles are from the UT-085 balun doubler. Clearly the DC voltage across the 47 ohm bias resistor provides a useful measurement of output power. There is a relationship between bias voltage and frequency doubler output power, which can be used as a power indicator, but this voltage will likely change when the doubler drives something other than a perfect 50 ohm RF load.

Power output versus power input is quite linear over the drive level range from about +7 dBm to +25 dBm, as shown in the plot in Figure 6. The open circles are the T4-1 version driven at 144 MHz and the filled circles are from the 576 MHz to 1152 MHz half-wave line version. This type of frequency doubler is very different from other frequency multipliers in its linear input to output curve. For example, the odd-harmonic multiplier using a CMOS logic chip provides the same harmonic output level over a very wide range of input levels, once the drive level is high enough to toggle the logic. Class C multipliers using bipolar transistors or FETs generally display a very non-linear output level versus input level curve, and in fact the drive level is varied to optimize a particular harmonic. Frequency multipliers that use the non-linear semiconductor properties of diodes must be optimized for a particular drive level, and output power typically falls off rapidly both above and below the optimum drive level.

This suggests that different multipliers should be chosen for different applications. For example, the output level of a VXO typically varies considerably over the tuning range of the oscillator. It is good practice to imediately follow a VXO with a limiter circuit so that LO chain performance is not a function of tuning. When a frequency multiplier is needed, using a CMOS logic chip after the VXO implements the limiting function with no additional parts. On the other hand, a microwave frequency multiplier chain with many stages of frequency multiplication, amplifiers and filters can benefit greatly from the use of diode balanced diode doublers. The linear input-to-output level relationship

makes it very easy to tune up all the preceeding stages just by observing the output. With bias resistors in the multipliers, each stage has a built-in test point. The entire LO multiplier chain can be tuned up using just a voltmeter.



Conservative amateurs who own Spectrum Analyzers may question the viability of tuning up LO chains without this critical piece of test equipment, but consider this: A

narrow bandpass filter followed by a diode detector is a one channel spectrum analyzer. Since balanced diode doublers must be preceeded by narrow filters to ensure sine wave drive, each multiplier stage is the ideal test instrument for tuning the previous stages—assuming that the filter elements have somewhat restricted tuning range so that they can't be tuned to the wrong harmonic.

Frequency multipliers using single transistors or transistors in balanced pairs are most useful when either parts count or DC power must be reduced. While it is possible to achieve good performance with a number of different types of frequency multiplier circuits, the use of balance doublers for even harmonic multiplication is highly recommended. The built-in suppression of all undesired outputs, linear output to input level relationship, broadband, non-critical frequency behavior, and no power supply requirements make it easy to build and adjust very high performance multiplier chains.

Below is a letter and more measurements I sent to Wes Hayward after making a few more measurements.

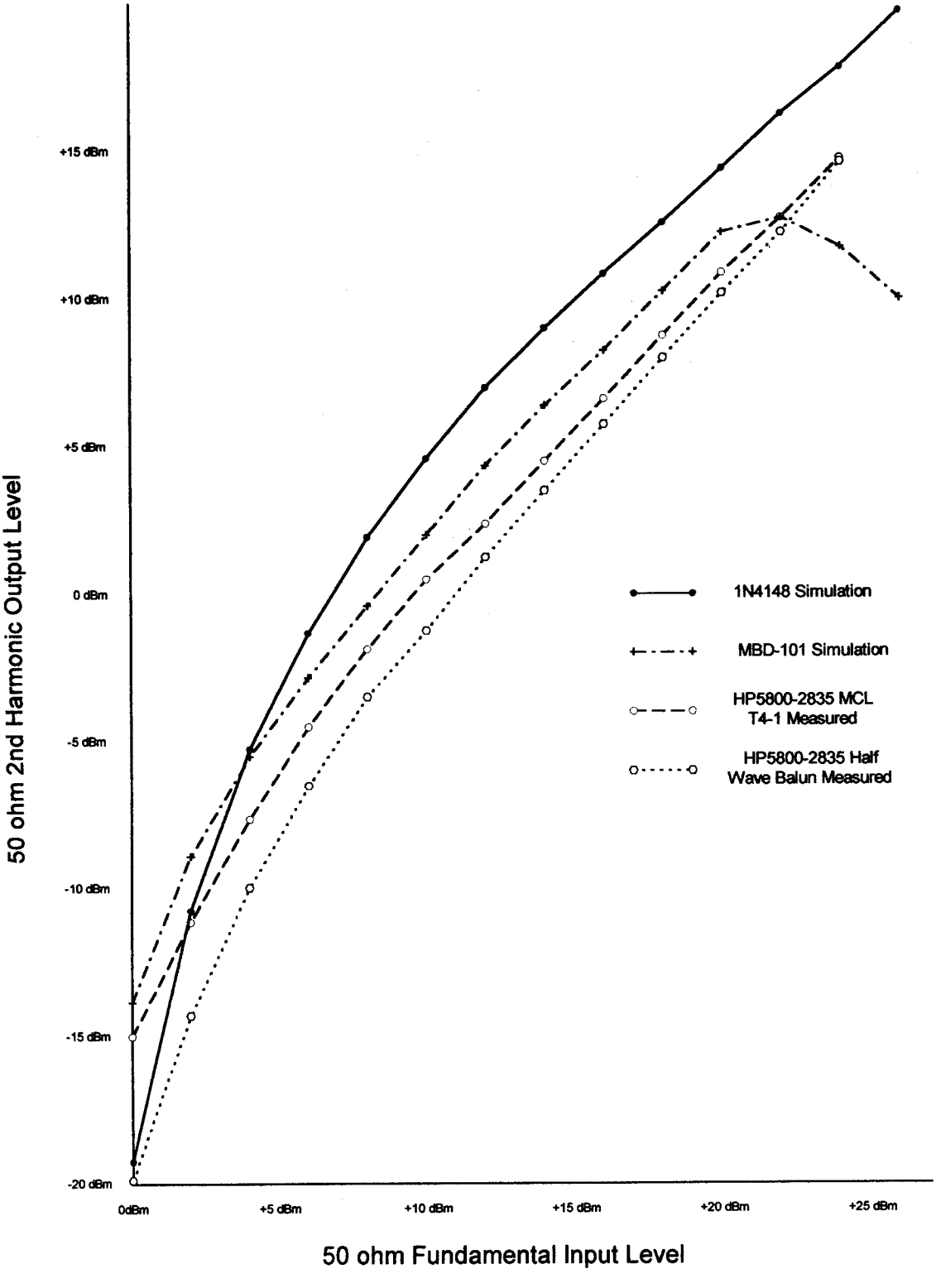
Hi Wes,

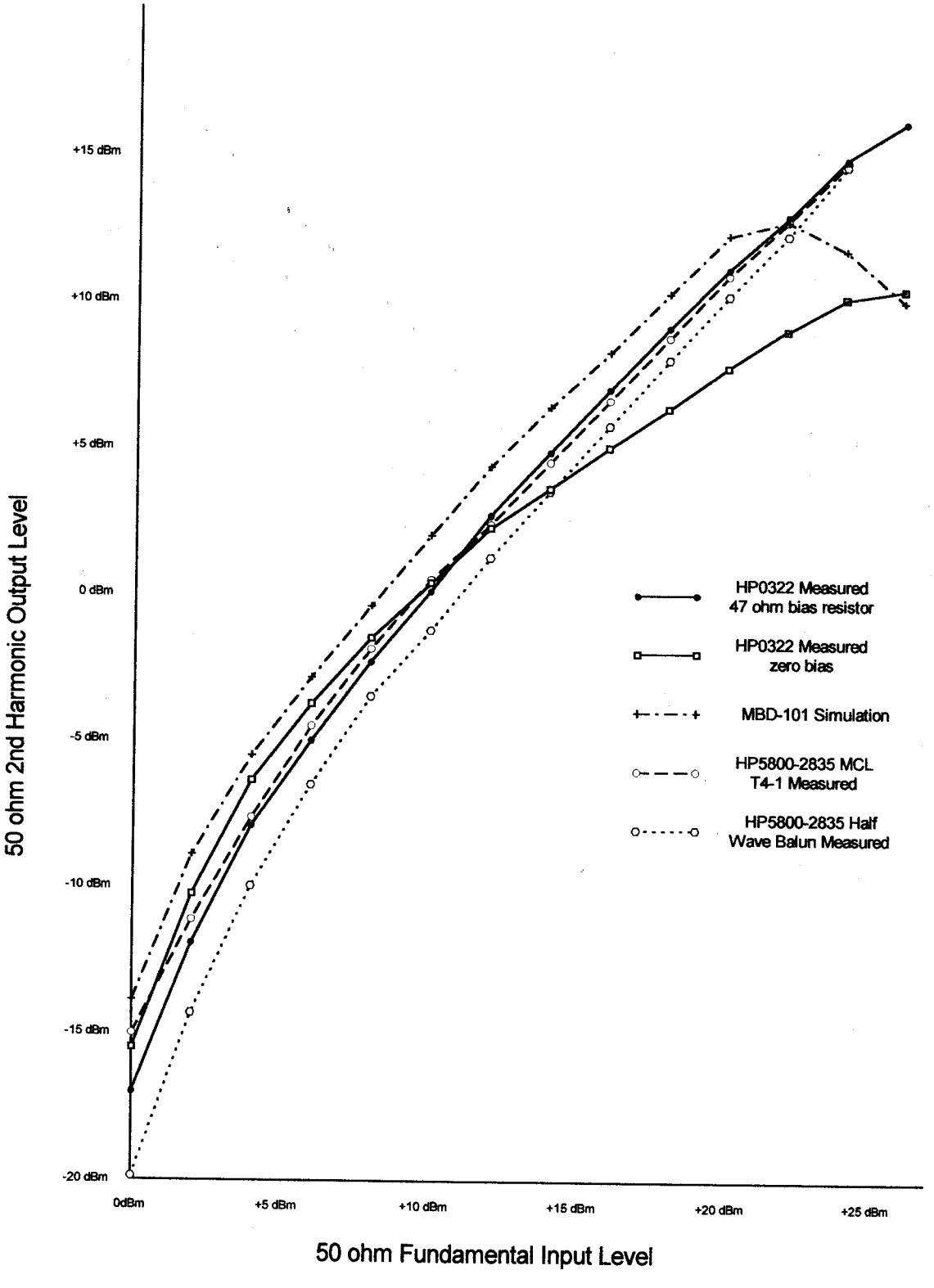
I did a few more sims this morning, sweeping drive level to two of the transformer doublers, one with MBD-101s and one with 1N4148s. I don't have a PSPICE model for the HP2835. The MBD-101 is close at low frequency and low drive level, but in the sims the MBD-101 folds over starting at about +20 dBm drive and the HP2835 doesn't fold until about +26 dBm in the measurements.

The 1N4148 is interesting in the simulations. It takes significantly more drive to get it started, as expected. At 0 dBm it puts out only about –20 dBm, and it doesn't hit 10 dB conversion loss until + 5 dBm drive. It keeps getting better until +12 dBm drive, where the simulated loss is only 5.0 dB! That holds until +16 dBm drive, where the loss starts to increase again. By +20 dBm drive, it is putting out +14 dBm and at +26 dBm drive it is putting out +19.7 dBm. These are simulations, of course, but it is a very brain-dead circuit that only requires that the diode behave like a diode. At +26 dBm drive, the DC dissipated in the 47 ohm bias resistor is 41.3 mW, so there is lots of available RF energy floating around to end up in the second harmonic. Still, only 5 dB conversion loss as a passive frequency doubler seems optimistic. Also, the 1N4148 has significantly more output on the fundamental and odd harmonics. This is to be expected, as the varacter modes and carrier storage times are more significant. I didn't see any evidence of parametric amplification in the sims, but I wasn't really looking for them in this simple, resistively loaded circuit with an ideal transformer.

Bottom line at this point is that I would use the microwave Shottkey diodes for a lab bench doubler, since it is wonderfully "linear" over a broad range of inputs and has significantly better suppression of undesired outputs. The switching diodes are a good choice for HF rigs, as they have lower simulated conversion loss, high output capability, acceptable suppression of the fundamental and odd harmonics, and are cheap and available. For higher power I'd try the switching diodes, and even try parallel combinations and or quadrature power splitting and recombining to get good matches and higher output capability. It might be possible to get a quarter watt out on the second harmonic of a 1 watt rig, broadband, passive and with a very good input match. This would be a useful book project, as the 1 watt rig already has to have clean sine wave output. Perhaps a VXO "unchirpable" for 12 m and 6 m, with the 6 m passive power doubler integrated into a dipole insulator.

The other interesting point is that diode doublers with "linear" behavior over a drive range greater than their conversion loss lend themselves to cascade doublers with no gain in between. 400 mW in at 36 MHz would give you +7 dBm at 144 MHz.


50 ohm 2nd Harmonic Output Level
+15 dBm
+10 dBm
+5 dBm
0 dBm
-5 dBm
-10 dBm
-15 dBm
-20 dBm
0dBm
+5 dBm
+10 dBm
+15 dBm
+20 dBm
+25 dBm
50 ohm Fundamental Input Level
1N4148 Simulation
MBD-101 Simulation
HP5800-2835 MCL T4-1 Measured
HP5800-2835 Half Wave Balun Measured


50 ohm 2nd Harmonic Output Level
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0 dBm
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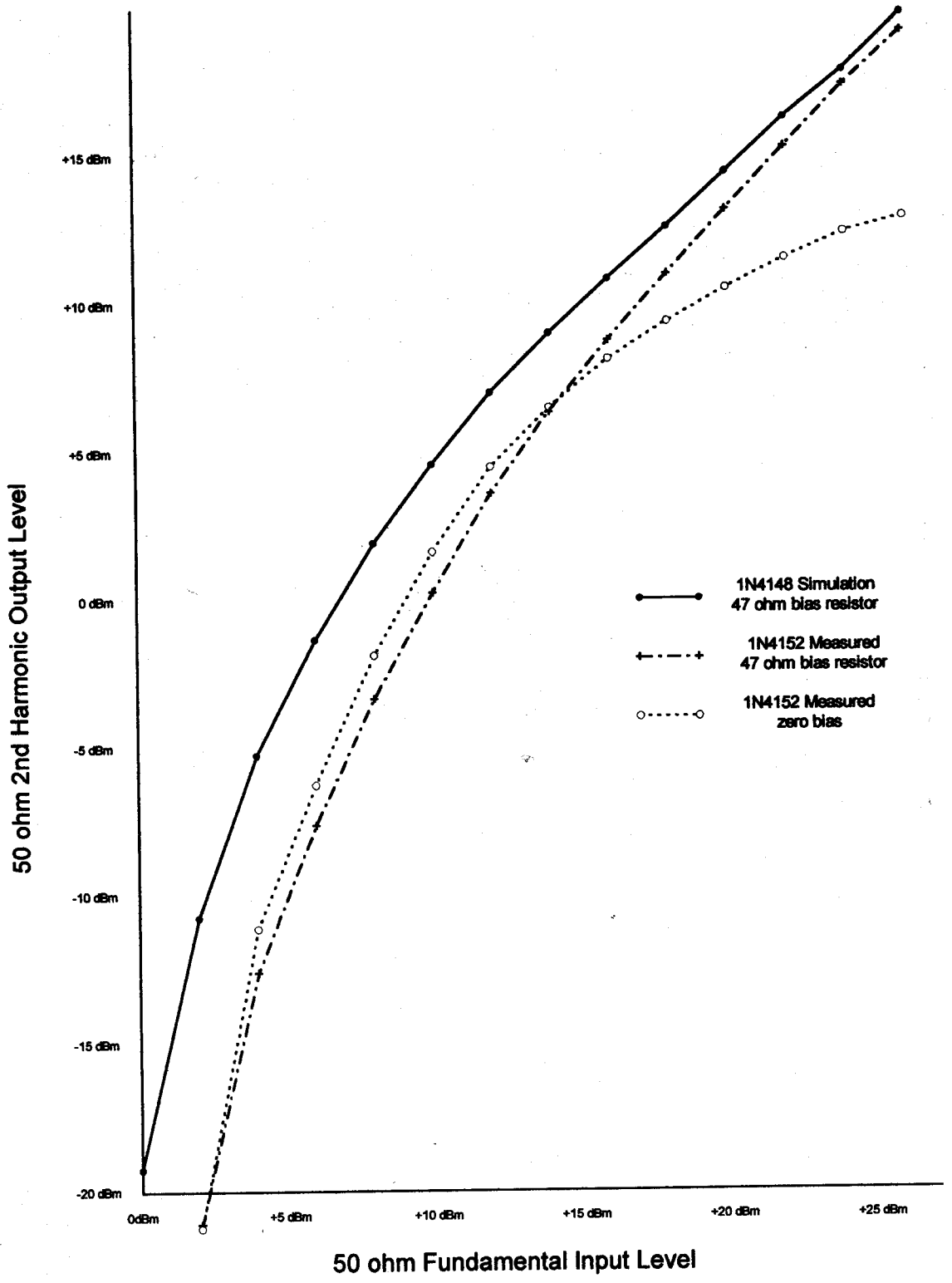
-15 dBm
-20 dBm
0dBm
+5 dBm
+10 dBm
+15 dBm
+20 dBm
+25 dBm
50 ohm Fundamental Input Level
HP0322 Measured
47 ohm bias resistor
HP0322 Measured
zero bias
MBD-101 Simulation
HP5800-2835 MCL
T4-1 Measured
HP5800-2835 Half
Wave Balun Measured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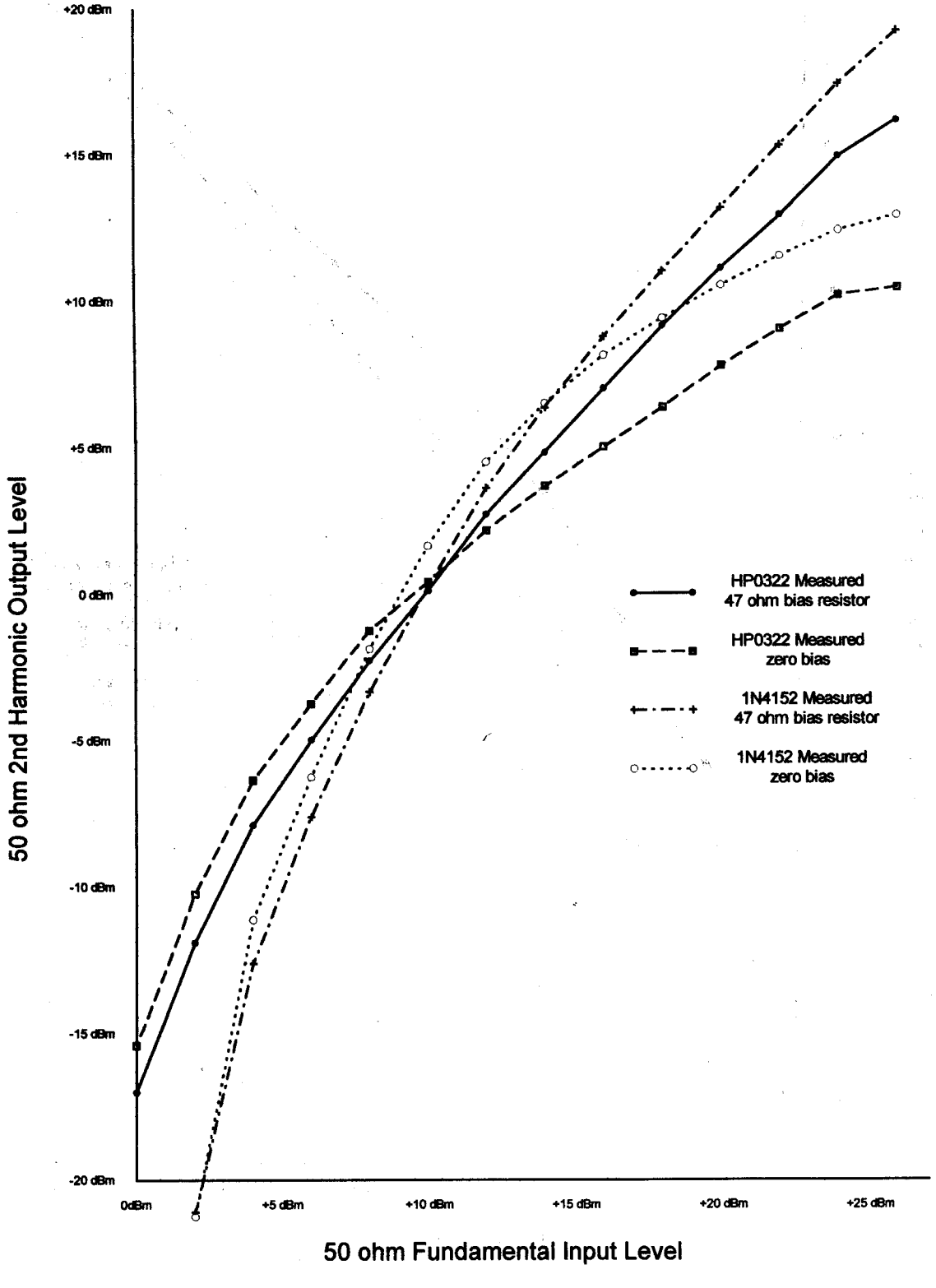
50 ohm 2nd Harmonic Output Level
0dBm
+5 dBm
+10 dBm
+15 dBm
+20 dBm
+25 dBm
50 ohm Fundamental Input Level
1N4148 Simulation
47 ohm bias resistor
1N4152 Measured
47 ohm bias resistor
1N4152 Measured
zero bias


+20 dBm
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+10 dBm
+5 dBm
0 dBm
-5 dBm
-10 dBm
-15 dBm
-20 dBm
50 ohm 2nd Harmonic Output Level
0dBm
+5 dBm
+10 dBm
+15 dBm
+20 dBm
+25 dBm
50 ohm Fundamental Input Level
HP0322 Measured
47 ohm bias resistor
HP0322 Measured
zero bias
1N4152 Measured
47 ohm bias resistor
1N4152 Measured
zero bias