Frequency Stabilization of L-C Oscillators

So you have a clean, pure L-C VFO, but it drifts. Here's a way of stabilizing its frequency.

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For many builders and users of simple receivers and transmitters, the long-term stability of oscillators forms a major problem. Usually, oscillator drift caused by temperature variations is reduced by the use of temperature sensitive components such as NTC capacitors. However, crystal stability is seldom achieved.

This article describes a digital method for frequency stabilization by which an HF L-C oscillator can achieve the stability of a crystal oscillator. This simple unit can be used for new construction or as an add-on to existing equipment.

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Principles of Stabilization

Two simple principles exist for L-C oscillator frequency stabilization (I'll disregard complex synthesiser systems.) One method uses a digital frequency counter that measures a VFO frequency periodically. Any deviation between the measured values and a preset value results in automatic correction of the VFO frequency. The principle can be executed with simple means.[1]

This article describes the second principle, which uses a mixer to downconvert the VFO frequency to a low value for further treatment. It has significantly better performance than the technique mentioned above.

[1]Notes appear on page 23.

Basic Operating Principle

A special form of frequency-locked loop is used. Fig 1 shows the block diagram. The heart of the system is a digital mixer. The VFO frequency is mixed with a crystal oscillator to a low frequency, which is then compared to a reference frequency. Any deviation between the frequencies, caused by drift, generates a control voltage that corrects the VFO.

The digital mixer is a standard high-speed CMOS D-type flip-flop. Its operation as a digital mixer is not intuitively clear, so I will explain it in some detail.

In a D flip-flop the information on the data input (1 or 0) is transferred to the Q output on the low-to-high transition of the clock pulse. In this case,

the clock pulse is a 10-Hz signal derived from a crystal oscillator.

The VFO signal is connected to the data input. In this way the D flip-flop acts as a digital sample-and-hold circuit. Since the output can change only at the rising edge of the clock pulse, the output frequency can never become higher than 5 Hz (half the clock frequency), but it is still determined by the two input frequencies. Let's see how.

If at each transition of the 10-Hz clock the VFO signal is high (or low)—exactly in phase with the clock—the output will remain high (or low). The output frequency is 0 Hz.

If the VFO frequency is tuned slightly upwards, say 1 Hz, an output frequency of 1 Hz will occur. If the VFO frequency increases further, the output increases equally up to its maximum value of 5 Hz. As the VFO frequency increases further, the mixer output goes back to 0 Hz and rises again as the VFO continues to be tuned higher.

If we keep the output of the digital mixer constant by automatically controlling the VFO, the VFO's frequency must be constant as well. We have made a frequency-locked loop.

At a VFO frequency that is 10 Hz higher, the digital mixer will generate exactly the same output frequency. This type of frequency-locked loop has many stable operating points, with 10-Hz spacing between the lock points.

In a stable loop, a fixed ratio N exists between the VFO frequency and the clock frequency. N is always a very large number. (See the calculations in the Appendix.)

Automatic frequency control of the

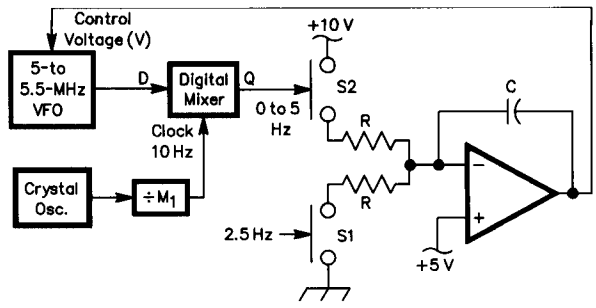

Fig 1—Block diagram of the basic frequency-stabilization system.

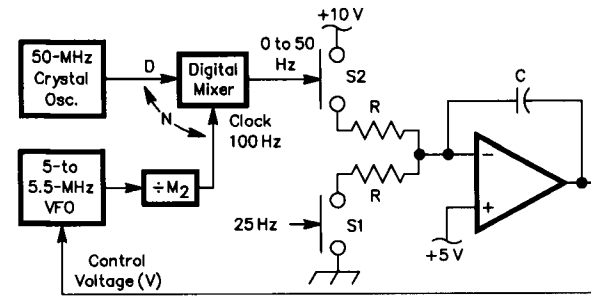

Fig 2—Block diagram of an improved system.

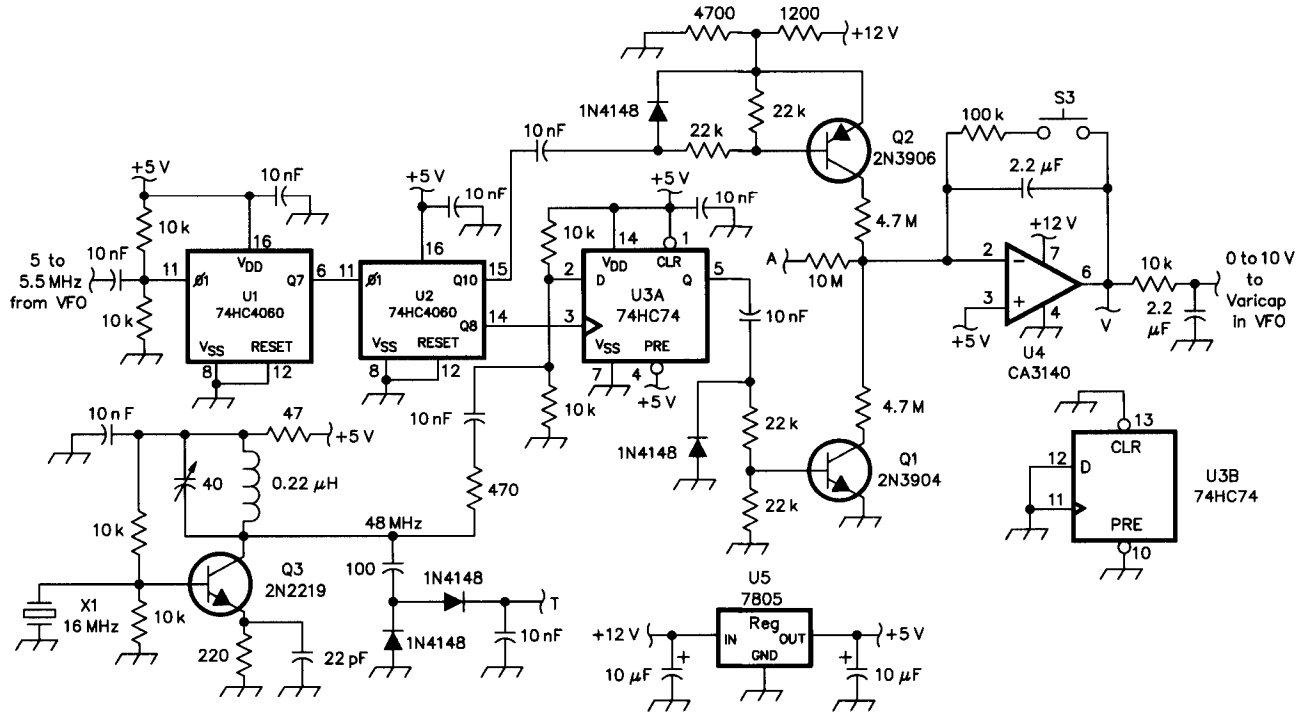

Fig 3-Schematic diagram of the frequency-stabilization circuit. The VFO circuit is not shown.

VFO is achieved in the following way:

The 0 to 5-Hz output frequency of the digital mixer is compared to another low frequency. (This frequency does not need to be crystal stable.) 2.5 Hz is a suitable value, as the output of the digital mixer will then stabilize in the middle of its range. This reference signal is conveniently derived from the same crystal oscillator as the 10-Hz frequency: ($f_{clock}/4$).

Both signals momentarily close switches S1 and S2, resulting in a slightly increased or decreased charge in the hold capacitor, C, of the integrator after each pulse.

The ouput voltage, V, of the integrator is connected to a voltage-variable capacitor in the VFO. So the VFO frequency also changes slightly up or down after each pulse until both low frequencies are the same. The frequency stays on such a stable lock point, and any slow frequency drift is corrected.

The long-term stability of the VFO is then determined only by the crystal oscillator from which the 10-Hz signal is derived.

Advanced Operating Principle

A considerable improvement is still possible. In the system described above, the correction pulses have a frequency of 2.5 Hz. If it were possible to increase that frequency and still maintain the 10-Hz lock points, a higher VFO drift rate could be corrected; or with the same drift rate, a faster correction with smaller individual steps would be possible.

This is what happens in the system shown in Fig 2. The main difference between Fig 1 and Fig 2 is the location of divider *M*. The crystal oscillator provides a 50-MHz signal to the digital mixer. Suppose that the VFO frequency of 5 MHz is divided by the fixed divider M_2, when M_2=50,000. This results in a 100-Hz signal to the clock input of the D flip-flop. Its maximum output frequency will now be 50 Hz, ten times as high as before. A little arithmetic will show that the spacing of the lock points is still 10 Hz.

N is the ratio between the frequencies of the crystal oscillator and the output of divider M_2. In the example N=500,000, M_2=50,000.

When the system is stable the following relation holds:

$$F_{vfo}/M_2 = F_{xtal}/N \quad \text{(Eq 1)}$$

resulting in:

$$F_{vfo} = F_{xtal} \bullet M_2/N \quad \text{(Eq 2)}$$

With these values the VFO frequency will be 5,000,000 Hz.

The next stable point is when N=N+1, so N=500,001. Again using Eq 2, this results in a VFO frequency of 4,999,990 Hz—giving a spacing of 10 Hz. (The Appendix shows that with this system the spacing varies with *N* and is only exactly 10 Hz with the numbers used above.)

Operation in Practice

During normal manual tuning of the VFO, the action of the controller is not noticed, as it is slow. After manual tuning, the frequency creeps to the nearest 10-Hz lock point, which is never further away than 5 Hz up or down. (A musician with absolute pitch might notice such a small change in a receiver CW tone, but I can't.)

Of course the action of the controller must be small to avoid overshoot of the frequency. Each corrective pulse to the integrator may change the VFO frequency a very little, less than 1 Hz. You don't want the VFO to "hunt."

Acceptable Distance between Lock Points

In the system described, the spacing between lock points is 10 Hz. I found that a spacing of up to 40 Hz is still acceptable. This means that there is quite some freedom in the design, allowing other VFO or crystal oscillator frequencies to be used.

In the practical system described below, the spacing between lock points varies between 15.9 Hz and 19.2 Hz when the VFO is tuned from 5 to 5.5 MHz.

Detailed Circuit

The practical circuit is shown in Fig 3. Two cascaded binary dividers, U1 and U2, divide the VFO frequency by 32768 in 15 cascaded stages (7 in U1 and 8 in U2). This forms the clock signal for the 74HC74 D flip-flop, U3A. (Only one of the two flip-flops in the IC is used.)

The crystal oscillator operates at 48 MHz. I used a 16-MHz crystal in third-overtone mode in a design taken from *Solid State Design for the Radio Amateur*.[2] I added a diode detector with which the peak-to-peak amplitude of the 48-MHz voltage can be measured.

Switches S1 and S2 of Figs 1 and 2 are formed by transistors Q1 and Q2. These are normally off. The on time is determined by the differentiating R-C networks in their bases and is less than 1 ms per pulse. Via the 4.7-MΩ resistors, the output of the integrator changes slightly after each pulse.

The output voltage of the integrator has a range of 0 to 10 V. After turn-on it starts approximately in the middle of its range. The small ripple on the output signal of the integrator caused by the correction pulses is smoothed by an R-C filter before it is connected to the varicap in the VFO.

In case the output should become saturated (0 or 10 V), it can be brought to midrange again by momentarily pressing S3. I advise mounting S3 on the front panel of the equipment in which the stabilizer is built. Press it now and then when you start to retune the radio.

No details are given of the VFO and associated buffer circuits, but the tuning range of the varicap in the VFO must be larger than the expected drift. A convenient sensitivity is 1 kHz/V. The phase of the action of the varicap is not important. (The frequency-locked loop will stabilize in the range of 0 Hz to maximum or in the range of maximum to 0 Hz of the output of the digital mixer.)

The amplitude of the VFO signal to the first digital circuit must be approximately 4 V p-p. The input impedance of the digital circuits is high.

The unit needs a supply voltage of 12 V, draws a current of some 20 mA and has its own 5-V regulator, U5, to supply the crystal oscillator and digital circuits with 5 V.

Construction

I used the "ugly construction" technique as described in *The 1995 ARRL Handbook*. (I prefer the name *amateur-type surface-mounted technology!*)

I placed the ICs upside down on the copper cladding of a piece of printed-circuit board. The supply connections of all ICs are decoupled with 10-nF ceramic capacitors that, together with the ground supply connections, keep the ICs in place. I used thin insulated wire to make all connections and soldered directly to the IC pins.

For the coil in the overtone oscillator circuit, I used a small RF choke of 0.22 µH. A 1/2-inch, 6-turn air coil wound on a 1/4-inch form worked fine also.

The 2.2-µF capacitor in the integrator circuit must be a type with little leakage—polycarbonate or polystyrene. The resistors connected to the input of U4 should be mounted close to the IC.

I suggest mounting the circuit in a small metal box to avoid any influence

of RF signals from transmitters and to avoid interference to reception caused by the switching signals of the CMOS ICs.

Adjustment and Testing

The only adjustment is the 40-pF trimmer capacitor in the 48-MHz overtone oscillator. Oscillation can be confirmed by measuring the dc voltage at test point T, which must be about 4 V. The amplitude at this point can be adjusted with the trimmer; the precise frequency is not important.

When all the wiring is done the stabilizer should work. If not, the individual circuits can be tested in the following way. With a VFO frequency of 5 MHz the output of U1, pin 6 must be 39 kHz, and the outputs of U2, pins 15 and 14 must be 152 Hz and 38 Hz, respectively. Besides confirming proper operation of the ICs with an oscilloscope, a multimeter can be used as well. If U1 and U2 operate properly, their outputs will be square waves and a dc voltmeter will indicate 2.5 V on the outputs. If they do not work, their outputs will be 0 or 5 V.

The integrator and the action of the varicap in the VFO can be tested as well. Measure the dc output voltage of the integrator on test point V. The impedance at that point is low, so any multimeter can be used.

Disconnect the 4.7-MΩ resistors from Q1 and Q2 and press S3. The output voltage should be 5 V. Connect point A to ground for a few seconds. The output voltage should increase at a rate of 1 V every 4.4 seconds. When point A is open, the output should remain stable at the last value. Connecting point A to +12 V should give the opposite action (but slightly faster).

When the output voltage is changed from 5 to 6 V, the VFO frequency should change about 1 kHz. In normal

Appendix

Fig A shows a simplified block diagram of the frequency stabilization system. The simplification concerns the output of the frequency comparator, which is assumed to be 0 Hz here and which is a low frequency in the actual system. The difference is not significant for these calculations. The divider N of Fig A is not really present in the actual circuit; it symbolizes the ratio of the two frequencies at the inputs of the digital mixer.

The following relation holds for the frequency-locked loop:

$$\frac{f_v}{M}=\frac{f_x}{N} \quad \text{(Eq 1)} \quad \Rightarrow \quad f_v=\frac{f_x M}{N} \quad \text{(Eq 2)}$$

The next lock point exists when N=N+1. The difference D between lock points then becomes:

$$D=\frac{f_x M}{N}-\frac{f_x M}{N+1}=f_x M\left(\frac{1}{N}-\frac{1}{N+1}\right)$$

The term between brackets can be written as:

$$\frac{N+1-N}{N(N+1)}=\frac{1}{N(N+1)}$$

As N is always large compared with the 1 in the denominator, only a negligible error results if the term is simplfied to:

$$\frac{1}{N^2} \Rightarrow D=\frac{f_x M}{N^2} \qquad \text{(Eq 3)}$$

From Eq 1 it also follows that:

$$N=\frac{f_x M}{f_v} \qquad \text{(Eq 4)}$$

Substituting Eq 4 into Eq 3 results in:

$$D=\frac{f_v^2}{M f_x} \qquad \text{(Eq 5)}$$

We can now fill in the values used in the practical system (Fig 3) with:

$f_v = 5.0\,\text{MHz}$, $M = 2^{15}$, $f_x = 48\,\text{MHz}$

These values result in the the difference D between lock points as:

$$D=\frac{\left(5\times10^6\right)^2}{48\times10^6\times2^{15}}=15.98\,\text{Hz} \quad f_{clock}=\frac{5\times10^6}{2^{15}}=152.58\,\text{Hz}$$

For a VFO frequency of 5.5 MHz we get:

$$D=\frac{\left(5.5\times10^6\right)^2}{48\times10^6\times2^{15}}=19.23\,\text{Hz} \quad f_{clock}=\frac{5.5\times10^6}{2^{15}}=167.84\,\text{Hz}$$

The frequencies of the correction pulses are $f_{clock}/4$: 38.14 Hz at 5 MHz and 41.96 Hz at 5.5 MHz.

Design Method for Other Frequencies

Given the frequencies of the VFO and of the overtone oscillator in MHz and the desired distance between lock points D in Hz, calculate M by:

$$M=\frac{f_v^2}{f_x D}\times10^6$$

Select the nearest power of 2 and check if D is below the desired value according to:

$$D=\frac{f_v^2}{M f_x}\times10^6$$

In case D deviates too much from the desired value, take the next higher value for M and repeat the calculation for D.

Example

A VFO operates between 37 and 38 MHz and the overtone oscillator operates at 80 MHz. The required distance between lock points, D, is 20 Hz. Calculate M:

$$M=\frac{38^2}{80\times20}\times10^6=902.500$$

Select M=1,048,576 (20 cascaded binary dividers). Calculate D at 37 and at 38 MHz, resulting in 16.3 Hz and 17.2 Hz, respectively. As D is below the desired value of 20 Hz over the whole range of the VFO, the selected value of M is the correct one.

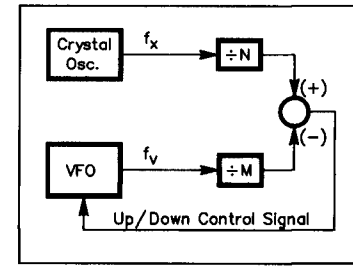

Fig A—A simplified block diagram of a frequency-locked loop.

operation, point A is left open; it is used for test purposes only.

Testing of the frequency discriminator can take place in the following way. Reconnect the 4.7-MΩ resistor to Q2. The integrator output should decrease at a rate of about 1 V every 100 seconds. The 4.7-MΩ resistor connected to Q1 has the opposite effect. The VFO frequency should become stable with both resistors in place and point A open.

(This 1 V per 100 s corresponds with a change in VFO frequency of 1 kHz per 100 s. This is the maximum drift rate that can be corrected. In 100 s, 3800 correction pulses have been generated, so the change in VFO frequency is 0.26 Hz per correction pulse.)

The values given above are typical values. Because of component tolerances, results of ±50% from the values given are possible and are fully acceptable.

Results and Further Experimentation

I have used the circuit in Fig 3 on a number of L-C oscillators, including one operating at 38 MHz. In all cases I was able to obtain virtually drift-free operation.

In this design I used 74HC integrated circuits. I found that 74HCT types also work well without any circuit modification.

According to the data sheets, the maximun toggle frequency of a 74HC74 is 76 MHz (59 MHz for a HCT version), and the maximum input frequency for a 74HC(T)4060 is 88 MHz. My ICs still operated at up to 95 MHz. This means that the circuit can be used with considerably higher VFO and crystal frequencies than mentioned so far. To verify this I have used the system on a 38-MHz L-C oscillator in combination with an 80-MHz overtone oscillator (of different design than that in in Fig 3). In this case M=1.048.576 (20 cascaded binary stages using the output of the first IC from pin 1 instead of pin 6. Be aware that in a 4060 IC not all divider ouputs are available.) At 38 MHz I got reliable operation with a spacing between the lock points of 17.2 Hz. After a cold start the loop stabilized within seconds and stayed on the same lock point for hours.

The quality of the L-C oscillator itself must already be very good: a T9 tone without appreciable hum, jitter, microphony, hand effects, etc, with long-term drift as the only deficiency.

There are two drawbacks to this stablization technique. One is that it is not easily possible to work split frequency or use an RIT function when the stabilizer is in operation. After a number of jumps from one frequency to the other, the VFO may lose its original lock point. Secondly, with a fixed value of M, the distance between lock points varies with the square of the VFO frequency, making the system less suitable for a multiband VFO. In such a case, M should be selectable, which increases complexity.

Conclusion

With this simple, low-cost circuit the long-term stability of HF L-C oscillators can achieve the stability of a crystal oscillator, while maintaining fine tuning steps.

Notes

[1]Spaargaren, Klaas, PA0KSB, *Ham Radio*, Dec 1977. (This is still published in the latest edition of the British *RSGB Radio Communication Handbook*.)

[2]*Solid State Design for the Radio Amateur*, published by ARRL.

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