By Jacob Makhinson, N6NWP

A Drift-Free VFO

Build this clean, quiet, stable VFO.

The last decade has seen a considerable improvement in the area of receiver IMD distortion (IMD) characteristics, which has enhanced the ability of amateur receivers to handle strong signals. Conversely, the ability of receivers to receive weak signals in the presence of strong unwanted signals is limited either by the receiver IMD capabilities or local-oscillator (LO) phase noise. The phase noise of a properly designed, free-running LC VFO need not limit dynamic range.

Many VFO designs have appeared in the Amateur Radio literature, and the quest for a low-drift VFO hasn't ceased. If the frequency-stability requirements are stringent, the thermal-drift compensation can be very tedious. Wes Hayward's recent *QST* article[1] devoted to VFO drift compensation is an excellent example of this difficult pursuit.

For many designers, the quest for stability ended when low-cost frequency synthesizers appeared. Unfortunately, synthesizers come with problems—notably phase-noise problems and spurious responses. Building a low-phase-noise synthesizer is a serious undertaking—it requires considerable technical skill and possibly prohibitive cost and circuit complexity.

This article demonstrates that an LC VFO still offers excellent spectral purity, low cost, ease of construction and component availability. It shows that it is possible to combine in a VFO both very low phase noise and exceptionally good long-term stability.

Design Criteria

To avoid degradation of the receiver's front end, several requirements should be imposed on the phase noise level of the VFO. An excessively high level of close-in phase noise (within the bandwidth of the SSB signal) may reduce the receiver's ability to separate closely spaced signals. As an example, a 14-pole crystal filter described in Note 2 provides adjacent-signal rejection of 103 dB at a 2-kHz offset. This requires the use of a VFO with –139 dBc/Hz

[1]Notes appear on page 36.

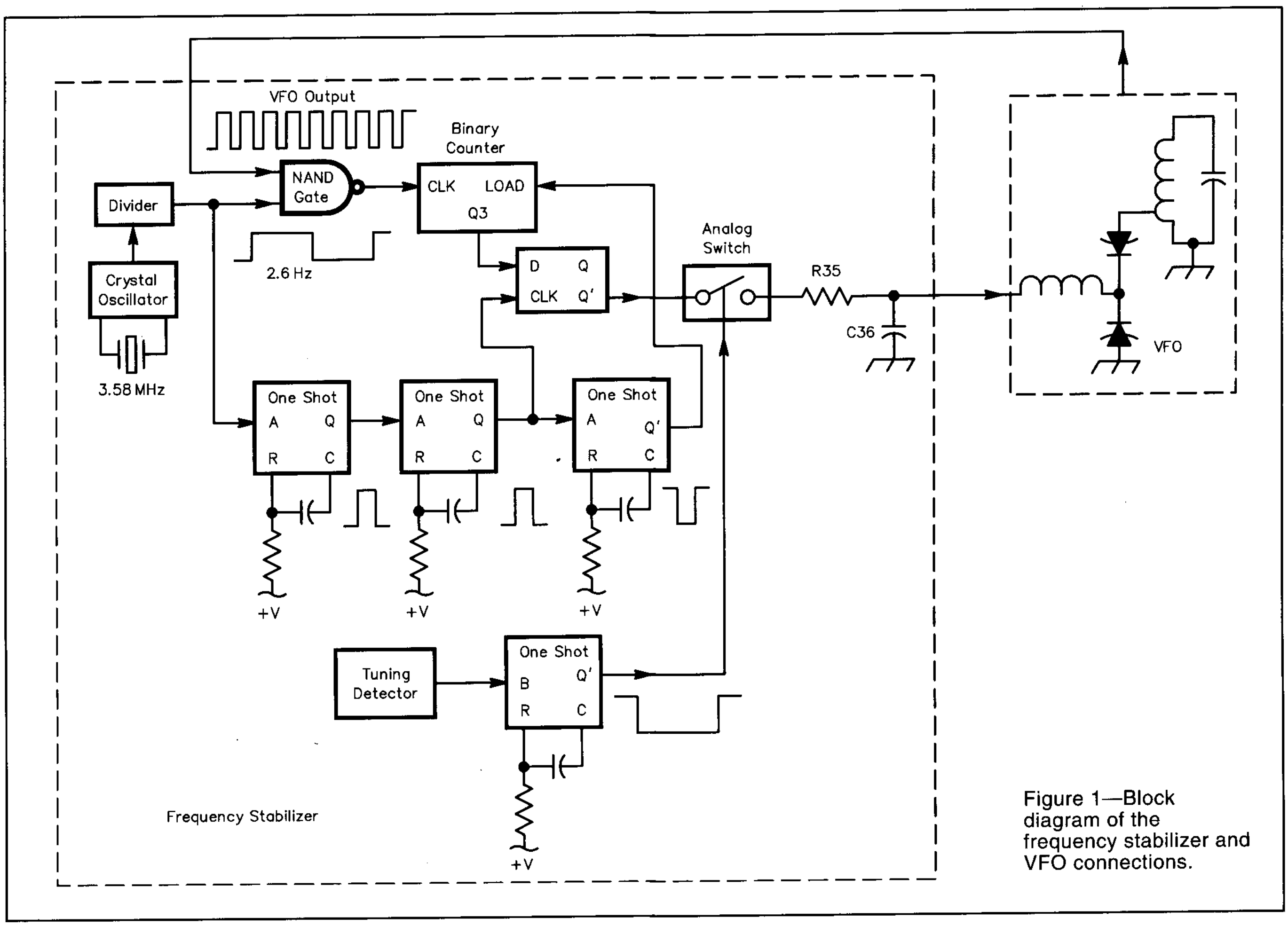

Figure 1—Block diagram of the frequency stabilizer and VFO connections.

phase noise at a 2-kHz offset.

$$Pn = P - 10 \log(BW) = -103 - 10 \log(4000) = -139 \text{ dBc/Hz}$$

where

Pn = VFO phase-noise spectral density, in decibels relative to the carrier output power, in a 1-Hz bandwidth (dBc/Hz)

P = VFO power level (dBc) in a given bandwidth (BW)

BW = test bandwidth, in Hertz

In addition, excessive close-in phase noise may lead to reciprocal mixing, where the noise sidebands of a VFO mix with strong off-channel signals to produce unwanted IF signals.

Excessive far-out phase noise may degrade the receiver dynamic range. In a properly designed receiver, the phase-noise-governed dynamic range (PNDR) should be equal to or better than the spurious-free dynamic range (SFDR). We can calculate the PNDR:[3]

$$PNDR = -Pn - 10 \log(BW)$$

Assuming the PNDR equals the SFDR at 112 dB in a 2.5-kHz IF noise bandwidth, the required far-out phase noise level is –146 dBc/Hz:

$$Pn = -SFDR - 10 \log(BW) = -112 - 34 = -146 \text{ dBc/Hz}$$

Another form of VFO instability—frequency drift—has always been a nuisance and a great concern to the amateur community. The objective of this project was to keep the long-term frequency drift (seconds, minutes, hours) under 20 Hz. This includes thermal drift from both in-

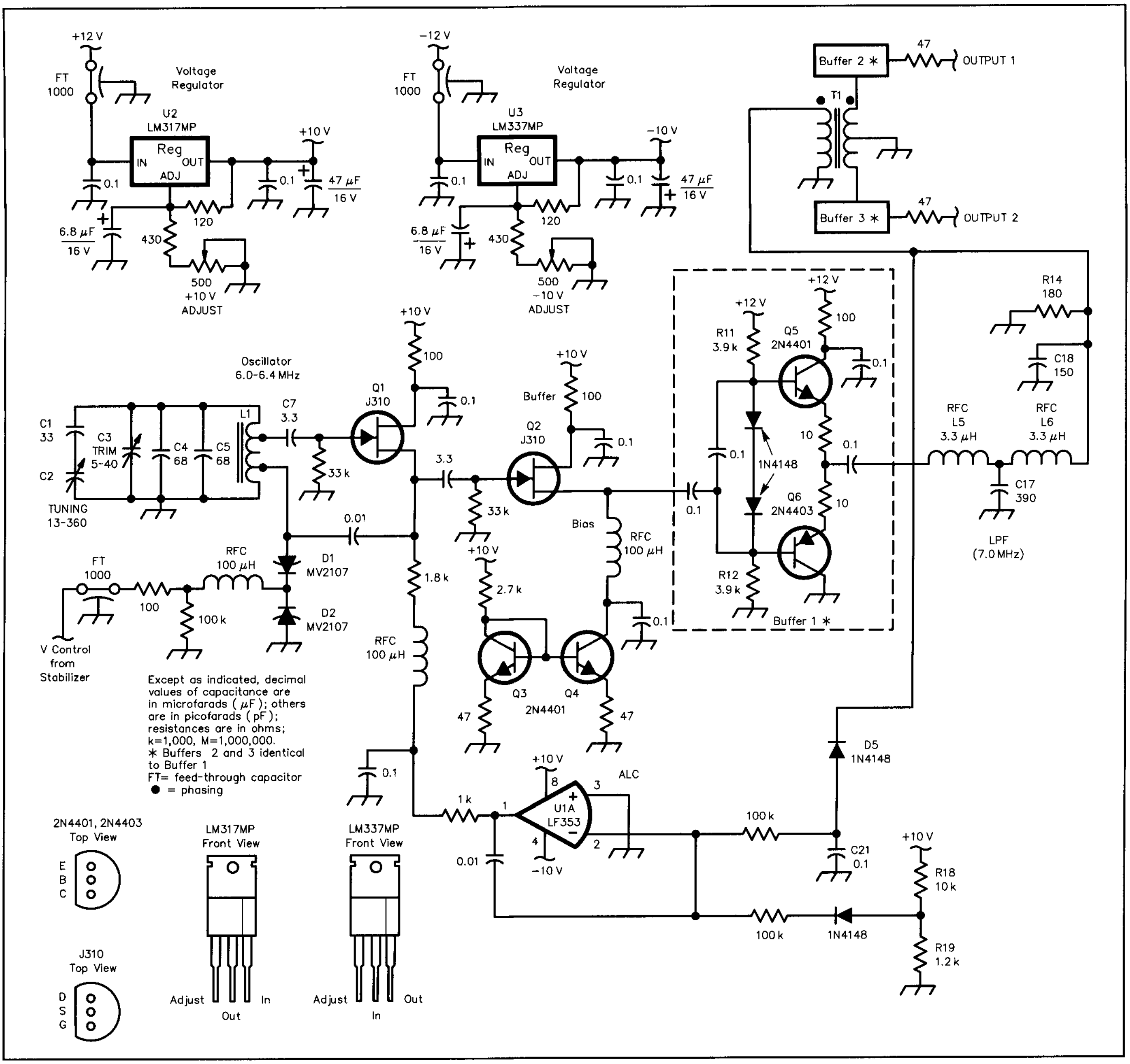

Figure 2—VFO schematic. Buffers 2 and 3 are identical to Buffer 1. Most of the parts are available from Mouser Electronics, Digi-Key Corporation or Allied Electronics. The cores for L1 and T1 are from Amidon Associates.[7] Use 1/4-W, 5%-tolerance carbon-composition or film resistors and ceramic, 20%-tolerance capacitors unless otherwise indicated. RF chokes or encapsulated inductors may be used for those labeled "RFC."

Q1, Q2—J310, N-channel JFET (Allied)
D1, D2—MV2107 or ECG/NTE613 tuning diode (Varicap, Allied)
L1—29 turns of #18 AWG enameled copper wire on a T-80-6 iron-powder toroidal core tapped at 4 turns and 20 turns from the cold end (Amidon)
T1—#32 AWG enameled copper wire on a BN-43-2402 two-hole ferrite balun core (Amidon) primary: 5 turns; secondary: 16 turns, center tapped
Vector part #8007 circuit board (Digi-Key)
Vector part #T44 terminals (Digi-Key)

ternal heating and environmental changes.

Block Diagram

The block diagram of Figure 1 shows the LC VFO and the frequency stabilizer. The stabilizer monitors the VFO frequency and forms an error signal that is applied to the VFO to compensate for frequency drift. This technique, which is capable of stabilizing a VFO to within a few hertz, was devised by Klaas Spaargaren, PAØKSB, and first described in *RadComm* magazine in 1973.[4] My project builds upon Spaargaren's idea and presents a few refinements.

The stabilizer converts a free-running VFO into an oscillator that can be tuned in the usual fashion, but then locks to the nearest of a series of small frequency steps. Unlike traditional PLL frequency synthesizers, the stabilizer has no effect on the phase-noise performance of the VFO; it only compensates for thermal drift.

The timing signal (2.6 Hz) is derived from a crystal oscillator via a frequency divider. The timing signal drives a NAND gate to provide a crystal-controlled time window, during which the binary counter counts the VFO output. When the gate closes, the final digit of the count remains in the counter. For counts 0 to 3, the Q3 output of the counter is a logic 0; for counts of 4 to 7, a logic 1.

The result is stored in a D flip-flop memory cell: When the 2.6-Hz timing signal goes low, the first of three one-shots triggers. The second follows and clocks the binary counter Q3 output into the memory cell. The negative-going pulse from the third resets the counter for the next counting sequence.

The output of the memory cell is applied to an RC integrating circuit with a time constant of several minutes. This slowly changing dc voltage controls the VFO frequency via a couple of Varicaps connected to a tap on the VFO coil.

If the counter output is 0, the memory-cell output is 1, which charges C and increases the VFO frequency. A counter output of 1 discharges C and decreases the VFO frequency. The stabilizer constantly searches for equilibrium, so the VFO frequency slowly swings a few hertz around the lock frequency. The circuit limits the frequency swing to a maximum of ±2 Hz, typically ±1 Hz.

A difficulty arises when the operator changes frequency because the control voltage is disturbed. If the memory-cell output connects directly to the RC integrator, the frequency correction that occurs immediately after tuning results in a frequency hop. To overcome this problem, an analog switch disconnects the integrator from the memory during tuning. The tuning detector—an infrared interrupter switch and a one-shot—controls the analog switch.

Circuit Description

VFO

The VFO is a tapped-coil Hartley oscillator that is optimized for low phase noise (see Figure 2). Ulrich Rohde compiled a set of design rules intended to minimize the phase noise in oscillators.[5] The guidelines implemented in this design are:

- Maximize the unloaded Q of the resonator
- Maximize the RF voltage across the resonator
- Avoid device saturation at all costs
- Choose an active device with a low noise figure
- Minimize phase perturbation by using a high-impedance device (FET)
- Don't use a gate-clamping diode to limit voltage swing

The tank coil, L1, has an iron-powder toroidal core; coil Q exceeds 300. C1, C4, C5 and C7 are NP0 (C0G) ceramic capacitors (5% or 10% tolerance). C2 is the main tuning capacitor, and C3 is a small ceramic trimmer capacitor.

The VFO frequency range is set from 6.0 MHz to 6.4 MHz (to accommodate a 20-meter receiver with an 8-MHz IF). The loaded Q of the resonator is kept high by using a tapped coil and loose coupling to the gate of the FET through C7 (more than 8 kΩ at 6 MHz). The RF voltage swing across the resonator exceeds 50 V, P-P. Varicaps D1 and D2, which compensate for thermal drift, are connected across the coil's lower tap (less than 14% of the total turns) and have a negligible effect on overall phase-noise. J310 is the TO-92 version of U310—a very low-noise FET in HF applications.

An ALC loop limits the voltage swing. The signal is sampled at the primary of T1, rectified by the D5-C21 network and fed to the inverting input of an integrator, U1A, where it is compared against the reference voltage at the junction of R18 and R19. The dc voltage at the integrator output sets Q1's drain current so that the signal swing at T1's primary is always 2.5 V, P-P. The ALC loop also makes VFO performance independent of Q1's pinch-off voltage. The signal at Q1's source is a 6.5-V, P-P, sinusoid with almost no distortion.

Q2 is a high-impedance buffer that is loosely coupled to Q1. Q2's drain current is set to 3.4 mA (by the constant-current source, Q3-Q4) regardless of Q2's pinch-off voltage.

Buffer 1 is a push-pull stage biased into slight conduction by resistors R11 and R12. It has excellent linearity and a very low output impedance, which is required to drive an LC filter. The filter (L5, L6, C17, C18 and R14) is a four-pole, 0.1-dB Chebyshev low-pass filter with a ripple frequency of 7 MHz. All harmonics at the VFO output are at least 45 dB below the fundamental.

T1 provides the two complementary outputs required for a commutation mixer and raises the voltage swing at the VFO output.

Buffers 2 and 3 are electrically identical to buffer 1. They further decouple the VFO from its load and serve as low-distortion 50-Ω drivers. The signal level at each output is 4 V, P-P, when driving a high-impedance load (eg, a CMOS gate), +10 dBm when driving a 50-Ω load.

Frequency Stabilizer

NAND gates U4A and B (see Figure 3) comprise a Pierce crystal oscillator. The timing signal (2.6 Hz) appears at the output of the frequency divider (U5, U6, U7 and U8A). The exact frequency of the crystal and the timing signal is unimportant, but the stabilizer has been optimized for 2.3 to 2.7 Hz.

There are two requirements for the crystal oscillator: No harmonics should fall in the IF passband, and the crystal should have a low temperature coefficient. Crystal-oscillator thermal drift should not exceed 10 Hz within the temperature operating range. Crystals in HC-33 cases with frequencies between 2.0 and 3.58 MHz worked best for me. The frequency divider is sufficiently flexible to provide the desired timing-signal frequency.

U4C, biased into a linear range, converts the sinusoidal signal from one of the two VFO outputs into a square wave. U4D gates the VFO signal bursts into the clock input of the binary counter, U9. At the end of every burst, the final digit is held by the counter.

The falling edge of the timing signal triggers U10A, the first of three cascaded one-shots. The pulse at the output of U10B clocks the data from the counter into U8B. The pulse at the output of U11A resets U9.

If the number of pulses in each successive burst is equal (no VFO drift), U9 constantly counts the same number, and the output of U8B never changes. In practice, however, U8B constantly toggles between two states. The integrating circuit, R35-C36 (time constant = 6.5 minutes), converts the toggling into a slowly changing voltage. Varicaps D1 and D2 transform a few millivolts of change into ±1 or 2 Hz change of VFO frequency.

U13A, a high-input-impedance buffer, prevents the discharge of C36. U13B, a noninverting amplifier with a gain of 1.5, ensures compliance between the control-voltage range and the capacitance-per-volt ratio of the Varicaps (1 to 6 V for best performance). Network R36, R37, C37 and D7 establishes the initial dc voltage applied to the varicaps; the value is set by the C37-C36 voltage divider.

An infrared interrupter switch, U14, serves as sensor in the tuning-detector circuit. The slotted interrupter detects the movements of a serrated disc (see Figure 4) on the VFO reduction-drive shaft. U15A and B, a two-level limit comparator, converts the signal at its input into pulses. U16A produces trigger pulses for the one-shot, U11B, by detecting both leading and falling edges of the signal at its input. U11B is retriggerable—its Q' output stays low during manual tuning and for 3.6 seconds after tuning stops. Analog switch U12A disconnects

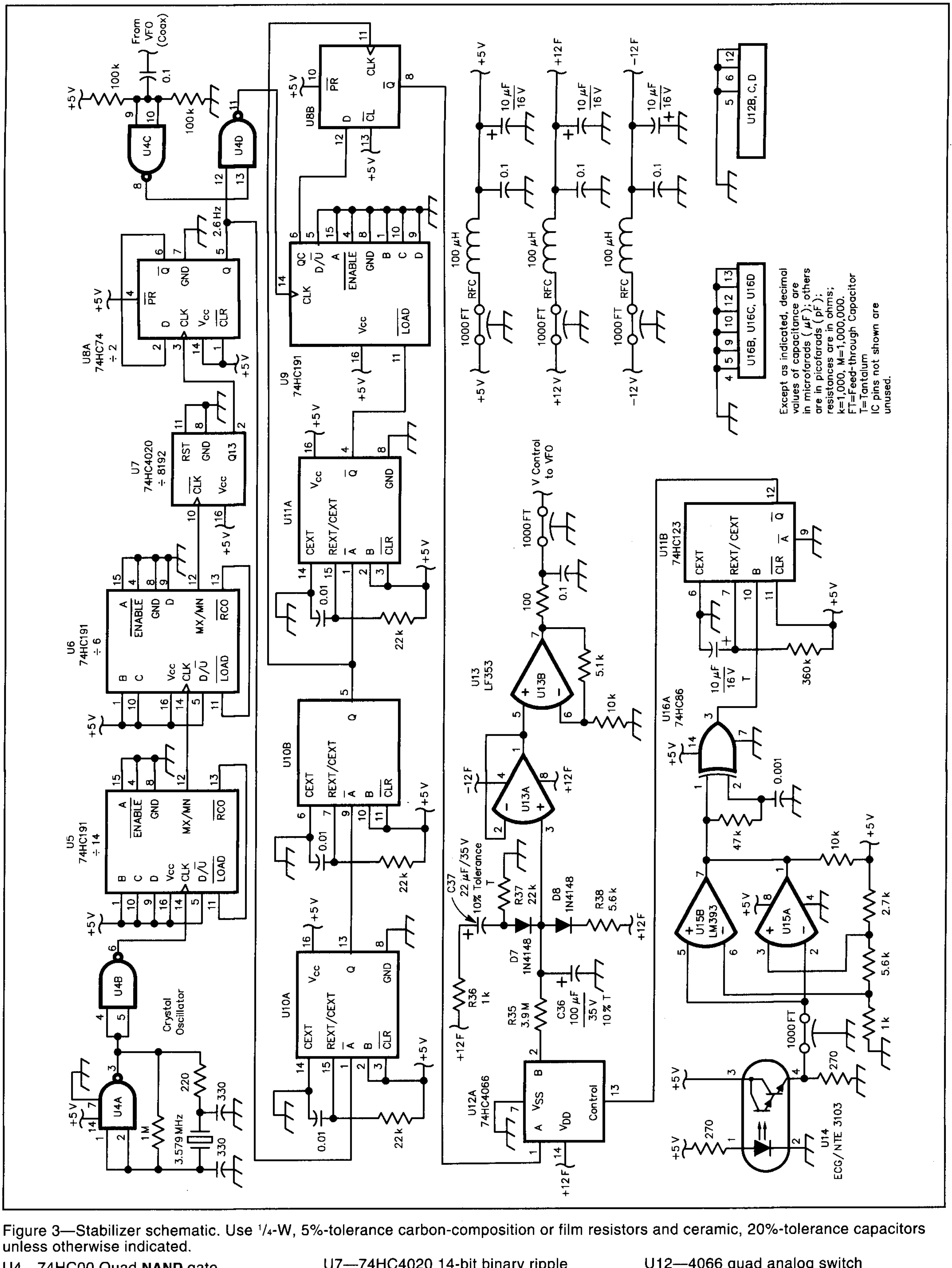

Figure 3—Stabilizer schematic. Use 1/4-W, 5%-tolerance carbon-composition or film resistors and ceramic, 20%-tolerance capacitors unless otherwise indicated.

U4—74HC00 Quad **NAND** gate
U5, U6, U9—74HC191 presettable 4-bit binary counter
U7—74HC4020 14-bit binary ripple counter
U8—74HC74 dual D flip-flop
U10, U11—Dual 74HC123 one-shot
U12—4066 quad analog switch
U14—ECG/NTE3103 optical interrupter (Darlington output, Allied, see Note 7)

C36 from the flip-flop during tuning, thus preserving the capacitor charge. This system does not provide for an RIT control.

Construction

The VFO and the stabilizer are in separate boxes. Mount components within the enclosures on the perf board's foil side. Make ground connections to the foil plane. Use Vector pins as terminal posts for the input and output signals.

The VFO box is a die-cast aluminum enclosure ($4^{11}/_{16} \times 3^{11}/_{16} \times 2^{1}/_{16}$ inches) to ensure mechanical rigidity. The two RF outputs exit the box via BNC connectors and coax. DC enters via feedthrough capacitors. Rigidly attach C2 to the enclosure wall. Cover L1 with a low-loss polystyrene Q dope and place it as far as possible from the ground plane and enclosure walls. The layout is not critical, but observe standard RF building methods: use short leads, dress them for minimum coupling and solder bypass capacitors directly to the ground plane close to the terminal they bypass.

The stabilizer is in a $5^{1}/_{2} \times 3 \times 1^{1}/_{4}$-inch LMB aluminum enclosure. Component placement and layout is not critical, but keep component leads short around the crystal oscillator. Use a BNC connector for the signal from the VFO module. Solder the ground pins of all ICs directly to the ground plane, and decouple each power-supply pin of ICs U4 through U9 to ground via a 0.1-µF capacitor. Route all dc voltages to the module via feedthrough capacitors to avoid RF leakage. Mount U14 so that the serrated disc is in the middle of the slot.

Mount C37 in a socket in case you need to adjust its value: For unknown or varying VFO drift direction, use a 22-µF capacitor to place the initial varicap control voltage at midrange ($V_c \approx 2.9$ V). Use 10-µF if VFO drift is predominantly negative ($V_c \approx 1.5$ V), and 33-µF if it's predominantly positive ($V_c \approx 4.0$ V).

Measurements

The VFO thermal drift without the stabilizer was under 800 Hz at room temperature (after 90 minutes) and under 1500 Hz when the ambient temperature was raised 20°C. There was no attempt to compensate for thermal drift.

With the frequency stabilizer connected, the thermal drift did not exceed 10 Hz at room temperature, 20 Hz when raised 20°C. In one of the experiments, power was on for several days, and drift was under 10 Hz at room temperature. Frequency lock is attained in less than 10 seconds after the power is switched on.

With the components shown in the schematic, the stabilizer can compensate for a maximum 1800-Hz drift with a 25°C temperature rise. To compensate for a greater frequency drift, select varicaps with higher diode capacitances; the frequency swing will increase from ±1 or 2 Hz to a higher value.

I designed a special device to measure VFO phase-noise performance for this project. A detailed description is beyond the scope of this article, but the method employs two frequency sources held in phase quadrature via a very narrow-band (5-Hz) PLL. Notes 5 and 6 outline the principles of this measurement.

Figure 5 and Table 1 show the phase-noise measurements. The SSB phase noise is simply 3 dB less than the measurements in the middle column.

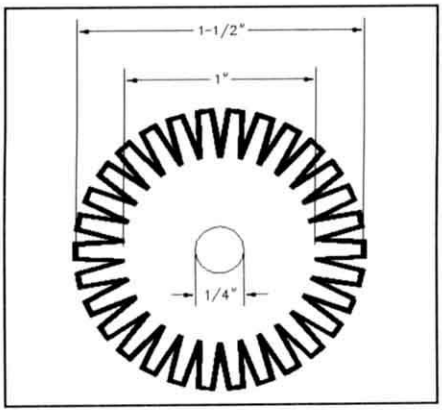

Figure 4—Mechanical details of interrupter wheel. Use a good reduction drive and make one tooth for every 20 to 40 Hz of frequency change. Use any rigid, opaque material.

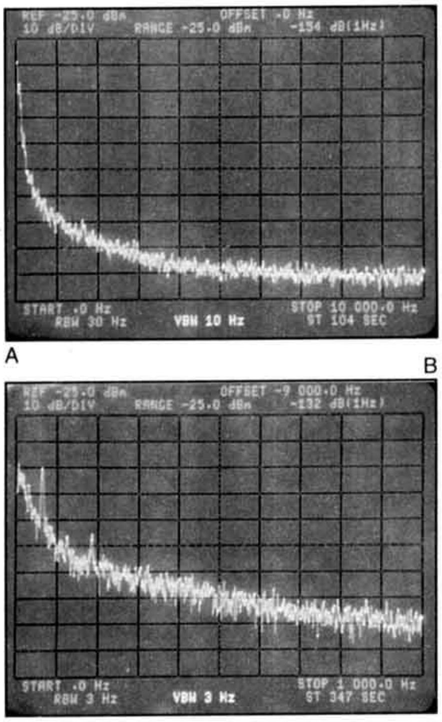

Figure 5—A shows phase-noise levels at offsets between 10 Hz and 10 kHz. At offsets beyond 10 kHz, the measurement is limited by the noise floor of the measurement fixture (–158 dBc/Hz).
B shows the phase-noise levels for offsets between 10 Hz and 1 kHz. Sixty hertz and a few harmonics thereof appear on the curve because the measurement fixture is not completely immune to such pick-up.

Table 1
Phase Noise versus Frequency Offset

Offset from Carrier (Hz)	*Phase Noise (dBc/Hz)*	*SSB Phase Noise (dBc/Hz)*
10	−74	−77
100	−101	−104
1k	−132	−135
5k	−151	−154
10k	−154	−157
100k	< −155	< −158

Summary

By following several design guidelines, it is possible to build a low-cost, easy-to-construct LC VFO with a very low level of phase noise.

The method shown makes the oscillator essentially drift-free, with very little phase noise, VFOs built with these techniques are viable in applications where low overall noise level and wide dynamic range is of great importance.

The technique can also spare VFO designers the drudgery of more conventional drift-compensating techniques.

Acknowledgments

My thanks to Alex Osipenko, UAØKBO, for the original ideas that prompted this project and to Colin Horrabin, G3SBI, for sending me Klaas Spaargaren's article from *RadCom* magazine.

Jacob holds an MSEE from the Civil Aviation Engineering Institute in Riga, Latvia. Since 1984, he has been employed at Philips Ultrasound, where he is involved in the design of ultrasound imaging systems. A radio amateur since 1986, Jacob holds an Advanced class license. His favorite amateur interest is high-performance receivers. You can reach Jacob at 1100 N Sunset Canyon Dr, Burbank, CA 91504.

Notes

[1]Wes Hayward, W7ZOI, "Measuring and Compensating Oscillator Frequency Drift," *QST*, Dec 1993, pp 37-41.

[2]Jacob Makhinson, N6NWP, "Designing and Building High-Performance Crystal Ladder Filters," *QEX*, Jan 1995, pp 3-17.

[3]Peter Chadwick, G3RZP, "Phase Noise Intermodulation and Dynamic Range," *Frequency Dividers and Synthesizers IC Handbook*, Plessey Semiconductors, 1988, p 151.

[4]Klaas Spaargaren, PAØKSB, "Technical Topics: Crystal-Stabilized VFO" *RadComm*, Jul 1973, pp 472-473. Comments followed in later "Technical Topics" columns. Also see, "Frequency Stabilization of L-C Oscillators," *QEX*, February 1996, pp 19-23.

[5]Ulrich Rohde, KA2WEU/DJ2LR, *Digital PLL Frequency Synthesizers* (Englewood Cliffs: Prentice-Hall, 1983) p 78.

[6]*The ARRL Handbook* (Newington: ARRL, 1995; Order no. 1735) pp 14.8-14.13; see the *ARRL Publications Catalog* elsewhere in this issue.

[7]Mouser Electronics, 2401 Hwy 287 N, Mansfield, TX 76063; tel 800-346-6873; e-mail: **sales@mouser.com**; Web **http://www.mouser.com**. Digi-Key Corporation, 701 Brooks Ave S, PO Box 677, Thief River Falls, MN 56701-0677; tel 800-344-4539 (800-DIGI-KEY); fax 218-681-3380; Web site: **http://www.digikey.com/**. Allied Electronics, 7410 Pebble Dr, Fort Worth, TX 76118; tel 800-433-5700; Web: **http://www.allied.avnet.com/**. Amidon, 3122 Alpine Ave, Santa Ana, CA 92799; tel 714-850-4660, fax 714-850-1163.