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The ARRL Experimenters' Exchange

In this second issue, *QEX* welcomes Mark Forbes, KC9C as a regular columnist to keep us abreast of new components of interest to Amateur Radio experimenters. As a research and development engineer, Mark sees most of the new components as they are introduced. If you become aware of a new component that Mark hasn't covered, you might drop him a line and give him what information you can dig up.

I'm seeing some good manuscripts on a variety of subjects, as you can tell from those in this issue. I'd like to try to stimulate prospective authors by tossing out a few ideas for articles for *QEX*.

Can someone write an article on designing power supplies with 3-terminal regulators? What types are available? What are the heat sinking requirements? Does anyone have experience with the new Intersil ICL7663/7664 CMOS Programmable Micropower Voltage Regulators?

Not too much has appeared in amateur literature concerning surface acoustic wave (SAW) filters. A practical design article on SAW filters would be useful.

There are a number of analog ICs that are approaching a complete receiver in one chip. An article examining these chips and their possible amateur applications would seem to be a good one.

Similarly, there are chips that are almost complete transmitters. An example is the Motorola MC1374 TV Modulator Circuit which was designed to generate a TV signal with sound for various TV games.

RFI is a particularly sore subject these days. Those experimenters who have tried to integrate a computer into their ham shacks are aware of the hash generated by digital equipment due to the fast rise times. What are the effective and economical precautions and remedies? How does one go about metal coating plastic cases, and is it effective? A good article on this subject would make a worthwhile contribution about now.

There has been an explosion of video equipment on the market for home video recording as well as some reasonably priced gear sold for plant and office security. While realizing that most ATV hardware will be homebrew or used/surplus variety, some of these new gadgets on the market should have an impact on some of the more sophisticated ATV systems. An example of an exciting new product is Hitachi's VK-C1000 tubless color video camera priced under $2000.

A quick scan of past Amateur Radio literature on direction finding might lead one to conclude that the state of the art involves wiring up discarded broom handles for 2-meter DF antennas. A good article on fixed and portable DF systems would be most welcome.

Many of the ICs on the market today have hidden attributes that you could pass along to your fellow experimenter in an article. As an example, it is possible that a stage in an analog IC designed as an audio oscillator might work in the rf region as well. Digital chips also have unadvertised features (and flaws) that could be documented in *QEX* by someone in the know.

The design of an uninterruptible power supply (UPS) for a repeater or home station would be a good topic for an article.

Packet radio is ripe for numerous articles. Local area network and internet protocols are now in the formative stages. Many of us could use a down-to-earth (non-math) article on error-correcting codes and how they might be applied to Amateur Radio hf and vhf packet links. A good, cheap, easily reproduced Bell 202-compatible modem is very much needed. This list could go on and on.

I probably missed some of the obvious experimental subjects of interest. Start your own list of needed projects and articles. Half of the battle is thinking of a topic and writing the first few words. The rest is down hill. - W4RI

Algorithmic State Machine for Remote Receiver Link System Controller

By Eric Smitt, K9ES*

As trustee for a repeater in central Massachusetts, I was asked to design a remote receiver link and a controller for all the hardware. Many ideas were researched. The least expensive and possibly the most reliable system proved to be an "Algorithmic State Machine," or ASM for short.

The task of a controller is to take specific control signals from the remote receiver and control the operation of a remote link transmitter. Many FCC rules governing this operation can be written into a flowchart form of a computer program. This flow chart, or algorithm, dictates when to turn the link transmitter on and when to shut it off. It generates identification at the proper time and controls the various audio paths within the link system. It keeps time on the transmitter, and in the case of a time out, turns the transmitter off. Finally, it can be remotely controlled for master override (presently only by local control at the remote receiver site).

A controller for this task could be approached from many angles - all the way from analog timers and TTL gates to a microprocessor such as a 6802. But I decided that a micro would be overkill, because no math was required, and the algorithmic state machine would serve us best. The unit described is our actual one which is in service on the Data General Radio Club repeater on 145.270 MHz. The unit is made from 74LS and 74S TTL and consists of 26 integrated circuts for the actual controller and a pair of dual op amps and analog CMOS switches for the audio circuitry. The PROMs are low cost 82S23 or 6330 devices. The total cost is much lower than a microprocessor, and the timing accuracy is magnitudes better than monostables or 555 timers.

Block Diagram

The algorithmic state machine is broken into basic units (see Fig. 1). The control sequencer is a pair of 74LS193 presettable up-down counters which are used to address the control program stored in PROM. The counter can be preset to a new number, or the present count can be increased by 1 to provide a new address. The decision whether to enter a new value or just increase the present value by 1 is a function of the algorithm and logic. The logic actually tests conditions and makes judgments on the results of the test.

The control program is written into a special memory, called a PROM. I selected a PROM with a field of 32 locations with 8 bits per location (32 x 8). The IC actually contains an array of 256 fusible links. Each link can be blown by a programming device. There are 5 input lines and 8 data output lines in each PROM, with a chip enable line. The input lines are called an address, and the output lines are the contents of the address. I used 2 PROMs for a 16-bit-wide control store and used 16 of the 32 possible addresses.

The next portion of the algorithmic state machine is the register which stores the data from the PROMs. This storage is necessary because the data will be changing during the period that the address lines change and when the output signals might glitch. The register stores the data once the PROM output is stable and holds the data stable during the period that the PROM address lines are changing. The register is also designed to drive the many control lines within the logic. I selected 74LS374 and 74S374 ICs as the 16-bit register. The upper 8 bits from the PROM go to the 74S374, and this register drives all the control lines. The lower 8 bits go to a 74LS374 register, with 3 bits feeding the test multiplexer (MUX), and 5 bits feeding the data input of the 74LS193 sequencers.

The final portion of the algorithmic state machine is the logic for the clock generation (see Fig. 2). Sixty-Hz ac is fed from the power transformer into a 7404 buffer and network. The output is a squared-off signal, high for 9.16 ms and low for 9.16 ms. This is fed into the clock inputs of a 7476 dual J-K flip flop. With the addition of a 7410 IC, a dual-phase clock is produced, with a frequency of 15 Hz. CLK-A feeds the sequencer, and CLK-B feeds the register. Additional hardware for the algorithmic state machine provides two timers

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and a cw generator. The first timer takes the 60-Hz clock and divides by 21,600. The second timer divides the 60 Hz by 72,000. Each timer is under direct control from bits in the algorithmic state machine, and each timer feeds a D-type flip flop which generates a signal to feed the algorithmic state machine test multiplexer. Each flip flop (flag) can be cleared by the control bits of the algorithmic state machine.

Cw Generator Sequencer

The cw generator is synchonous with the ASM because it is clocked by a phase-related clock of CLK-A. An 8-bit up counter, similar to the counter in the sequencer of the algorithmic state machine, addresses both a PROM and a MUX, similar to the test MUX in the ASM. Because cw information is serial in nature and because the PROM puts out 8 bits per addressed word, the MUX cycles through the output data from the PROM and provides a parallel-to-serial conversion. The output of the MUX drives a CMOS analog switch which places a sine-wave audio tone on the main audio line in the transmitter. The cw circuit gets enabled by a bit of the ASM and then gets triggered to start by the bit which places the transmitter on the air. Upon completion of the identification, a signal called CWDONE can be tested by the ASM. The completion signal comes from the up counters reaching a given state. This signal "$\overline{\text{FIN}}$" resets the 2 flags which stop the sequence clock to the cw generator and generates CWDONE. Cw time is set at 15 Hz, which works out to about 12 wpm.

Basic Timing of the ASM

The algorithmic state machine is clocked at 15 Hz. When CLK-A goes high, the control sequencer will either increment or load a new address. This will take a few hundred nanoseconds, and the new address will appear on the address lines to the PROMs. In less than 100 ns, the output of the PROMs will be stable data. 36.3 ms later, the register gets clocked, and the data will remain until the next CLK-B signal. The control sequencer $\overline{\text{COUNT UP}}$ input is affected only by the high-to-low transition of $\overline{\text{CLK-A AND TRUE}}$, but the $\overline{\text{LOAD}}$ input is affected by the entire period that $\overline{\text{CLK-A AND FALSE}}$ is low. The register is affected only by the low-to-high edge of CLK-B.

ASM Control-Bit Assignment

The following symbols are labels which describe the actual signals used in the circuit. A label XXX indicates that the true state will be logic 1. A label $\overline{\text{XXX}}$ indicates that the true state will be logic 0. This was not done to cause confusion but to save hardware. Logic 1 in TTL is any level between 4 and 5 volts, and logic 0 is any level below 1 volt. The following will describe the machine language of the program:

Bit 0	LINK	Enables PTT of 450 transmiter
Bit 1	$\overline{\text{2MA}}$	Feeds 2-meter audio to 450 transmitter
Bit 2	CW	Enables cw sequence when link is present
Bit 3	$\overline{\text{PL}}$	Feeds CTCSS encoder audio to 450 transmitter
Bit 4	$\overline{\text{ACT}}$	Allows 3-minute timeout counter to count
Bit 5	$\overline{\text{CACT}}$	Resets timeout flag
Bit 6	$\overline{\text{IACT}}$	Allows 10-minute i-d required counter to count
Bit 7	$\overline{\text{CIACT}}$	Resets cw time flag
Bits 8 - 10		Test condition select
Bits 11 - 15		New address if test result is false

The test-condition-select MUX receives 7 states from the logic of the ASM and the control bits for the selection. If ASM control program output lines 8, 9 and 10 have logic states 1, 1 and 0 respectively, the MUX selects input 6 and feeds the binary state of input 6 to the true and the reverse of input 6 to the false output. If input 6 has a logic 1 on it, the true output will have logic 1, and the false output will have logic 0. If the input 6 were logic 0, the false output would be logic 1, and the true output would be logic 0. Thus, a logic 0 input on a selected line will produce a false signal, and a logic 1 input on a selected line will produce a true signal. If the true signal is present, when CLK-A goes high, the control sequencer will increment its count. If the false signal is present, the control sequencer will be set to the count present on the new address field when CLK-A is high.

COR and Squelch-Tail Circuitry (Fig. 4)

The COR circuit uses a 74LS122 retriggerable monostable flip flop to generate a squelch tail upon loss for receiver COR. A variable length delay of 0.5 to 3 seconds allows the link to remain on the air for periods of time after the receiver has lost a signal. The link will pass the open-squelch noise during this short period, and the voter at the local repeater site can determine that the signal-to-noise ratio is 1.0 and not to select the link audio for repeating. The 74LS122 has 4 different inputs, and CLK-A retriggers the flip flop. The CTCSS decoder can feed a true input if PL is to be required at the remote receiver. The selection of this requirement will presently be done by a front-panel switch, but upon completion of a bi-directional link to the site, it will be done by the main repeater micro setting parameters in the link ASM. This is planned for the future, as one remote receiver is located at the repeater site of the Amherst, NH 145.490 group. Several other ideas will be studied, including repeater link up and 10-meter fm diversity reception.

Timers (Fig. 5)

The two timers are straight-forward dividers using 74LS92, 74LS90 and 74LS390 ICs. I designed a time out to occur if the link transmitter is on the air for longer than 3 minutes. The cw i-d time is designed to occur at least every 10 minutes. Because the

control bits from the ASM feed the timer, I decided to use the reset inputs as enables. If the bit is high, the counter is reset to zero. When the bit goes low, the counter is enabled, and in the case of the 3-minute counter, after 10,800 input counts, the output will go high. This is fed into the clock input of a 74LS74 counter. The D input is held low. Upon the rising edge of the output of the counter string, the $\overline{Q}$ output of the 74LS74 will go high. This state will remain until the ASM outputs a random control signal called $\overline{CACT}$, which will reset the time-out flag. The Q output is called $\overline{TIMEOUT}$ and feeds input 6 of the test MUX. The ASM can then test the state of the time-out flip flop as well as reset the flag.

The second timer determines i-d time and is a chain which divides the 60-Hz input by 36,000 counts as well as setting the CW TIME flag. This is also a 74LS74, and the $\overline{Q}$ output is called CW TIME and gets fed to input 5 of the test MUX. The signal $\overline{CIACT}$ from the ASM resets this flag.

Audio Path Circuitry (Fig. 7)

The audio circuitry uses two dual op amps (747) in a single-voltage supply and a pair of Harris HI-200 CMOS analog switches to control the audio path within the unit. It was determined that we would transmit a CTCSS tone on the 450 transmitter whenever the audio being passed over the link should be fed into the voting system and shut off the PL during periods when the link was identifying in cw. I use the CMOS analog switches to select audio feeds to a 3-input mixer which drives the mike line of the 450 transmitter.

It was determined that the audio on the cw link would come from a sine-wave source. This would prevent excessive sideband products from being generated by the 450 transmitter. The 2-meter receiver audio de-emphasis was removed, and the 450 transmitter pre-emphasis was removed so that our voting system could look at unprocessed audio. To put a square-wave cw source on would definitely over-deviate the transmitter. A 555 oscillator was out of the question. One of the dual op amps is used as a twin-T oscillator. This puts out a sine wave with less than 4% total harmonic distortion. The frequency of the audio is a function of both resistor and capacitor values in the feedback loop between U-27 pins 1 and 12. I selected mylar capacitors as they do not seem to drift with temperature. I measured a dozen values at 0.0047 µF with a digital capacitance meter and selected two values which were closest to each other and half the value of a 0.01-µF capacitor measured with the same meter. This work reduces total distortion on the sine-wave output. Resistors should be 5% tolerance or better. The frequency of the oscillator came out at 950 Hz.

The second half of the op amp is used to establish output level for the audio mixer. U-28 is another 747 dual op amp. Half of the IC is a buffer stage for the mixer, and the other half is the audio mixer. Between the input stages of the mixer and their sources are the CMOS analog switches. They provide high isolation when open but add only 50 ohms resistance to the closed path. A logic low on the control line will close the switch, and a logic high will open the switch. The closing and opening time is less than 50 ns. The audio mixer is a straight-forward analog adder, providing an output equal to the sum of the inputs. The total gain of one input versus the output is one, and the output impedance is 10 kΩ. Level adjustment for the cw level, the 2-meter audio level and the output feed to the 450 mike line is provided. The high-frequency 3-dB roll off of this circuit is near 45 kHz, as measured in the lab.

Power Supply and Link Construction (Figs.7&8)

The power supply requirements are simplified by use of 3-terminal regulators wherever possible. A 7812 provides +12 V for the analog at up to 1 A. A 7912 provides -12 V for the CMOS analog switches, and a 323 provides +5 V at 3 A for all TTL circuitry. Derived from the +12 is a +8-V regulator (7808) for the Communications Specialist CTCSS logic. I selected the IC-701 microcircuit from Comm Spec and built it into the logic to provide CTCSS encoding and decoding. I feel that this unit is the best value for CTCSS work (Communications Specialist, 426 W Taft Ave., Orange, CA 92667). A separate power supply for +13.8 V at 10 A is designed around the LM350 regulator and a pair of 2N3055 pass transistors. This feeds the 2-meter receiver and 450 transmitter. I chose Spectrum Communications gear for both the link 2-meter receiver and the link transmitter. The total package is housed in an aluminum chassis measuring 17 x 13 x 4 inches. A piece of G-10 epoxy board is placed on the chassis bottom, and the 3 units are housed in individual boxes made from the G-10. All heat generation is conducted through heat sinks to have forced-air cooling provided by fans. The power suppply regulators are all mounted on a large heat sink external to the box. The ac input for the unit has EMI filtering provided by a Corcom EMI filter and a low-pass vhf filter made by ferrite beads and bypass capacitors.

All connections for control and power go through feed-through capacitors, and all internal rf connections go through BNC jacks. Audio lines go through RCA audio jacks.

Wherever possible, shielding is used. Where air flow is required, copper screen is soldered to the G-10 epoxy. Rf integrity is mandatory, because this location will have high rf fields present. I did not dwell on construction for the logic. This is because I used a general-purpose wire-wrap board to construct the ASM. The layout which I used in the wire-wrap version is shown in Figs. 9 and 10. At some later date, if there is sufficient interest, an etched-circuit board will be made.

But, for a single project, wire wrap is the best method. I soldered resistors and capacitors to the board but put sockets in for all the ICs.

Troubleshooting

Refer to the microsequencer program for the next step in troubleshooting. The numbers referred to are the octal addresses for the control sequencer. You can monitor the address with a logic analyzer or set of LEDs connected to the address. If you use LEDs, do not overload the address lines. Use a 74LS04 buffer to drive the LED from +5 V, limiting LED current with a 1-kΩ resistor. Bench testing the algorithmic state machine could prove interesting. Pressing the reset switch and holding it down should stop the clock and place all zeros on the address lines to the ASM PROMs.

When the switch is removed, the address should loop from 1 to 5 to 1. If nothing is done, it will remain in this loop for 10 minutes and then jump from 5 to 6, set the cw flag and jump back to 1. It will continue to do this loop forever, waiting for a signal called COR. Then it should jump from 1 to 2. It will now start a cw message and go from 2 to 3 to 15. It will loop from 15 to 16 and stay in 16 until the cw message is done. Then it will go from 16 to 17 to 4. At address 4, it will loop back to 2 to 3 to 4 and back to 2 then continue this loop until 3 minutes are up. It will jump from 2 to 7, turn on the cw i-d, jump to 13 and stay at 13 until the cw i-d is done. Once it is completed, it will go from 14 to 11, turn off the link transmitter and stay in 11 until the COR signal has cleared. This is the completion of the time-out sequence. When the COR has dropped, the address will go to 12, enable the cw i-d and jump to 1 waiting for a COR to occur in the first loop described. After timing out, it will i-d immediately upon receiving the COR signal.

Summary

The algorithmic state machine can provide a lot of power for a simple or complex control project. All things considered, the algorithmic state machine is the best choice for this application and can be easily expanded for future applications. An additional PROM can provide 8 more control functions or allow another test MUX to be selected. A page-select function can expand the addressing capabilities by banking the program in pages of 32 instructions and using a *select* MUX to choose which page of PROMs will be selected. The real power is almost unlimited, and the construction is simple.

Determine from your needs whether the ASM is a better solution than a 6802, 8085 or other micro. If you do not need the heavy arithmetic power of a micro, the ASM may be for you. Steps to use for the design of the ASM are easily understood.

1. Write down all control signals (inputs and outputs) to the hardware that you wish to control.

2. Prepare a simple flow chart representing the steps that you want to use to control the hardware. Include any tests which are to be carried out on various conditions within the hardware. Label each major step (a step is a unit of time wherein all of the control functions are carried out at the exact time or at the same clock tick).

3. Fill in the jumping addresses from the test results.

4. Label all the control signals out and assign a bit position for each control signal in the control word.

5. Make a truth table of all the bits for each word.

6. Program the PROMs, construct the ASM and have fun! □ *Program and Figs.* →

Learning

IEEE Computer Society Tutorials

On March 22-26, 1982 the Orlando Marriott Inn in Orlando, Florida will be the site of a solid week of tutorials on a variety of subjects. They include VLSI design, microprocessor interfacing techniques, graphis and data communications. Inquire Tutorial Week East 82, P.O. Box 639, Silver Spring, MD 20901, 301-589-3386.

Encyclopedia of Integrated Circuits

That's the title of a handbook of reference data by Walter Buchsbaum. It is $19.95 plus postage and handling from Prentice-Hall, Englewood Cliffs, NJ 07632.

Southeast Computer Group Net

W4NNO is net control for this net which meets at 1300 Eastern time on Saturdays and Sundays on 7230 kHz, and 2000 Wednesdays on 3905 kHz. For a sample newsletter, send an s.a.s.e. to Don Johnson, WA4ZMR, Rt. 1, Box 74, Thonotosassa, FL 33592.

Epson Printer Newsletter

Epson Information Exchange is published by Frank Barden for users of the popular MX-series printers. It's $12.00 per year from 136 Candlewick Dr., Wendell, NC 27609.

Remote Link Microsequencer Program

Loc	Octal	Hex	Random Field	Test	New Address
00	055001	5A 01	$\overline{CACT}$,$\overline{CIACT}$	TRUE	CONT
01	056500	5D 45	$\overline{IACT}$	COR	05
02	102707	85 C7	LINK,$\overline{2MA}$,$\overline{PL}$,ACT,$\overline{IACT}$	$\overline{TIMEOUT}$	07
03	102615	85 8D	LINK,$\overline{2MA}$,$\overline{PL}$,$\overline{ACT}$,$\overline{IACT}$	CWDONE	15
04	102542	85 62	LINK,$\overline{2MA}$,$\overline{PL}$,$\overline{ACT}$,IACT	$\overline{COR}$	02
05	054641	59 A1	$\overline{IACT}$,$\overline{CACT}$	CWTIME	01
06	067041	6E 21	CW,$\overline{CIACT}$	FALSE	01
07	175213	FA 88	LINK,CW,$\overline{CACT}$,$\overline{CIACT}$	CWDONE	13
10	155213	DA 8B	LINK,$\overline{CACT}$,$\overline{CIACT}$	CWDONE	13
11	055151	5A 69	$\overline{CACT}$,$\overline{CIACT}$	$\overline{COR}$	11
12	077441	7F 21	CW	FALSE	01
13	155213	DA 89	LINK,$\overline{CACT}$,$\overline{CIACT}$	CWDONE	13
14	057451	5F 29		FALSE	11
15	163016	E6 0E	LINK,CW,$\overline{ACT}$,$\overline{CIACT}$	TRUE	CONT
16	153216	D6 8E	LINK,$\overline{ACT}$,$\overline{CIACT}$	CWDONE	16
17	102444	85 24	LINK,$\overline{2MA}$,$\overline{PL}$,$\overline{ACT}$,$\overline{IACT}$	FALSE	04

10	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
LINK	$\overline{2MA}$	CW	$\overline{PL}$	$\overline{ACT}$	$\overline{CACT}$	$\overline{IACT}$	$\overline{CIACT}$	TEST			NEW ADDRESS				

0	TRUE	ALWAYS CONTINUE
1	FALSE	ALWAYS JUMP TO NEW ADDRESS
2	COR	CONTINUE IF 2 METER COR PRESENT
3	COR(BAR)	JUMP TO NEW ADDRESS IF 2 METER COR PRESENT
4	CWDONE	CONTINUE IF CW ID COMPLETED
5	CWTIME	CONTINUE IF ID TIME REQUIRED
6	TIMEOUT(BAR)	JUMP IF LINK TRANSMITTER TIMED OUT
7	UNUSED	

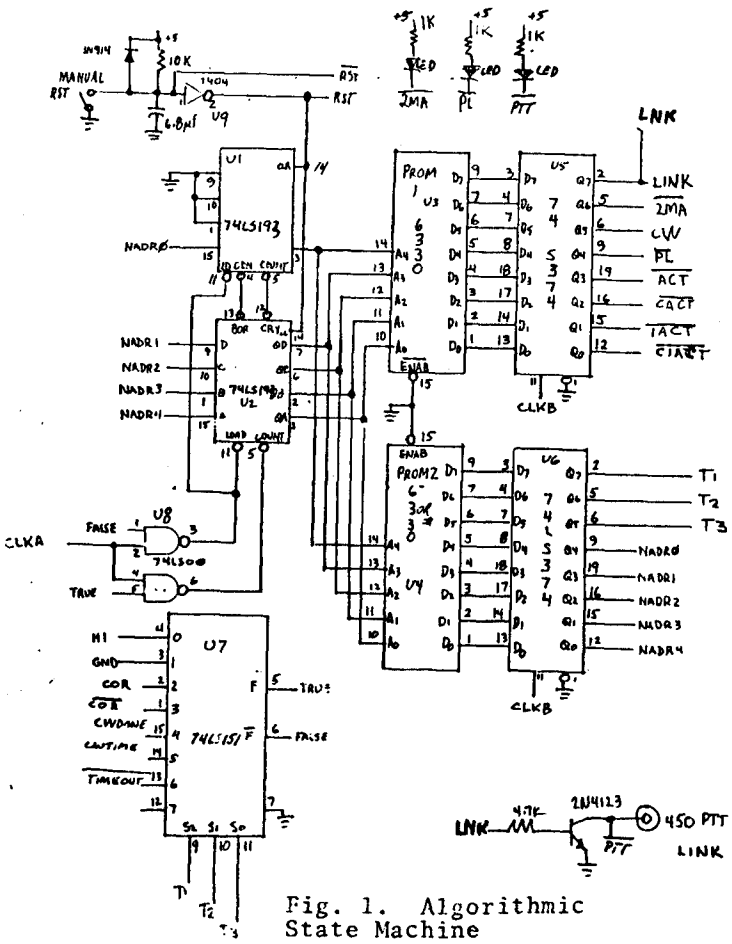

Fig. 1. Algorithmic State Machine

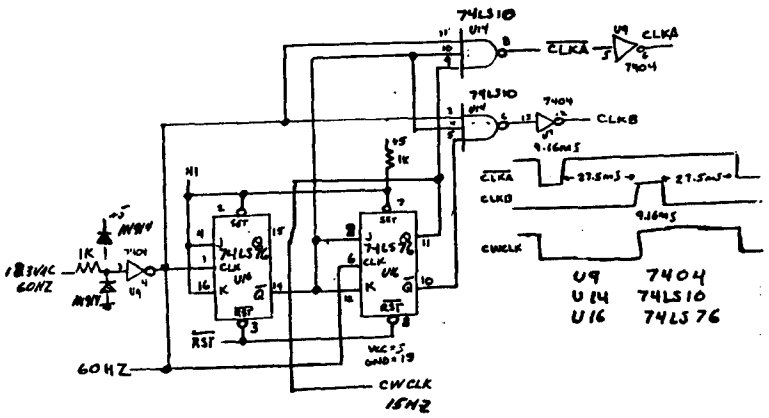

Fig. 2. Basic Clock Generation

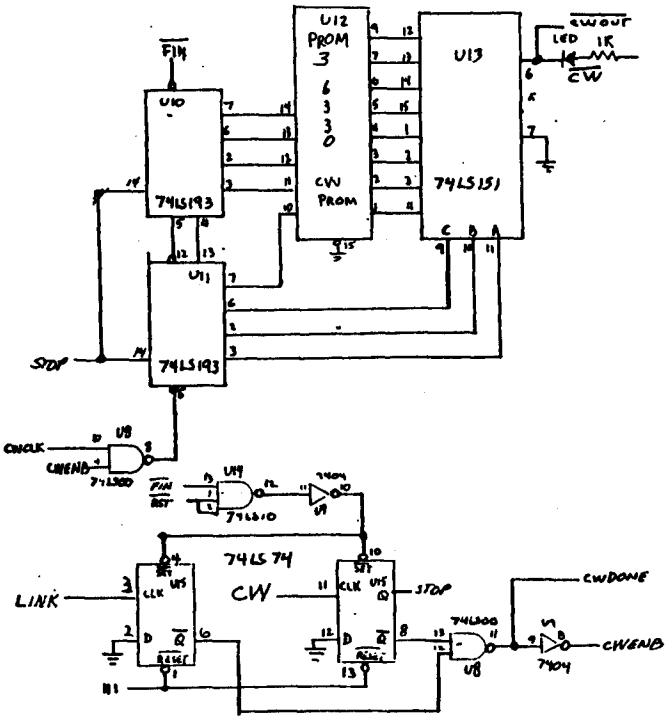

Fig. 3. Cw Generator Sequencer

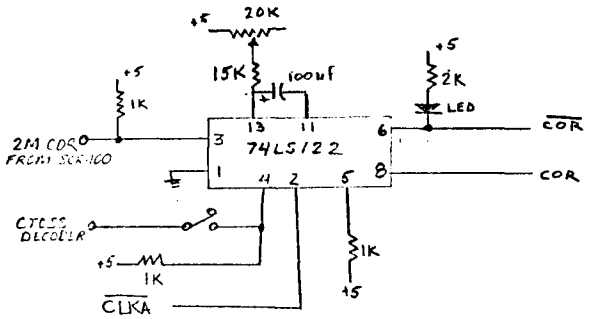

Fig. 4. COR and Squelch-Tail Circuitry

FIGURE 5 EVENT TIMER CHAINS

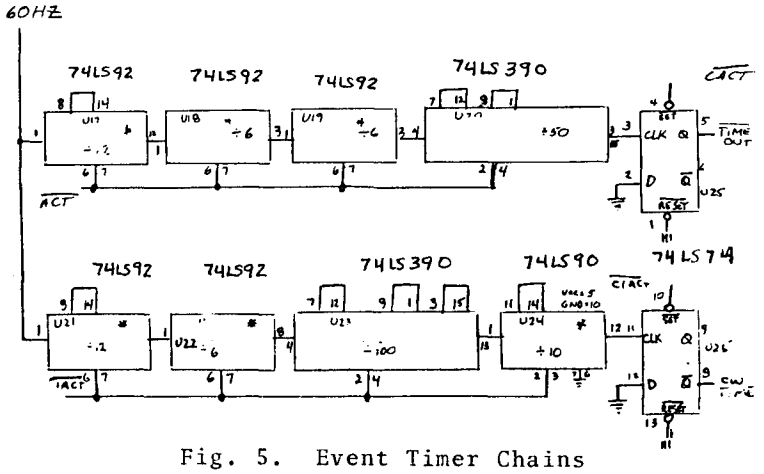

Fig. 5. Event Timer Chains

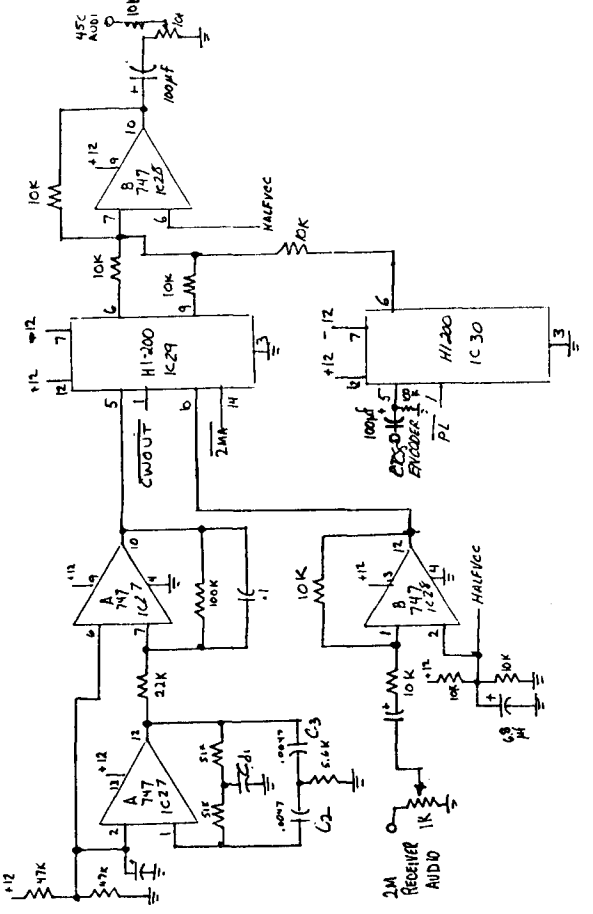

Fig. 6. Audio Circuitry

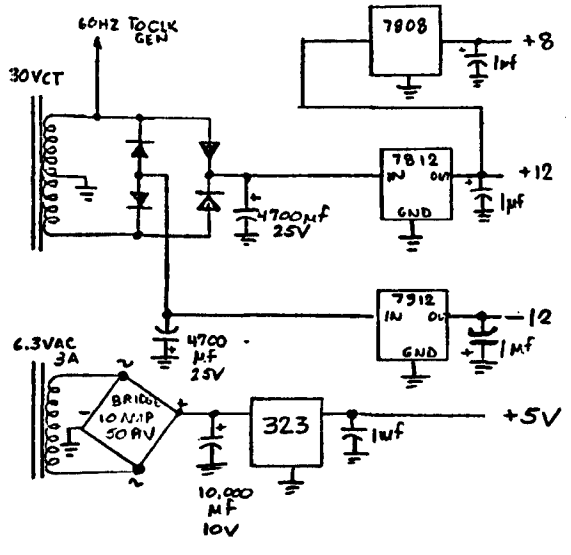

Fig. 7. Power Supply to ASM

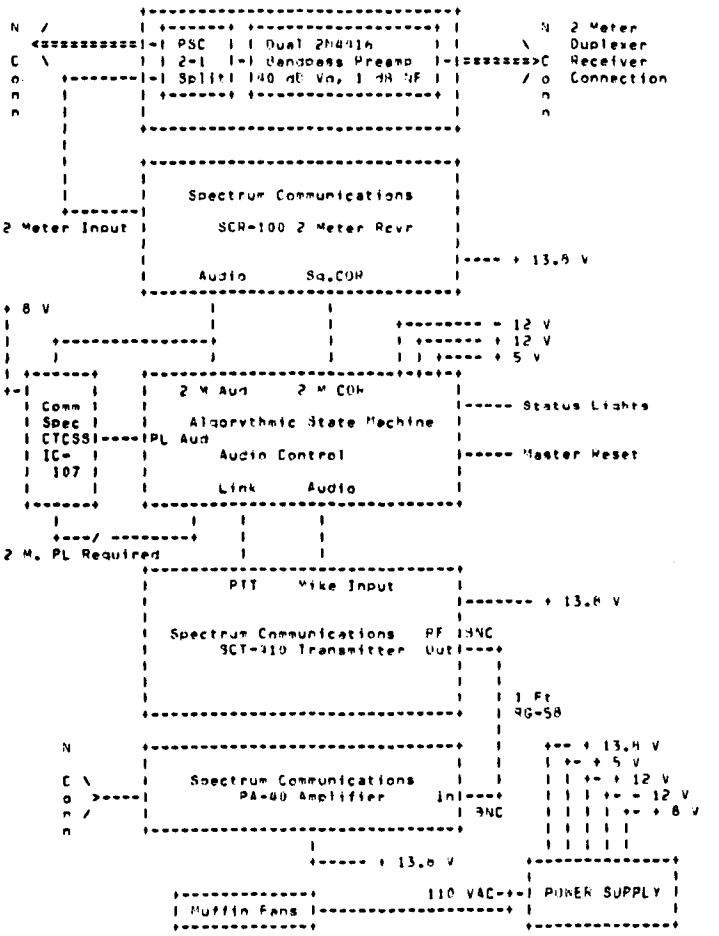

Fig. 8. Total Remote Receiver Link

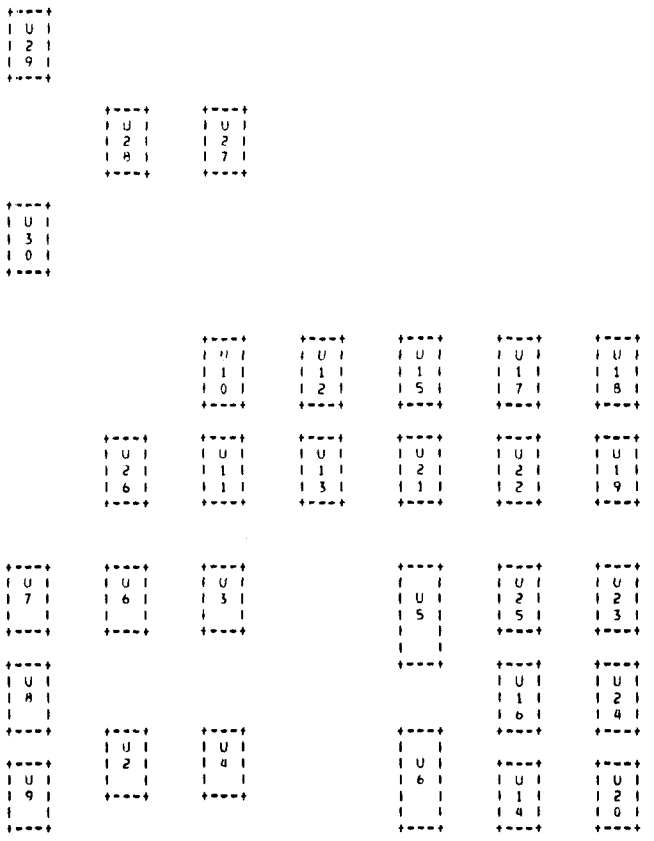

Fig. 9. Layout of ASM Showing IC Numbers

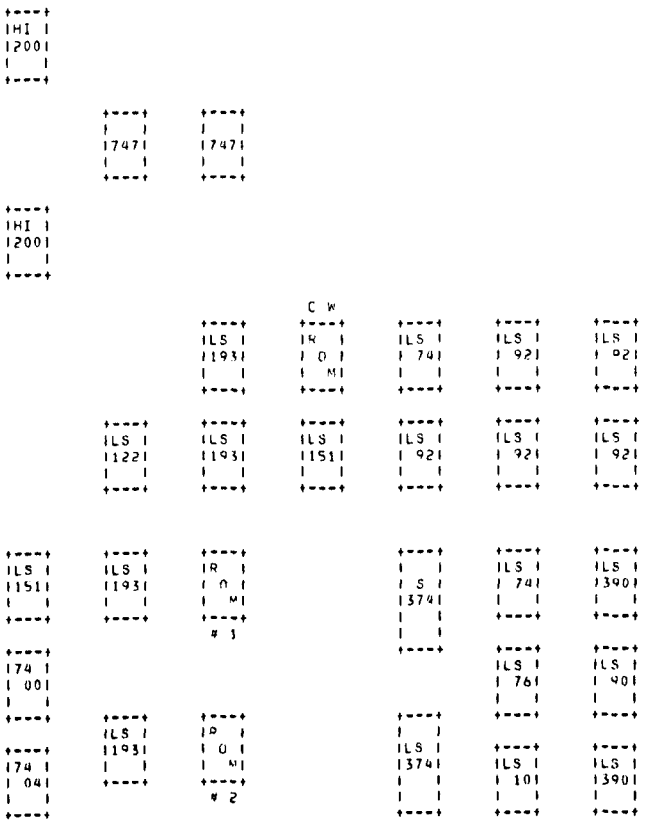

Fig. 10. Layout of ASM Showing IC Types

Data Communications

Conducted by
David W. Borden, K8MMO*

The Line Interface Program (LIP) is the heart of the software running on the VADCG Terminal Node Controller (TNC). This program is 2k in length, fitting in two 2708 PROMs. It does the work of making packets, feeding the 8273 Protocol Controller Chip as required. Written by Doug Lockhart, VE7APU, it is used throughout Canada and the United States by packeteers. This month we will begin to examine this program and how it works. The analysis is quite lengthy and will continue in the next column as required.

The LIP works with two buffers which will be examined closely later. The program works with the circular terminal buffer (also called the transmit buffer), removing outgoing data from it and transmitting it out the modem (and rf transmitter). It works with the circular line buffer (also called the receive buffer), taking in data from the modem (and rf receiver) and putting it in the buffer for the Termianl Interface Program (TIP) to process. It handles all the protocol on the link, recovers from detected errors, times out where required and deals with addressing (both for terminal-to-terminal and repeater operations) needs. Tailored to the needs of Amateur Radio, it controls the link in half-duplex (also called two-way alternate) mode by switching between transmit and receive when necessary. It does not change unless bugs are detected or a major protocol change is required (for instance, a change of the addressing scheme). Every end user employs the same LIP software.

It should first be noted that in the VADCG system, two features of the 8273 chip are used which affect the end result

*Route 2, Box 233B, Sterling, VA 22170, 703-450-5284.

(continued on page 16)

Computer Simulation of a Half-Wave Filter

By Bill K. Imamura, JA6GW*

When evaluating the harmonic suppression capability of a filter network, in almost all cases, the attenuation characteristic of the network when terminated into a pure resistive impedance with the value of unity (normalized) is considered. It can be misleading, if not incorrect.

The input impedance of an actual load, such as an antenna, can be 52 ohms on the fundamental frequency. On the harmonics, however, it is almost impractical to expect that the antenna shows the same unity impedance. A twenty-meter beam can hardly show an SWR of 1:1 on ten meters, and yet the second harmonic of a twenty-meter wave is on ten meters.

It has been brought to my attention that the effect of a non-resistive or a reactive load should be contemplated. This article presents the results of my study on the insertion loss of a half-wave filter terminated with a non-resistive load on harmonic frequencies.

Input Impedance of Transmission Line on Harmonic Frequency

The impedance of an antenna on harmonic frequencies can hardly be unity; that is, the transmission line is not flat, and some amount of SWR will result.

Fig. 1 illustrates the impedance circle for an SWR of 2:1 on a Smith chart. The circle intersects the real axis at R=2.0 and it is the vector locus of the input impedance of the transmission line. The coordinate at a certain point located on the circle gives the complex impedance at the corresponding point along the line.

Mr. K. Kajii, JA1FG, wrote concerning how to calculate values of impedance on an SWR circle in his excellent article.[1] Data for the study here was, in large part, derived from his article. Results of computer calculation showing the complex impedance at the typical twelve points on the SWR circle are in Fig. 2.

Effect of Reactive Load

An FT 901 transceiver here was tuned on ten meters and connected to a Mosley CL 203 twenty-meter beam. The indication of the SWR meter was around 5:1. A load which shows an SWR of 5:1 should be dealt with first.

Here is a program for the computation of the insertion loss of a half-wave filter. It is straight forward, and simple FORTRAN is used. I don't think that any explanation is necessary.

Data for the SWR of 5:1 were put into a computer. Results for the second harmonic are plotted as shown in Fig. 3.

It is well known that the theoretical attenuation or the attenuation when terminated into unity load is 58 dB. A noticeable dip appeared on the curve for the SWR of 5:1. The worst-case insertion loss is only 36 dB. Good harmonic suppression of 68 dB, however, can be expected when the transmission line length is optimum or at point 4-5 on the circle.

In Fig. 4 is the plot for the SWR of 2:1. The suppression tends to be uniform at lower SWR. If the SWR were to increase to 10:1, the worst-case suppression would be as low as 24 dB.

Source Impedance

The computation was executed on the basis that the source impedance is purely resistive and that the value is unity.

I have, however, no definite idea on the exact value of output impedance of the signal source which is the FT 901 on the second harmonic frequency. A vacuum tube final with a π tank circuit seems to have low output impedance on harmonic frequencies because it has a shunt capacitor at its output port.

Fig. 5 shows the results of computation for zero source impedance. Much more distorted curves were plotted.

Final Comments

It should be pointed out that the harmonic suppression of a half-wave filter is the function of the transmission line length. Ten to 20 dB of harmonic suppression is gained or lost depending on line length. □

[1] *Ham Journal* (published in Japan), spring issue.

*2-2-37 Hikari-ga-oka, Fukuoka City, Japan 816

```
ISN    STNO.   SOURCE STATEMENT

       C   T NETWORK INPUT IMPEDANCE AND INSERTION LOSS
       C
 1           INTEGER DEG, DEGREE
 2           COMPLEX XXC,XXL,ZZ1,ZZ2,ZZ3,UNIT,XXC2,ZZIN,ZZ4,ZZ5,ZZ6,ZZOUT
 3           DIMENSION Q0(4), R(12), X(12), DEG(12)
 4           DATA Q0/1.,2.,4.,10./
       C
 5           DO 40 M=1,6
 6           READ(9,110) SWR
 7         110 FORMAT(F3.0)
 8           READ(9,120) (DEG(K),K=1,12)
 9         120 FORMAT(12(I4,1X))
10           READ(9,130) (R(K),K=1,12)
11         130 FORMAT(6(F7.3,1X))
12           READ(9,140) (X(K),K=1,12)
13         140 FORMAT(6(F7.3,1X))
       C
14           WRITE(6,150) SWR,(R(MM),MM=1,12), (X(NN),NN=1,12)
15         150 FORMAT(1H ,10X,'LOAD IMPEDANCE',10X,'SWR=',F5.1//
          +11X,'R',5X,12F9.3/11X,'X',5X,12F9.3///)
       C
16           DO 10 I=1,4
17           Q=Q0(I)
18           XC=(1.+Q**2)/Q/2.
19           XL=Q
20           WRITE(6,700) SWR, Q
21         700 FORMAT(1H ,15X,'SWR=',F3.0,10X,'Q=',F3.0/)
22           WRITE(6,500) XC, XL, Q
23         500 FORMAT(1H ,10X,3HXC=,F5.2,15X,3HXL=,F5.2,15X,2HQ=,F4.1/)
24           WRITE(6,100)
25         100 FORMAT(1H ,10X,1HN,15X,4HLOAD,26X,'Z-IN (1ST STAGE)',12X,
          +'Z-IN (2ND STAGE)',12X,'INSERTION LOSS'/)
       C
26           DO 20 J=1,12
27           DEGREE=DEG(J)
28           WRITE(6,600) DEGREE
29         600 FORMAT(1HO,15X,I4,' DEG')
30           RO=R(J)
31           XO=X(J)
32           ZZOUT=CMPLX(RO,XO)
33           ZOUT=CABS(ZZOUT)
       C
34           DO 30 N=1,5
35           XL=Q
36           XL=XL*FLOAT(N)
37           XXL=CMPLX(0.,XL)
38           XC=(1.+Q**2)/Q/2.
39           XC=XC/FLOAT(N)
40           XXC=CMPLX(0.,-XC)
       C
41           ZZ1=ZZOUT+XXL
42           ZZ2=(ZZ1*XXC)/(ZZ1+XXC)
43           ZZ3=ZZ2+XXL
44           ZZ4=ZZ3+XXL
45           ZZ5=(ZZ4*XXC)/(ZZ4+XXC)
46           ZZIN=ZZ5+XXL
47           ZIN=CABS(ZZIN)
```



```
ISN    STNO.   SOURCE STATEMENT

48           RIN=REAL(ZZIN)
49           XIN=AIMAG(ZZIN)
       C
50           P1=RO/((1.+RO)**2+XO**2)
51           P2=RIN/((1.+RIN)**2+XIN**2)
52           DB=10.*ALOG(P2/P1)
53           WRITE(6,200) N, ZZOUT, ZZ3, ZZIN, DB
54         200 FORMAT(1H ,10X,I1,10X,3(2F10.3,10X),F10.3)
55          30 CONTINUE
56          20 CONTINUE
57           WRITE(6,400)
58         400 FORMAT(1H ,//)
59          10 CONTINUE
60           WRITE(6,900)
61         900 FORMAT(1H1)
62          40 CONTINUE
63           STOP
64           END
```

LMAD IMPEDANCE SWR= 2.0

R	0.500	0.526	0.615	0.800	1.143	1.665	2.000	1.665	1.143	0.800	0.615	0.526
X	0.000	-0.197	-0.400	-0.600	-0.742	-0.625	0.000	0.625	0.742	0.600	0.400	0.197

SWR= 2. Q= 1.

XC= 1.00 XL= 1.00 W= 1.0

N	LMAD		Z-IN (1ST STAGE)		Z-IN (2ND STAGE)		INSERTION LOSS
	-180 DEG						
1	0.500	0.000	2.000	0.000	0.500	0.000	0.000
2	0.500	0.000	0.050	1.350	0.002	1.412	-60.707
3	0.500	0.000	0.008	2.626	0.000	2.646	-109.919
4	0.500	0.000	0.002	3.734	0.000	3.742	-141.288
5	0.500	0.000	0.000	4.792	0.000	4.796	-164.747
	-150 DEG						
1	0.526	-0.197	1.067	0.624	0.526	-0.197	-0.000
2	0.526	-0.197	0.067	1.335	0.002	1.412	-57.735
3	0.526	-0.197	0.009	2.624	0.000	2.646	-107.963
4	0.526	-0.197	0.003	3.733	0.000	3.742	-139.739
5	0.526	-0.197	0.001	4.791	0.000	4.796	-163.421
	-120 DEG						
1	0.615	-0.400	1.143	0.743	0.615	-0.400	0.000
2	0.615	-0.400	0.097	1.327	0.003	1.412	-53.947
3	0.615	-0.400	0.012	2.621	0.000	2.646	-104.940
4	0.615	-0.400	0.003	3.732	0.000	3.742	-137.111
5	0.615	-0.400	0.001	4.791	0.000	4.796	-161.018
	-90 DEG						
1	0.800	-0.600	0.800	0.600	0.800	-0.600	0.000
2	0.800	-0.600	0.138	1.345	0.004	1.412	-50.562
3	0.800	-0.600	0.018	2.620	0.000	2.646	-101.148
4	0.800	-0.600	0.005	3.731	0.000	3.742	-133.544
5	0.800	-0.600	0.002	4.791	0.000	4.796	-157.623
	-60 DEG						
1	1.143	-0.742	0.616	0.400	1.143	-0.742	-0.000
2	1.143	-0.742	0.152	1.399	0.005	1.414	-49.998
3	1.143	-0.742	0.025	2.624	0.000	2.646	-97.797
4	1.143	-0.742	0.007	3.732	0.000	3.742	-129.780
5	1.143	-0.742	0.003	4.791	0.000	4.796	-153.775
	-30 DEG						
1	1.665	-0.625	0.526	0.198	1.665	-0.625	0.000
2	1.665	-0.625	0.118	1.438	0.003	1.415	-52.810
3	1.665	-0.625	0.027	2.634	0.000	2.646	-97.330
4	1.665	-0.625	0.008	3.734	0.000	3.742	-127.937
5	1.665	-0.625	0.003	4.792	0.000	4.796	-151.295
	0 DEG						
1	2.000	0.000	0.500	0.000	2.000	0.000	0.000
2	2.000	0.000	0.080	1.440	0.002	1.415	-56.664
3	2.000	0.000	0.020	2.640	0.000	2.646	-100.226
4	2.000	0.000	0.007	3.737	0.000	3.742	-129.762
5	2.000	0.000	0.003	4.793	0.000	4.796	-152.379
1	1.665	0.625	0.526	-0.198	1.665	0.625	0.000
2	1.665	0.625	0.057	1.427	0.002	1.415	-59.934
3	1.665	0.625	0.014	2.640	0.000	2.646	-104.084
4	1.665	0.625	0.005	3.738	0.000	3.742	-133.528
5	1.665	0.625	0.002	4.793	0.000	4.796	-155.961
	30 DEG						
1	1.143	0.742	0.616	-0.400	1.143	0.742	0.000
2	1.143	0.742	0.045	1.411	0.001	1.414	-62.177
3	1.143	0.742	0.010	2.637	0.000	2.646	-107.324
4	1.143	0.742	0.003	3.737	0.000	3.742	-137.093
5	1.143	0.742	0.001	4.793	0.000	4.796	-159.666
	90 DEG						
1	0.800	0.600	0.800	-0.600	0.800	0.600	0.000
2	0.800	0.600	0.040	1.396	0.001	1.414	-63.368
3	0.800	0.600	0.008	2.635	0.000	2.646	-109.546
4	0.800	0.600	0.003	3.736	0.000	3.742	-139.720
5	0.800	0.600	0.001	4.793	0.000	4.796	-162.514
	120 DEG						
1	0.615	0.400	1.143	-0.743	0.615	0.400	0.000
2	0.615	0.400	0.039	1.381	0.001	1.413	-63.526
3	0.615	0.400	0.007	2.632	0.000	2.646	-110.711
4	0.615	0.400	0.002	3.735	0.000	3.742	-141.288
5	0.615	0.400	0.000	4.792	0.000	4.796	-164.308
	150 DEG						
1	0.526	0.197	1.067	-0.624	0.526	0.197	-0.000
2	0.526	0.197	0.042	1.366	0.001	1.413	-62.641
3	0.526	0.197	0.007	2.629	0.000	2.646	-110.832
4	0.526	0.197	0.002	3.734	0.000	3.742	-141.806
5	0.526	0.197	0.000	4.792	0.000	4.796	-165.045

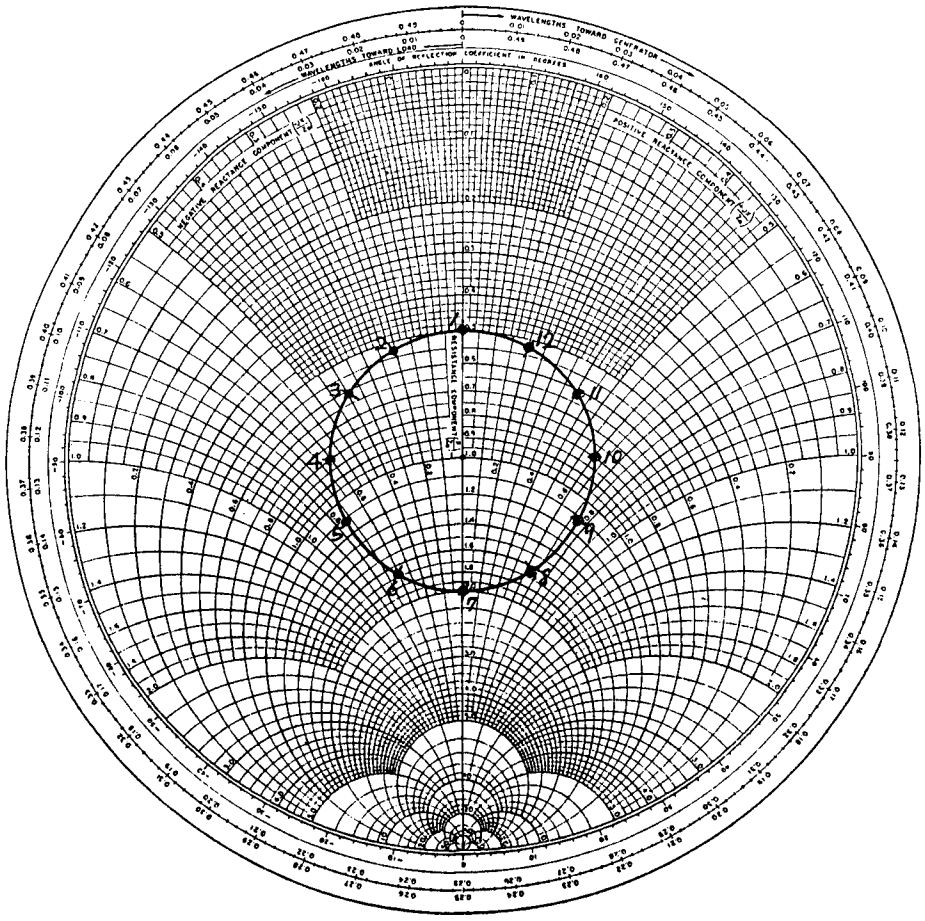

Fig 1. Twelve Points on Smith Chart

Point	SWR = 2.0		SWR = 5.0		SWR = 10.0	
1	0.5000	+j 0.0000	0.2000	+j0.0000	0.1000	+j0.0000
2	0.5264	-j0.1974	0.2137	-j0.2565	0.1071	-j0.2651
3	0.6154	-j0.3997	0.2632	-j0.5470	0.1329	-j0.5697
4	0.8000	-j0.6000	0.3846	-j0.9230	0.1980	-j0.9801
5	1.1429	-j0.7423	0.7143	-j1.4846	0.3883	-j1.6648
6	1.6653	-j0.6245	1.9174	-j2.3009	1.3103	-j3.2430
7	2.0000	+j0.0000	5.0000	+j0.0000	10.0000	+j0.0000
8	1.6653	+j0.6245	1.9174	+j2.3009	1.3103	+j3.2430
9	1.1429	+j0.7423	0.7143	+j1.4846	0.3883	+j1/6648
10	0.8000	+j0.6000	0.3846	+j0.9230	0.1980	+j0.9801
11	0.6154	+j0.3997	0.2632	+j0.5470	0.1329	+j0.5697
12	0.5264	+j0.1974	0.2137	+j0.2565	0.1071	+j0.2651

Fig. 2. Impedances on SWR Circle

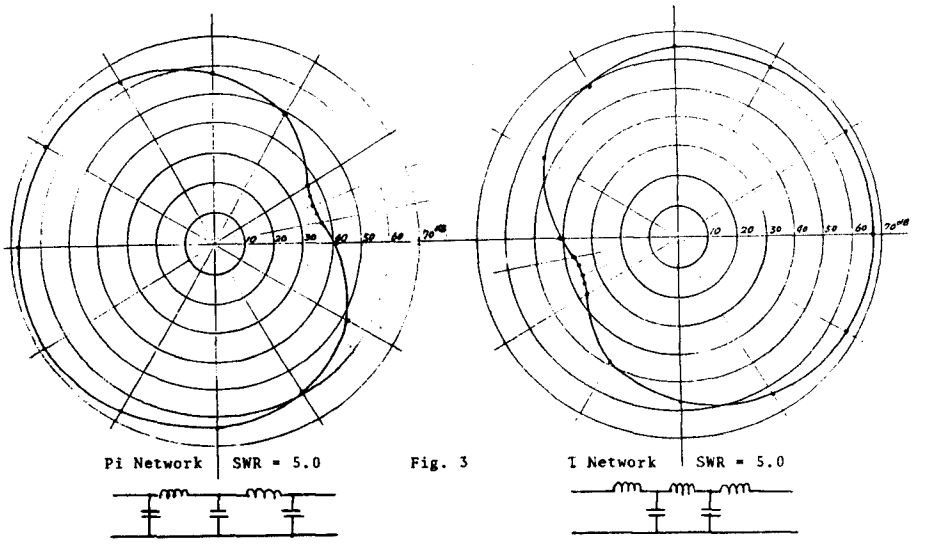

Fig. 3

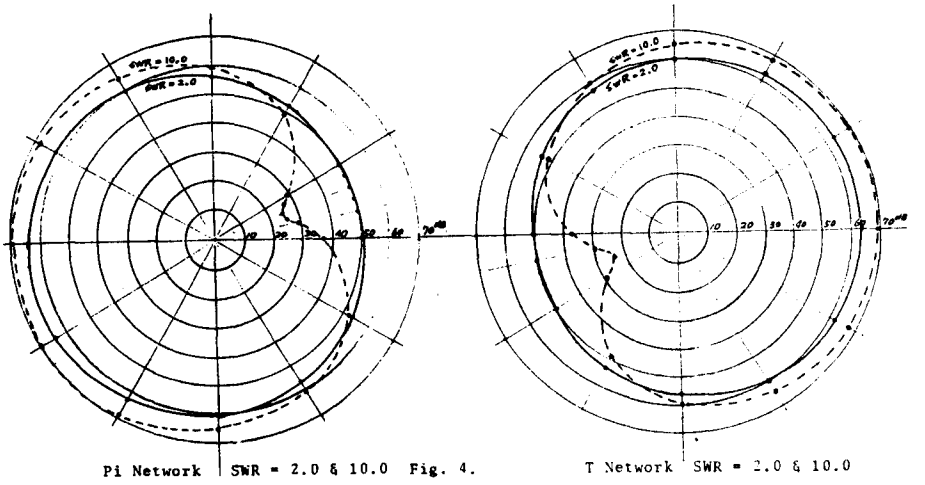

Fig. 4.

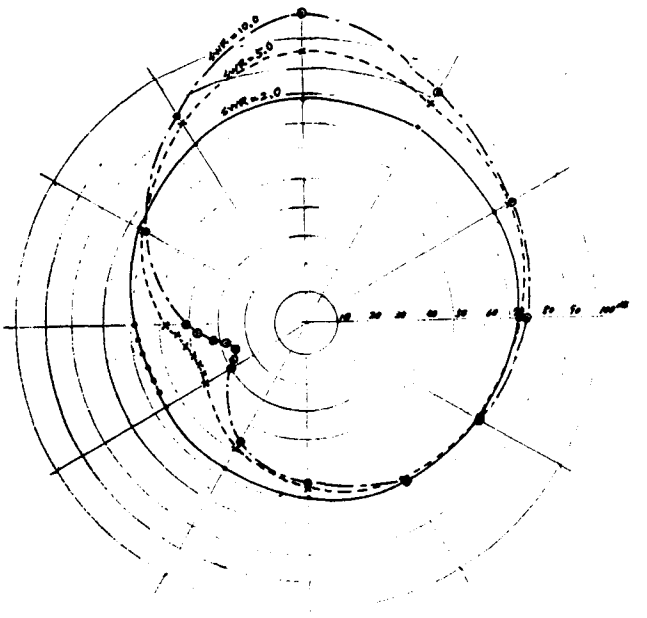

Fig. 5. Effect of Source Impedance - T Network

Components

Conducted by Mark Forbes, KC9C*

The purpose of this column is to keep the experimenter aware of new components that have been recently introduced. I am a development engineer in the research and development department of Duncan Electric Company. My job includes the design of both digital and analog circuits, as well as some software development. Because of this, articles and data sheets of many new products cross my desk that the average experimenter would not see for quite some time if ever. Through this column, I hope to be able to keep fellow experimenters posted. If you have any questions about a particular component, its availability or pricing, or anything regarding this column, feel free to drop me a line (s.a.s.e. please) or phone me. My phone number is: 317-447-4272, and you can call between 2300Z and 0230Z or weekends until 0230Z (please don't call later). The first two items are not "hot off the press," but are new enough that there has been no publicity in the Amateur Radio press.

SILICON SYSTEMS SSI 201 DTMF DECODER

DTMF decoding for autopatch or control use has come a long way in the last decade. Ten years ago *every* DTMF decoder for amateur use was designed using the 567 tone decoder. These systems had two big problems, however: 1) it took an awful lot of 567s to make a full 16-digit decoder, and 2) because the frequency was dependent on capacitors, it drifted with temperature. When Mostek introduced their DTMF decoder a couple years ago that only required an outboard filter for high group and low group, a limiter and a squarer, I thought that it would be only a matter of time before a single-chip decoder was introduced.

Silicon Systems has done exactly that with the SSI 201. This is a single chip that requires only a 3.579545 MHz color burst crystal and two 0.01 µF bypass capacitors for operation. The chip operates from a single 12-Vdc supply and contains all the analog and digital circuitry to convert DTMF audio into BCD digital signals. The circuit works extremely well and has an incredible dynamic range of 32.5 dB!

Although the SSI 201 is not exactly cheap (about $85.00 in single quantity) it is very economical in the long run when compared to a 567 system. The part is housed in an 18-pin ceramic DIP. For further information ask for the application note from: Silicon Systems Inc., 14351 Myford Rd., Tustin, CA 92680, 714-731-7110.

I have one of the chips, so if you have any questions or problems, get in touch.

NATIONAL SEMICONDUCTOR LM396 10-A REGULATOR

National introduced the LM396, which should be of interest to amateurs, last summer. The "Moose," as National calls it, is a self-contained, TO-3 packaged, adjustable voltage regulator. With proper heat sinking, this part is capable of regulating up to 10 amperes of current at an output voltage from -1.25 to 15 V.

Those specs make this a perfect part for a 13.8-Vdc power supply for even the high-power mobile 2-meter rigs. Other applications include a high-current 5-volt supply, or an adjustable high-current lab supply. Regardless of the application, National recommends an ample heat sink. In addition, liberal application of thermal compound is required. This device will dissipate up to 70 watts (remember that the power dissipation is the input voltage minus the output voltage times the output current); so don't use too high of an input voltage.

National recommends using 2000 µF per ampere of load current. Fortunately, hamfests are good sources of large capacitors. The high-temperature-rated capacitors will give a longer service life.

The Moose sells for about $10 in single quantities. More information on the LM396 can be obtained from: National Semiconductor corp., 2900 Semiconductor Dr., Santa Clara, CA 95051, 408-737-5000.

VARIAN CTC TO-220 RF TRANSISTORS

Varian (aka Eimac) has just introduced a high-power, uhf power transistor in a plastic TO-220 package. The plastic transistors are quoted to have higher gain than metal-ceramic type transistors and cost only about half to package. These transistors are capable of up to 30 watts at frequencies up to 500 MHz. These look very interesting! For more information: Communications Transistor Corporation, Varian Associates, 301 Industrial Way, San Carlos, CA 94070.

*1000 Shenandoah Dr., Lafayette, IN 47905, 317-447-4272 2300-0230Z weekdays, until 0230Z weekends.

Learning

PACKET SWITCHING: TOMORROW'S COMMUNICATIONS TODAY

This is a new book by Roy D. Rosner, K4YV on packet switching as applied to computer networks, voice, video, graphics and other forms of communications. It contains info on techniques, equipment, standards, commercial services and use of packet switching with satellites, cable and radio broadcasting. Price is $34.00 from the publisher, Lifetime Learning Publications, 10 Davis Dr, Belmont, CA 94002, 415-595-2350.

IEEE PRESS PUBLICATIONS

Modern Active Filter Design is the name of a new book edited by Rolf Schaumann, et al. Contents include design info on second-order, high-order, monolithic continuous analog and monolithic switched-capacitor filters -- a total of 42 reprinted papers. Ordering info:

Order No.	Binding	Nonmember	Member
PC01420	Cloth	$30.95	$23.30
PP01438	Paper	-	$15.45

This and other IEEE books are available from IEEE Service Center, 445 Hoes Ln, Piscataway, NY 08854.

FCC TUTORIAL VIDEO TAPES

The Federal Communications Commission Office of Science and Technology (FCC/OST) conducts a series of tutorials for the benefit of FCC personnel and the interested public. They are normally held in the Commission Meeting Room (Room 856) at 1919 M St., NW, Washington, DC.

For those who are unable to attend, video tapes of these tutorials are available (free of charge) by sending a blank VHS-120 cassette or U-Matic cassette (one-hour tape per hour or fraction of running time) to:

Audio-Visual Duplicator
Consumer Assistance & Information Division
Room 258, FCC
Washington, DC 20554

Their telephone number is 202-632-7000.

Here is a list of tutorials and their running times:

Title	Speaker/Affiliation	Time
Fiber Optics	Dr Charles Kao ITT	1:05
Bio-Effects of Non-Ionizing Radiation	Dr Robert Cleveland Geo-Met	1:03
Digital Speech	LTC Duane Adams DARPA	1:19
Precipitation Effects on Propagation	Dr Arno Penzias Bell Labs	1:06
Surface Acoustic Wave Devices	Dr Ernest Stern Lincoln Labs	0:27
An Overview of Computer Communications Protocols	Dr Vinton Cerf DARPA	1:08
Fundamental Limits of Information Theory	Dr Aaron Wyner Bell Labs	1:13
New Technology and Depreciation Policy	Dr Lee Davenport formerly GTE	1:15
Spread Spectrum Techniques in Non-Governmental Applications	Mr Walter Scales MITRE	1:15
Coding Theory and Near-Term Applications	Dr Elwyn Berlekamp Cyclotomics	1:02
Future of LSIs in the 90s	Mr Martin Cooper et al, Motorola	1:30
Transparent Metrology of Noisy Digital Signals	Dr Donald Halford NBS	0:55
Modulation and Coding for Efficient Digital Communications	Dr Andrew J Viterbi Linkabit Corp	1:15
Communications Satellites -- Achievements, Trends, and Projections	Dr Pier Bargellini	1:15

Data Communications (cont'd from page 8)

transmitted bits. Bit stuffing is used to avoid the occurrence of the flag bit pattern in the middle of a frame. The output is constantly checked for the occurrence of five one bits. If five one bits are detected, a zero bit is inserted. The receiving station always checks the incoming stream for five consecutive one bits and examines the next bit for zero. If a zero is found, it is deleted. The other feature chosen to be implemented is non-return-to-zero inverted (NRZI) encoding. This encoding scheme is chosen to ensure bit synchronization regardless of the length of the message. The combination of bit stuffing and NRZI encoding ensures a polarity change at least every six bits. If any brave experimenter attempts to generate this scheme in software using some other input/output device, these features should be taken into account. It should be easily seen that using an 8273 (or 1933) is the best answer to implementation of this scheme.

To begin, we must examine the protocol that we are using to communicate data between computers (or whatever the end user device is). It is a subset of the High Level Data Link Control (HDLC) standard protocol. It is closely related to both IBM's Synchronous Data Link Control (SDLC) and the Advanced Data Communications Control Procedure (ADCCP) protocols. The basic unit of information is the frame. The frame is composed of a link header, usually some information (called text) and a link trailer. Each frame has as a minimum, a flag byte (01111110), an address byte (more than one is authorized by HDLC), a control byte, two bytes of frame check sequence (CRC16) and a closing flag byte. The information can be inserted between the control byte and the frame check sequence as desired. There are three types of frames:

Unnumbered (also called Non-Sequenced) Information Frame: These frames have no sequence number at all and are used for setting operating modes such as connect and disconnect. A typical NSI frame appears like this:

FLAG ADDR CNTL FMCALL TOCALL FCS1 FCS2 FLAG

The address above is the address of the calling station (currently assigned by an area coordinator). The control field can be 17H for a connect request, 07H for a connect acknowledge, 53H for a disconnect request or 43H for a disconnect acknowledge. The Poll/Final (P/F) bit, 10H, is used to force a response from the receiving station. It demands a response and is also used in the other frame types for this purpose. The FMCALL is the call of the station orginating the frame and consists of six characters (left justified, blank filled). The TOCALL is the intended recipient of the frame in the six character format. This callsign sequence is required for connection, the establishment of flow contol between two packet stations.

Supervisory Frame: Used for window and flow control, these frames have receive sequence count (NR) but no send sequence count (NS). A typical supervisory frame appears like this:

FLAG ADDR CNTL FCS1 FCS2 FLAG

The address is the address of the sending station, the control field takes the form of either of two of the three defined control commands and responses. Receive Ready (RR) confirms sequenced frames of value NR-1 and indicates the orginating station is ready to receive. Receive Not Ready (RNR) indicates a temporary busy condition as buffer is full and no more frames can be accepted for a short time. RNR gives confirmation of sequenced frames of value NR-1.

Information Frame: These frames optionally contain information (text) and contain both received sequence count (NR) and send sequence count (NS). A typical information frame appears like this:

FLAG ADDR CNTL ....TEXT....FCS1 FCS2 FLAG

The address is the address of the sending station. The control field contains the sequence number of the next expected I-frame (NR) and the sequence count of this frame (NS). The text field is currently limited to 128 bytes and could be shorter or nil. It consists of ASCII-coded data (remembering the NRZI encoding and bit stuffing applied to the entire finished frame by the 8273 Protocol Encoder chip).

The addressing scheme used in the currently single byte packet address is the subject of much discussion. Currently, by convention, address 00H is reserved for no operation. In the Lockhart Station Node scheme, all users appear on the Station Node with address 00H and are assigned an address by the Station Node. Current United States users have chosen to hard code this address, assigning it by local area. The address 00H is still reserved in the U.S. scheme. For Magnuski style repeater operation, address 80H is reserved, addresses 81H-8FH are repeater input channel addresses, address C0H is reserved, addresses C1H-FEH are repeater output addresses. Address FFH is traditionally reserved for broadcast operation (all packeteers addressed. Both the ISO standard (HDLC) and the ANSI draft standard (ADCCP) allow for extension of this address field. Design work in this area is underway by Terry Fox, WB4JFI of AMRAD, but the current LIP software does not allow it.

Both the TIP and LIP software must deal with two circular buffers. They are circular in that only a fixed memory space is allowed for each and then they wrap. The

(continued on page 17)

first is the Line Buffer (also called the receive buffer). The buffer is used for modem input and CRT output. It has the following assigned pointers that must be studied:

OLBE - The oldest line buffer entry. This is the starting point of the oldest received packet.

LBPE - The line buffer processing entry. This point is the beginning of the frame being processed now.

LBOP - The line buffer output pointer that is the current byte being sent to the CRT now.

CLBE - The current line buffer entry points to the beginning of the frame receiving bytes from the outside world now.

LBIP - The line buffer input pointer is the actual place bytes incoming from the outside world (modem) are going into.

The second circular buffer is the Terminal Buffer (also called the transmit buffer). This is the buffer concerned with modem output and keyboard input. The following pointers are maintained for it:

OTBE - The oldest terminal buffer entry is the wrap point for this buffer. All entries started here.

CTBIE - The current terminal buffer input entry is the beginning of a packet being constructed from characters incoming from the keyboard.

TBIP - The terminal buffer input pointer indicates the actual place the incoming byte from the keyboard is going now.

CTBOE - The current terminal buffer output entry is the beginning point to transmit packets.

TBOP - The termianl buffer output pointer indicates the actual byte being sent out the modem now.

LTBOE - The last terminal buffer output entry is the point to stop transmitting packets (up to seven may be assembled for transmission with HDLC).

Thus we have begun our study of the LIP by defining a lot of terms required to look at the code. Thanks go to Hank Magnuski, KA6M and Terry Fox, WB4JFI who provided information for this analysis. A good text to further study HDLC/SDLC/ADCCP is "Communications Architecture for Distributed Systems" by R. J. Cypser (Addison-Wesley Publishing Company, 1978). In the next column, actual routines will be examined using the terms and pointers outlined in this column.

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