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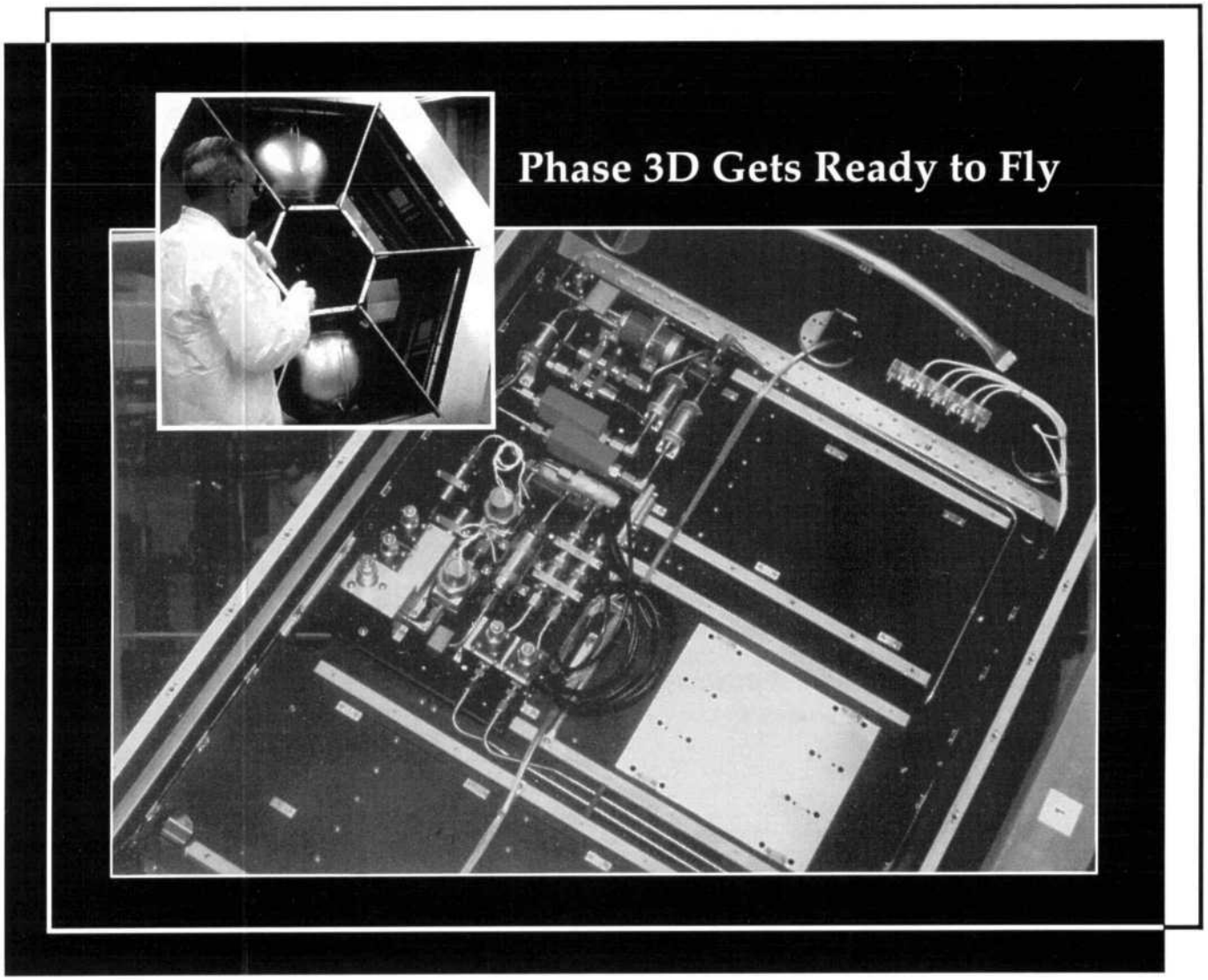
QEX

ARRL Experimenter's Exchange

October 1995



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Telex: 650215-5052 MCI
FAX: 860-594-0259 (24 hour direct line)
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Internet:qex@arrl.org

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About the Cover

Read the latest about Phase 3D this month in "Digital Communications." (Shown: Dick Jansson, WD4FAB.)

ISSUE NO. 164

Features

Columns

October 1995 QEX Advertising Index

THE AMERICAN RADIO RELAY LEAGUE

The American Radio Relay League, Inc, is a noncommercial association of radio amateurs, organized for the promotion of interests in Amateur Radio communication and experimentation, for the establishment of networks to provide communications in the event of disasters or other emergencies, for the advancement of radio art and of the public welfare, for the representation of the radio amateur in legislative matters, and for the maintenance of fraternalism and a high standard of conduct.

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Officers

President: RODNEY STAFFORD, KB6ZV
5155 Shadow Estates, San Jose, CA 95135

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Purpose of *QEX*:

1) provide a medium for the exchange of ideas and information between Amateur Radio experimenters

2) document advanced technical work in the Amateur Radio field

3) support efforts to advance the state of the Amateur Radio art

All correspondence concerning *QEX* should be addressed to the American Radio Relay League, 225 Main Street, Newington, CT 06111 USA. Envelopes containing manuscripts and correspondence for publication in *QEX* should be marked: Editor, *QEX*.

Both theoretical and practical technical articles are welcomed. Manuscripts should be typed and doubled spaced. Please use the standard ARRL abbreviations found in recent editions of *The ARRL Handbook*. Photos should be glossy, black and white positive prints of good definition and contrast, and should be the same size or larger than the size that is to appear in *QEX*.

Any opinions expressed in *QEX* are those of the authors, not necessarily those of the editor or the League. While we attempt to ensure that all articles are technically valid, authors are expected to defend their own material. Products mentioned in the text are included for your information; no endorsement is implied. The information is believed to be correct, but readers are cautioned to verify availability of the product before sending money to the vendor.

Empirically Speaking

DOS versus Windows

No, we're not trying to start a riot this month...although it *would* be entertaining! It's just that there is a legitimate question regarding development of software that supports our amateur experimental activities: Should we collectively be targeting DOS applications or Windows applications? (Speaking of starting a riot, no, Mac, OS/2 and Linux users, we haven't forgotten that you exist. But the reality of the home computer world is that it is predominately a DOS/Windows world—and getting more so.)

There is not a single "right" answer to the question. There are some types of applications that naturally fit better into one environment than the other. If, for example, your application requires printing of graphics, the Windows environment is almost certainly the place to be—trying to support the vast variety of different graphics printers in a DOS application is not for the weak of heart. On the other hand, a signal-processing application that needs to squeeze the most processing out of the available CPU cycles is probably best implemented in the DOS environment, where Windows' overhead won't get in the way. (If your application has *both* of these needs, good luck.)

But that leaves a large class of applications that aren't as demanding of specific resources. Suppose you're developing, say, a filter-design program. It could be as easily done under DOS as Windows. Which would be better? An improved (some would argue) user interface is available under Windows. If the needed user interface is fairly complex, much of the programming time for a DOS-mode application may be spent doing user-interface code that is largely "in the can" under Windows. On the other hand, a simple user interface may be more programming trouble under Windows than under DOS. And a DOS-mode program would be accessible to more PC users.

There are other considerations, too, such as memory management, video display handling and—not to be sneered at—the user learning curve of a unique interface. So the answer to DOS versus Windows isn't necessarily a given. But if the recent history of personal computers is any guide, one issue that is moot, or nearly so, is the available processing speed under DOS versus Windows. Except for that small class of needs-all-the-CPU-it-can-get applications, the percentage of CPU time spent on Windows' overhead has dwindled with the huge increase in computer speeds to the point where it's pretty much a nonissue.

So, what do *you* think? Should our bias be toward Windows for our design and development applications, or is DOS the environment of choice? Granted, there are those who hate the mere sight of a mouse. Equally, the typing-deficient user thinks keyboards smack of the 19th century. Setting aside these polar points of view, what makes the most sense for our a-building experimental toolbox?

This Month in *QEX*

Every repeater needs a CW ID circuit. If you're building your own repeater controller, this may be the most complex part of the control system. If so, you should be attracted to the simple one-chip solution, "A PIC Based Repeater IDer," by Gary C. Sutcliffe, W9XT.

A high-performance preamp is the key to a competitive microwave station, and the "PHEMT Preamp for 13 cm," by Rainer Bertelsmeier, DJ9BV, is just that.

What largely separates the good sounding receivers from the others is the performance of the AGC system. There are many approaches to AGC, but "A High-Performance AGC System for Home-Brew Transceivers," by Mark Mandelkern, KN5S, may be the one that best suits your home-building needs.

This month, "Conference Proceedings" lists the papers published at the 14th ARRL Digital Communications Conference and the 1995 AMSAT Space Symposium and Annual Meeting. Finally, Harold Price, NK6K, lets Steve Ford, WB8IMY, report on the AMSAT Annual Meeting, at which Phase 3D starred, in this month's "Digital Communications" column. —*KE3Z, email: jbloom@arrl.org*

A PIC Based Repeater IDer

A one-chip solution to a standard repeater control need.

By Gary C. Sutcliffe, W9XT

Last year the Washington County Amateur Radio Club (WCARC) of Wisconsin agreed to take over the local repeater that had been run by Maurice Heppe, W9MQD, for 25 years. The club did not have much money for equipment, but club members pitched in by donating time, money and equipment. The transmitter and receiver were donated commercial Motorola Micor equipment that was modified to operate on the 2-meter band.

The Motorola equipment can be configured to operate as a repeater with the right plug-in cards. These were easily found at hamfests. The one thing we were missing was a CW IDer. FCC rules require that amateur repeaters ID every ten minutes when the repeater is being used.

3310 Bonnie Lane
Slinger, WI 53086
Email: ppvvpp@mixcom.com

I volunteered to build an IDer for the club. I had the idea of using a Microchip Technology PIC microcontroller for generating CW in the back of my mind for a couple of years; here would be a good excuse to actually do it. I have done a number of PIC projects in the past, so this one should not be too difficult.

I wanted the PIC to do as much of the work as possible. It turned out that it was capable of doing just about everything needed. The only other circuitry needed was for the power supply and I/O. The PIC monitors repeater activity, acts as a ten-minute timer, drives a PTT relay and generates the CW. It even generates 900-Hz audio!

Hardware Design

Fig 1 shows the hardware design. The IDer is designed around the PIC 16C55. The PIC monitors the receiver's squelch to determine activity. I used an optoisolator to isolate the IDer from the radio equipment. The PIC also drives a PTT relay. This keeps the transmitter in operation when it is IDing and there is no signal being repeated.

The PIC has two CW outputs. One is on pin 12 but was not used in this application. It is simply set to a logical 1 during key-down time. You could use it to drive a transistor or other device in your application.

The other CW output (pin 11) is a 900-Hz tone during key down. Of course, this 900-Hz signal is a square wave. A simple R-C low-pass filter cuts out enough of the harmonics to turn the square wave into something resembling a sine wave. At least, it is close enough to a sine wave to sound good. R6 allows adjustment of the audio output level and C5 capacitively couples the audio to the transmitter.

A momentary push-button switch is used to reset the PIC. The software is written to immediately send the ID message after a reset. This is useful for setting the audio level since the unit will not ID again in normal operation for another ten minutes.

Software

The software is shown in Listing 1 and is available from the ARRL BBS (860-594-0306) as file PICCWID.ZIP and from the ARRL Internet server at http://www.arrl.org/qexfiles/piccwid.zip or via FTP from ftp.arrl.org in the /pub/qex directory. The program was written in PIC assembly language. The program spends most of its time waiting. When there is no repeater activity, it waits for the squelch line to go low (U1 pin 6), indicating that someone keyed up the repeater.

Assuming the repeater has previously been inactive, the ID sequence will be sent. It then goes into a lockout mode for two minutes. After that it resumes looking for U1 pin 6 to go low again. If that is detected within the next eight minutes, the ID will be repeated ten minutes after the last one.

Contacting Microchip Technology, Inc

You can get information about, and development software for, PIC controller devices directly from Microchip Technology, Inc. The World Wide Web URL http://www.ultranet.com/biz/mchip/ is Microchip's home page, which includes links to the needed files.

If you don't have Internet access but do have a modem, you can contact Microchip's BBS—possibly via a local phone call. The BBS is available via the CompuServe network, with no charge for the use of either the BBS or the network. Note that you aren't accessing CompuServe in this case, just using their network to get to Microchip's BBS.

To access the Microchip BBS via CompuServe's network, connect to a local CompuServe node using a speed of up to 9600 bit/s, 8 data bits, no parity and 1 stop bit (8N1). When the connection is made, hit **Enter**. CompuServe will display a message on your screen that may be garbled because CompuServe is expecting a 7E1 connection, not 8N1. Type **+** followed by **Enter**, and the message: "Host name:" should appear. Type **MCHIPBBS**, then press **Enter**. You should then get connected to the Microchip BBS.

If you don't know the number of a local CompuServe node, call 1-800-848-8980 (a tone-access menu system). Outside the US, call +614-457-1550.

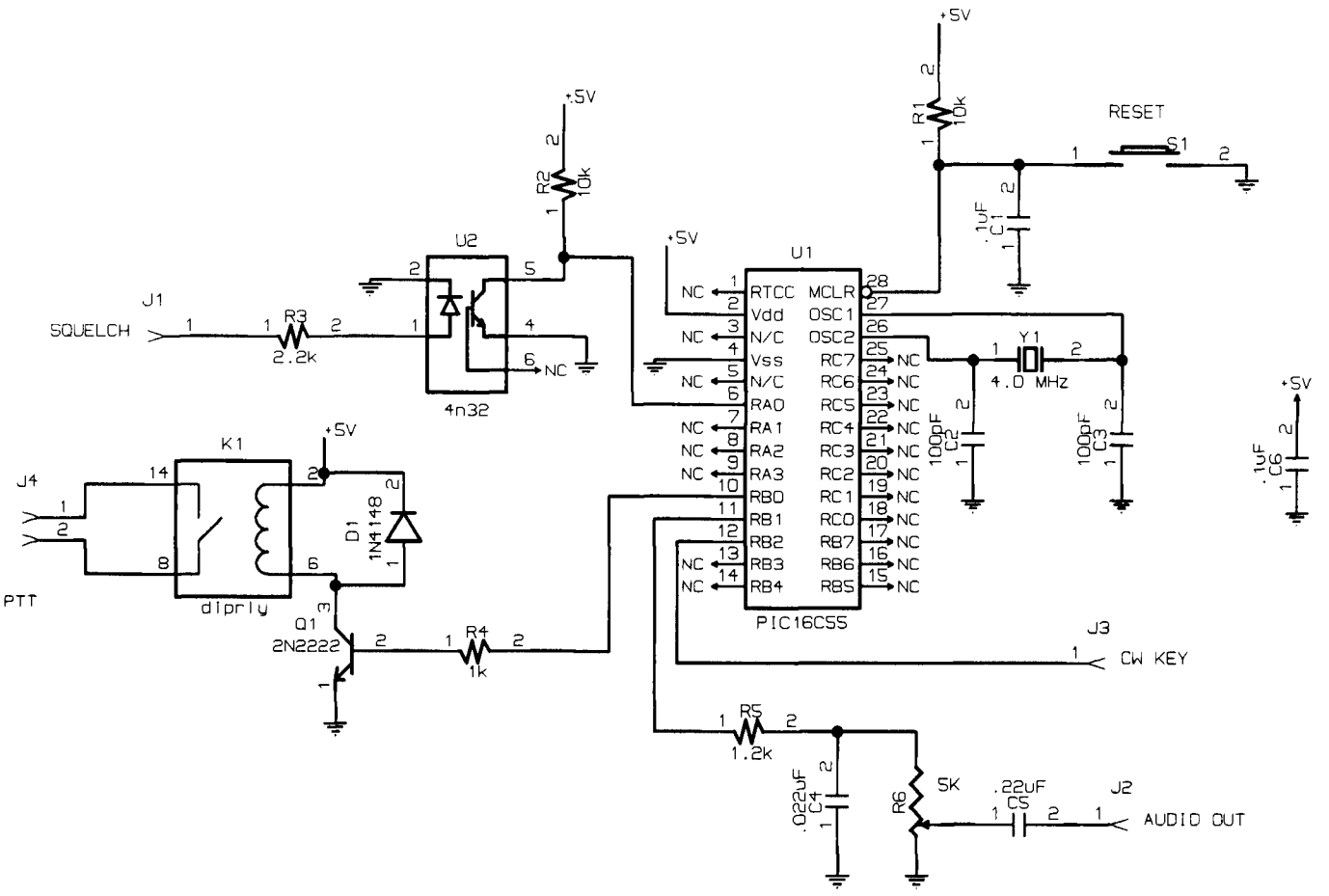


Fig 1

```
;*************************************************************************
; CWID.ASM - Repeater CW IDer based on the PIC 16C54
; By Gary C. Sutcliffe, W9XT
; Copyright 1995,  Gary C. Sutcliffe
; Rev 1.01    6 OCT 95
;*************************************************************************
; PIC Register and status bit definitions
;
status  equ     3h              ; F3 Reg is STATUS Reg.
f       equ     1               ;destination codes
w       equ     0

CARRY   equ     0h              ; Carry Bit is Bit.0 of F3
C       equ     0h
DCARRY  equ     1h
DC      equ     1h
Z bit   equ     2h              ; Bit 2 of F3 is Zero Bit
Z       equ     2h
P_DOWN  equ     3h
PD      equ     3h
T_OUT   equ     4h
TO      equ     4h
PC      equ     2h      ;program counter
porta   equ     5h      ;16C5X Port A
portb   equ     6h      ;16C5X Port B
portc   equ     7h      ;16C5X Port C - not implemented in 16C54, mem only
;*****************************************************************

;*****************************************************************
; Pin and variable definitions, program constants

ptt     equ     0h      ;Port B bit 0 (pin 10) PTT output
cwtone  equ     1h      ;Port B bit 1 (pin 11) morse tone output
cwkey   equ     2h      ;Port B bit 2  (pin 12) keyed morse output
sqin    equ     0h      ;Port A bit 0 (pin 6) indicates rcvr squelch broken

TFREQ   equ     0b7h    ;constant to ctl tone freq, hi value = low freq
                        ;b7h gives ~900 Hz with 4MHz xtal
BITTIME equ     036h    ;BITTIME determines how many cycles of the cw tone
                        ;frequency are required to equal the period of one
                        ; "dit" at the cw speed.  At 20 WPM, a bit time =
                        ; ~60 msec.  900 Hz => 1.11 msec.  60/1.11 = 54
                        ;54 => 36h.
flags   equ     08h     ;flags for program control
sqflg   equ     00h     ;squelch tripped flag in flags byte
wait    equ     01h     ;wait flag in flags
tmp     equ     09h     ; GP temp variables
tmp2    equ     0ah
lcnt    equ     0bh     ;loop count variable
cidx    equ     0ch     ;index into call sign table
bitcntr equ     0dh     ;bit counter, bit position in current byte
cwbyte  equ     0eh     ;byte to parse for sending CW
mscntr  equ     0fh     ;counts 50 millisecond delays
tensec  equ     10h     ;10 second  interval counter
;*****************************************************************
reset   org 01ffh
        goto start


        org 0
start   clrw                    ;set up option reg



        option
        call setup          ; setup i/o pin configs
        bcf portb, cwkey    ;be sure key is up at start
        call id             ;start out with an ID at startup or reset
        bcf flags,wait       ;don't wait 10 minutes to ID
        bcf flags,sqflg     ;start with no squelch broken
        call rsttime        ;reset 10 minute timer regs

; This is the main loop that handles when to ID

main
        btfss porta,sqin    ;check if rcvr squelch is broken (ie xmiting)
        bsf flags,sqflg     ;set the flag if it is
        btfss flags,sqflg   ;see if squelch flag set
        goto wtsome         ;if not, take some time off timer
        btfsc flags,wait    ;if we still have to wait, wait some more
        goto wtsome
        call id             ;transmitted & have not IDed in 10 min, ID now
        call wait2min       ;After ID, wait 2 min before checking xmit status
        bsf flags,wait      ;reset wait flag
        bcf flags,sqflg     ;clear squelch flag
        call rsttime        ;reset 10 minute timers
wtsome  call del50ms        ;kill 50 msec
        decfsz mscntr       ;check if msec counter = 0
        goto main           ;not this pass, try again
        movlw 0c8h          ;init 50 msec counter
        movwf mscntr        ;
        decfsz tensec       ;check if 10sec timer expired
        goto main           ;nope, go try again
        bcf flags,wait      ; tell them we don't have to wait to ID
        goto main

;*****************************************************************
;ID - sends call sign and operates PTT

id
        bsf portb,ptt       ;hit the PTT
        clrf cidx           ;set index to first byte in table
nxtbyt  movf cidx,w         ;get index in W for calc table offset after call
        call calltbl        ;get next byte from table
        movwf cwbyte        ;store byte
        movf cwbyte,f       ;see if its = 0
        btfsc status,Z      ;
        goto calldn         ;if =0, done sending call
        movlw 8
        movwf bitcntr       ;init bitcounter
nxtbit  btfss cwbyte,7      ;check most significant bit
        goto do0
        call keydown         ;hold key down 1 dit period
        goto newdit
do0     call keyup          ;key up 1 dit period
newdit  rlf cwbyte,f        ;rotate next bit into position
        decfsz bitcntr,f    ;see if we did all bits in this byte
        goto nxtbit         ;check the next bit in the byte of CW
        incf cidx           ;inc index to next byte in call sign table
        goto nxtbyt         ;get the next byte from call sign table

calldn  bcf portb, cwkey        ;be sure we end with key up
        bcf portb, ptt          ;release the PTT
        retlw 0                 ;end of ID
```

```
;*************************************************
; SETUP   configures I/O pins

setup   clrw
        tris portb          ;set port B as all outputs
        movlw 0fh           ; make port A all inputs
        tris porta          ; set port A
        retlw  1            ;return to main prog

;*********************************************************
; KEYDOWN - This sends a dit.  Note that this routine returns with
;cwkey in true (key down) position.

keydown bsf portb, cwkey  ;key down
        movlw BITTIME     ;go through loop this many times
        movwf lcnt
onecycd bsf portb,cwtone  ;set bit hi for first 1/2 of cycle
        movlw TFREQ       ;TFREQ is number of times through loop which
        movwf tmp         ;determines the tone freq
dlhi    decfsz tmp,f      ;decrement until 0
        goto dlhi
        bcf portb,cwtone  ;now clear the output pin for 2nd 1/2
        movlw TFREQ
        movwf tmp
dllow   decfsz tmp,f      ;wait until 0 to finish cycle
        goto dllow
        decfsz lcnt,f     ;
        goto onecycd      ;go do another cycle
        retlw 0           ;


;*********************************************************
; KEYUP - This is a delay for one bit period.  Note that this routine
; returns with cwkey in false (key up) position.  This routine is essentially
; the same as KEYDOWN except it does not toggle cwtone.  Instead it toggles
; a dummy bit in the tmp2 variable.  This is to keep the timing of the two
; routines the same.

keyup   bcf portb, cwkey  ;key up
        movlw BITTIME     ;go through loop this many times
        movwf lcnt
onecycu bsf tmp2,cwtone   ;simulate set bit hi for first 1/2 of cycle
        movlw TFREQ       ;TFREQ is number of times through loop which
        movwf tmp         ;determines the tone freq
ulhi    decfsz tmp,f      ;decrement until 0
        goto ulhi
        bcf tmp2,cwtone  ;simulate clearing the output pin for 2nd 1/2
        movlw TFREQ
        movwf tmp
ullow   decfsz tmp,f      ;wait until 0 to finish cycle
        goto ullow
        decfsz lcnt,f     ;
        goto onecycu      ;go do another cycle
        retlw 0           ;

;*************************************************************
; RSTTIME  - reset the registers that handle the 10 minute timer
; Because we wait 2 minutes after each ID, this is set up for 8 minutes
rsttime movlw 0c8h          ;init 50 msec counter
        movwf mscntr        ;when decr down to 0, 10 seconds elapsed
        movlw 30h          ;init 10 second counter for 8 min
        movwf tensec       ;10 min elapsed when = 0
        retlw 0
```

```
;*************************************************************************
; DEL50MS - software delay for 50 milliseconds.  Based on 4 MHz clock
;           Uses nested loop to generate delay

del50ms
        movlw 27h     ;Outer loop value
        movwf tmp
dl50o   movlw 0ffh    ;initialize inner loop value
        movwf tmp2
dl50i   goto dlnxt    ;fancy way of killing 2 cycles with 1 instruction
dlnxt   decfsz tmp2
        goto dl50i    ;end of inner loop
        decfsz tmp    ;check if outer loop done
        goto dl50o    ;if not restart inner loop
        retlw 0       ;return when done

;*********************************************************
;WAIT2MIN - Wait for 2 minutes.  After IDing, we will wait 2 minutes before
;checking if we will ID again because the repeater has been brought up again.
;This is to discourage kerchunkers and to prevent an endless ID every 10 min
;due to the repeater staying on a few seconds after IDing, and detecting
;the squelch being broken.

wait2min
        movlw 0c8h          ;init 50 msec counter
        movwf mscntr        ;when decr down to 0, 10 seconds elapsed
        movlw 0ch          ;init 10 second counter  for 2 min
        movwf tensec       ;2 min elapsed when = 0
wt2lp   call del50ms       ;kill 50 msec
        decfsz mscntr      ;check if msec counter = 0
        goto wt2lp         ;not this pass, try again
        movlw 0c8h         ;init 50 msec counter to count to 10 sec
        movwf mscntr       ;
        decfsz tensec      ;check if 10sec timer expired
        goto wt2lp         ;nope, go try again
        retlw 0            ;2 minutes are up, bug out


;*********************************************************
; CALLTBL - Callsign table.  This is were the call sign is put.  A 0
; is key up, 1 = keydown.  A dit is a single 1, a dah is three 1's
; in a row.  Put a 0 between dits & dahs in a letter. Put 3 0's between
; letters.  Put a few 0's at the very beggining so that the PTT relay
; has time to close before the CW starts.  The 1's & 0's are examined
; from left to right.
; The very last line must be all zeros.  That is what indicates the
; end of the ID string.

calltbl addwf PC,f        ;calc offset into table for next byte of CW
                          ;This table holds "DE N9LZW/R"
        retlw  B'00000001'    ;D..
        retlw  B'11010100'    ;..D
        retlw  B'01000001'    ;E N..
        retlw  B'11010001'    ;..N9..
        retlw  B'11011101'    ;..9..
        retlw  B'11011101'    ;..9
        retlw  B'00010111'    ;L..
        retlw  B'01010001'    ;..LZ..
        retlw  B'11011101'    ;..Z
        retlw  B'01000101'    ;Z..W..
        retlw  B'11011100'    ;..W..
        retlw  B'01110101'    ;../..
        retlw  B'01110100'    ;../..
        retlw  B'01011101'    ;..R
        retlw  B'00000000'    ; all zeros indicate end of table

        end                   ;end of CWID
```

This procedure will continue as long as the repeater is in use. It will be silent during periods of repeater inactivity. Just ground U1 pin 6 if you want your repeater to ID every ten minutes regardless of activity.

The timing for the CW (and ten-minute timer for that matter) is all done with software loops. With a 4-MHz crystal the CW speed will be about 19 WPM, just under the 20 WPM maximum specified by the FCC. Timing loops also generate the 900-Hz audio. You will need to modify the code if you wish to use different CW speeds or change the 900-Hz frequency to something else. Of course, a different crystal frequency will also affect the timing.

The one area of the code you will need to change is the call sign. The WCARC repeater trustee is Thomas Waldeschmidt, N9LZW, and his call is programmed into the PIC.

The call sign is entered at the end of the program. You must program a 1 for each key down period. Each dit is a single 1, and a dah is three consecutive 1s. A 0 is put in between dits and dahs in a letter, and three consecutive 0s separate letters.

The CW data is stored in 8-bit bytes, so the CW coding must be split up accordingly. A single letter or number may run over into two or more bytes. The program takes the call sign bytes one at a time and shifts through the bits. The output will be a key down or key up for 1s and 0s respectively. A byte consisting entirely of 0s indicates the end of the call-sign ID sequence.

PIC CW IDer Parts List

C1, C6—0.1-μF monolithic capacitor
C2, C3—100-pF disc capacitor
C4—0.022-μF disc capacitor
C5—0.22-μF disc capacitor
D1—1N4148 diode
K1—5-V, SPST DIP relay
Q1—2N2222 transistor
R1, R2—10-kΩ, 1/4-W resistor
R3—2.2-kΩ, 1/4-W resistor
R4—1-kΩ, 1/4-W resistor
R5—1.2-kΩ, 1/4-W resistor
R6—5-kΩ variable resistor
S1—Normally open momentary push-button switch
U1—PIC16C55 (or PIC16C54; see text)
U2—4N32 optoisolator
Y1—4-MHz crystal

Any of the above components and PIC development systems are available from:
Digi-Key
PO Box 677
Thief River Falls, MN
56701-0677
Tel: 800-344-4539

Information on PIC microcontrollers is available from:
Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ 85224
Tel: 602-786-7200

Construction

The WCARC unit was built on perf board using point-to-point wiring. The original design used a PIC16C55 since I had some left over from another project. You can also use the less expensive 16C54. The code didn't use any of the 16C55's features that are not available on the 'C54, so it works on either chip. Only the pin numbers differ.

The board was mounted in an aluminum box with phono connectors for all the input and output signals. A shielded enclosure is a good idea since the unit will normally be used just inches away from a transmitter.

To build your own unit you will need to be able to program the PIC with the code modified for your call sign. Most newer PROM programmers that can program micros and programmable logic can also do PICs. Microchip Technology and a number of other companies sell low-cost PIC development systems. An assembler for generating object code is available free from the Microchip BBS, or the Internet (see "Contacting Microchip Technology, Inc").

Summary

The PIC IDer is another example of how a low-cost microcontroller can be used to replace a number of components in a design. In this design, the microcontroller handles all the timing, control and output signal generation. With a few changes, the program could be modified to adapt to other application such as a VHF beacon.

Have fun building your PIC IDer, and if you ever find yourself in southeastern Wisconsin, tune to the WCARC repeater on 146.73 MHz and say hi! □□

PHEMT Preamp for 13 cm

Reprinted from Dubus Technik IV, Preamps and Receivers

By Rainer Bertelsmeier, DJ9BV

Abstract

A preamp equipped with a PHEMT provides top-notch performance in noise figure and gain as well as unconditional stability for the 13-cm band. Noise figure is 0.35 dB at a gain of 15 dB. It utilizes the NEC NE42484A C-band PHEMT and provides a facility for an optional second stage on board. The second stage, with the new HP GaAsMMIC MGA86576, can boost the gain to about 40 dB in one enclosure. The preamp is rather broadbanded and usable from 2300 to 2450 MHz.

Circuit

The construction of this LNA follows a proven 23-cm HEMT-LNA design using a wire loop with an open stub as an input circuit.[1]

The FET's grounded source requires a bias circuit to provide the negative voltage for the gate. A special active bias circuit (see "Bias Circuit for Grounded Source HEMTs") is integrated into the RF board, which provides regulation of voltage and current for the FET.

LNAH-2.3-N424A

Stub ST and inductance L1 (Fig 1) provide an optimum source impedance match for minimum noise figure. L1 functions as a dielectric transmission line above a PTFE board and has somewhat lower loss than a microstripline. L3 and L4 provide inductive feedback to increase the stability factor and the input return loss. R1, R2, L9 and R3 also serve to increase the stability factor. The system of C2, L5, C6, L7 and L8 is specially designed to match the output of the single-stage version to 50 Ω and to allow easy insertion of the GaAsMMIC for the two-stage version. In the two-stage version it provides the appropriate input and output match to the MMIC. This solution was found by doing some hours of design work with *Microwave Harmonica*. It allows the two versions to have the same PC board.

C4 provides a short at 2.3 GHz because it's in series resonance at this frequency. On all frequencies outside the operating band the gate structure is terminated by R1. Dr.1 is a printed λ/4-choke that decouples the gate bias supply.

LNAH-2.3-N424A/865

The two-stage version (Fig 2) utilizes an HP GaAsMMIC MGA86576 in

Glucksburger Str 20
D-22769 Hamburg
Germany

[1]Notes appear on page 12.

the second stage. It provides about 2 dB of noise figure and 24 dB of gain. The input is matched by a wire loop for optimum noise figure. The output is terminated by resistor R5 and a short transmission line, L10. Together with L7, L8 and C3, this results in a good measured output return loss.

The source pads have to provide a very low inductance path to the ground plane to preserve the MMIC's inherent unconditional stability. To achieve this unconditional stability, four ground connections are needed on each source. Appropriate source pads are provided on the PC board. Simulation indicates a minimum K factor of 1.2 in this arrangement on a 0.79-mm thick substrate. A thicker substrate is prohibitive.

The MMIC typically adds 0.07 dB to the noise figure of the first stage. This is somewhat difficult to measure because most converters will exhibit gain compression when the noise power of the source, amplified by more than 40 dB, enters the converter.

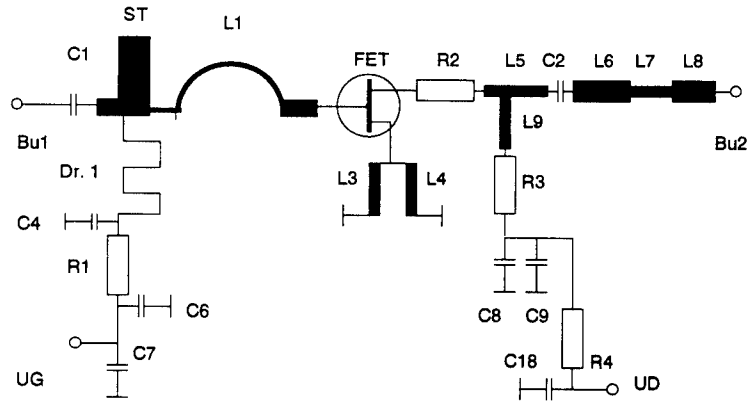


Fig 1—Circuit of LNAH 2.3 N424A.

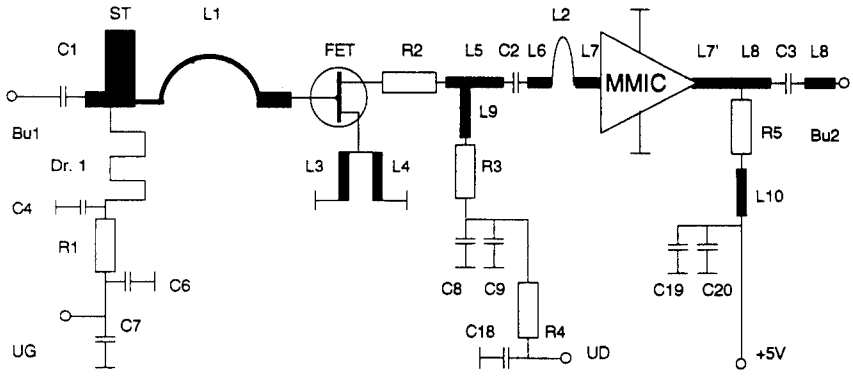


Fig 2—Circuit of LNAH 2.3 N424A/MGA865.

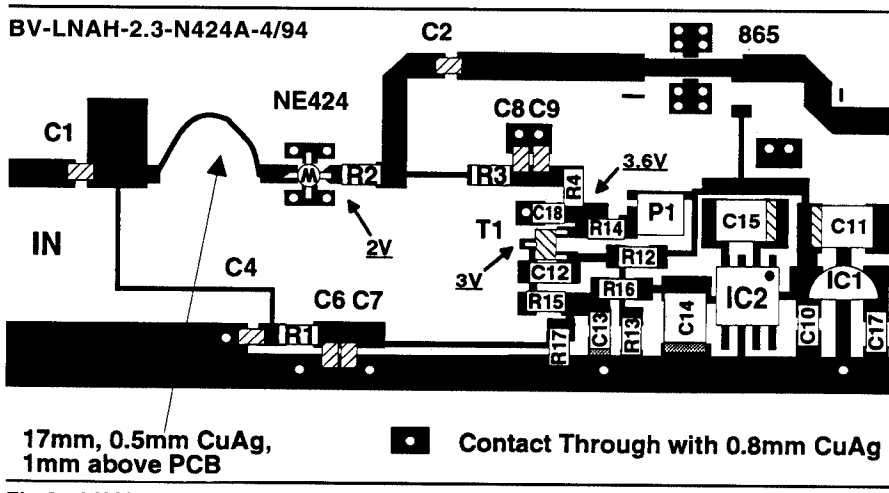


Fig 3—LNAH 2.3 N424A parts placement

Construction

The circuit is constructed using microstripline technique on 0.79-mm thick Taconix TLX glass (see Figs 3 and 5). An active bias circuit, which provides constant voltage and current, is integrated into the 34×72 mm PC board. Fig 4 shows the PC etching pattern.

LNAH-2.3-N424A

Fig 3 shows the parts layout for the single-stage version. Fig 6 shows the FETs as viewed from the top. Construction proceeds as follows:

1. Prepare a tinned box (solder side walls).
2. Prepare the PC board to fit into the box.
3. Prepare the holes for N-connectors into the box. Note: The input and output connectors are asymmetrical. Use the PC board to mark the connector positions.
4. Drill holes for through contacts (0.9-mm diameter) in the PC board and connect through with 0.8-mm CuAg (silver-plated copper) at the indicated positions.
5. Solder all resistors onto the PC board.
6. Solder all capacitors onto the PC board.
7. For L1, cut a 17-mm length of CuAg, 0.5-mm diameter wire. Bend down a

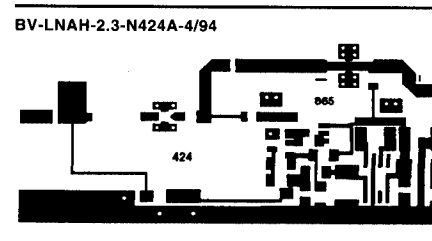


Fig 4—PC board LNAH 2.3 N424A.

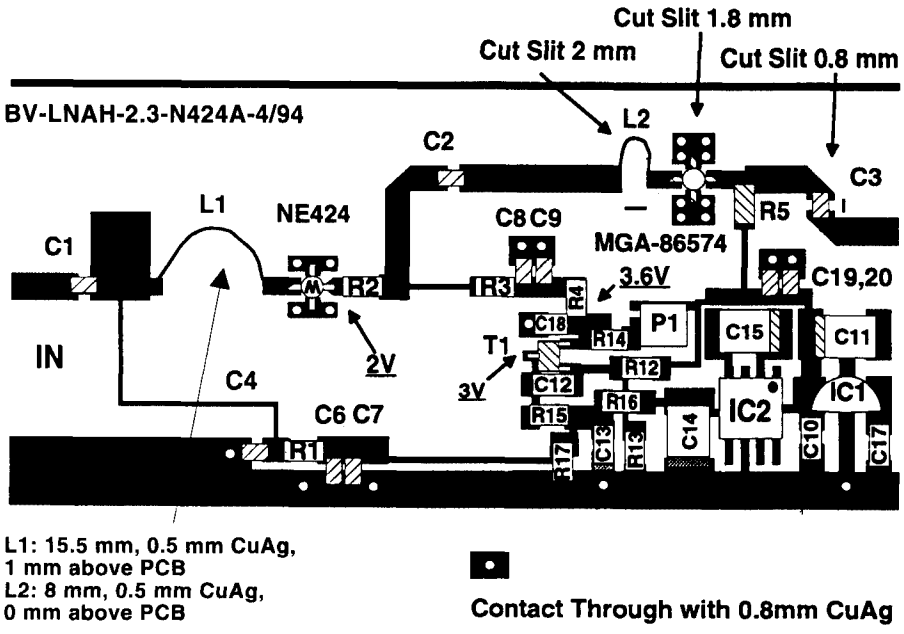


Fig 5—LNAH 2.3 N424A/MGA865 parts placement.

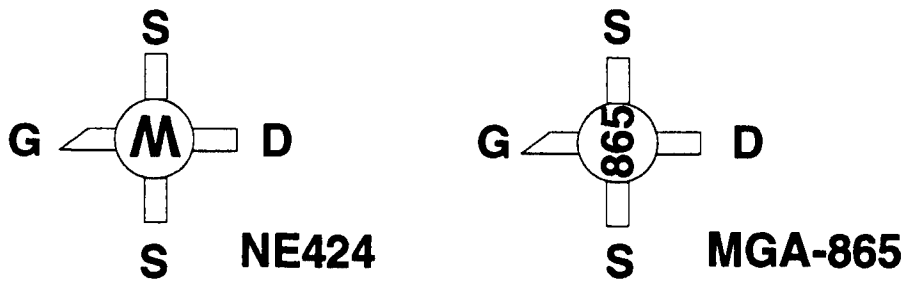


Fig 6—Top view of NE424A and MGA865.

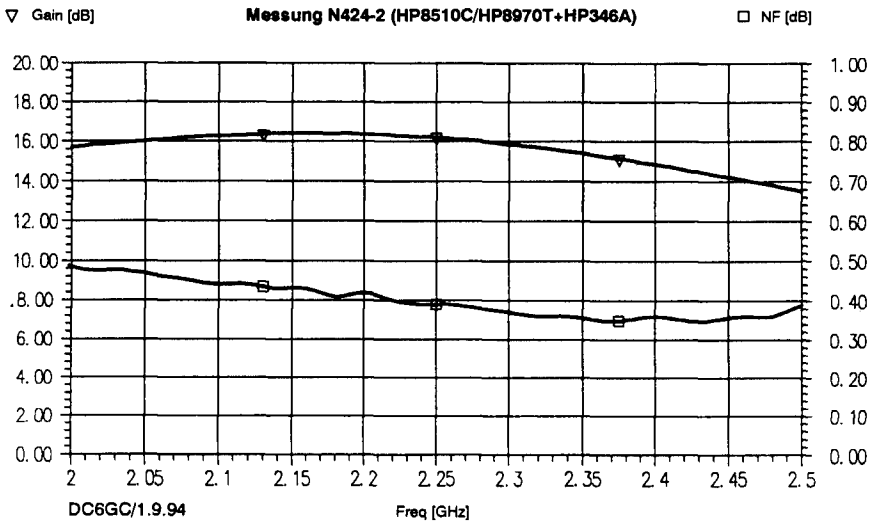


Fig 7—Measured noise figure and gain of LNAH 2.3 N424A.

1-mm length at each end to 45°. Form the wire into a half-circle loop according to Figs 3 and 5. Solder the wire into the circuit with a 1-mm clearance from the PC board. The wire loop has to be flush with the end of the gate stripline and should be soldered at a right angle to it. The wire loop has to be oriented flat, *parallel* to the PC board.

8. Verify the open-loop functioning of the bias circuit. Adjust P1 to 45 Ω. Solder a 100-Ω test resistor from the drain terminal of the PC board to ground. Apply +12 V and measure +5 V at the output of IC1, –1 V at IC2, pin 5, –2.5 V at the collector of T1, +3.6 V at the emitter of T1, +3 V at the base of T1, –2.5 V at R17 and +2 V across the 100-Ω resistor. If okay, remove the 100-Ω test resistor.
9. Solder PHEMT NE424A onto the PC board. Use only an insulated soldering tool and ground the PC board, your body and the power supply of the soldering tool. Never touch the PHEMT at the gate—only at the sources or the drain—when applying it to the PC board and solder fast (less than 5 seconds).
10. Solder the N-connectors into the side walls of the box.
11. Solder the finished PC board into the box—solder from both sides at the side walls and solder the center pins of the connectors to the microstriplines.
12. Solder the feed-through capacitor into the box.
13. Connect D1 between the feed-through capacitor and the PC board.
14. Connect 12-V B+ and adjust P1 for 16 mA of drain current (measure 160 mV across R4 on the RF board). Voltages should be around +2 V at the drain terminal, –0.4 V at the gate and +3.6 V at the emitter of T1.
15. Connect the LNA to a noise-figure meter—if you have one—and adjust the input wire loop, changing the clearance to the PC board, as well as the drain current, by adjusting P1, for minimum noise figure. Even without tuning, the noise figure should be within 0.1 dB of the minimum because of the limited tuning range of the wire loop.
16. Glue conducting foam onto the inside of the top cover and attach it to the top of the box.
17. Your small wonder is now finished.

LNAH-2.3-N424A/865

Refer to Fig 5 for construction layout. Construct as follows:

1. Prepare the PC board by cutting slits into the microstriplines around the MGA865. These are: a 2-mm slit for L2, a 1.8-mm slit for the MMIC and a 0.8-mm slit for C3.
2. For L2, cut an 8-mm length of CuAg, 0.5-mm diameter wire. Form the wire into a half-circle loop according to Fig 5. Solder the wire loop into the circuit. The wire loop has to lie flat on the PC board. The wire loop must be flush with the end of the gate stripline and should be soldered at a right angle to it.
3. Follow the instructions given above for the single-stage version.

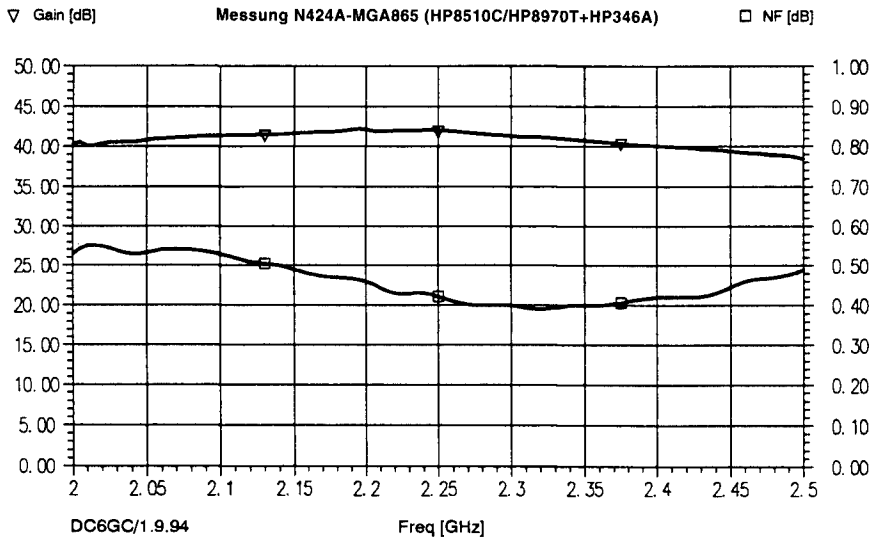


Fig 8—Measured noise figure and gain of LNAH 2.3 N424A/MGA865.

Measurement Results

Noise Figure and Gain

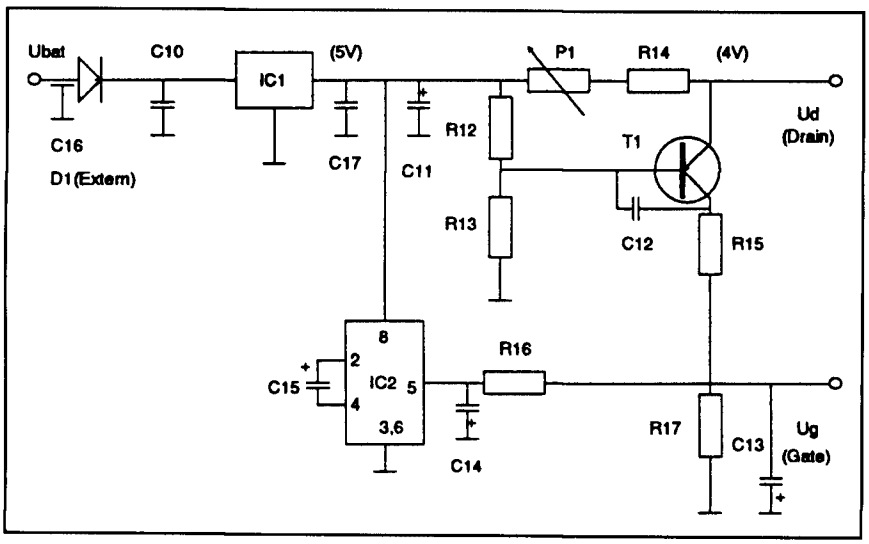
Measurements were taken using an HP8510 network analyzer and an HP8970B/HP346A noise-figure analyzer, transferred to a PC and plotted.

Figs 7 and 8 show the measurement results for gain and noise figure for the one-stage and two-stage versions, respectively. Using a special PHEMT NEC NE42484A optimized for C-band, a typical noise figure of 0.35 dB at a gain of 15 dB can be measured at 2.32 GHz. An optional second stage on the same PC board with the GaAs MMIC MGA86576 from HP will boost the gain from 15 dB to 41 dB. The two-stage version can be used for satellite operation. For EME, where lowest noise figure is at premium, a cascade of two identical one-stage LNAs may be more appropriate.

Both versions are rather broadbanded. They can cover the various

Bias Circuit for Grounded Source HEMTs

The FET's grounded source requires a bias circuit to provide the negative voltage for the gate. A special active bias circuit is integrated into the RF board, which provides regulation of voltage and current for the FET. PNP transistor T1 operates in a feedback loop with the FET and forces a constant current through the FET. T1 maintains a constant voltage across R14 and P1 by regulating the negative gate voltage on the FET. The drain voltage is set by R12 and R13. P1 serves for current adjustment (7 through 25 mA). IC1 is a standard 5-V regulator. IC2 generates the negative voltage. C13 provides a time delay of 10 ms and suppresses the 1-kHz ripple frequency of IC2.



On board bias circuit.

Measurements: LNAH 2.3 N424

13 cm: One-Stage Version

Device:	NE42484A
Noise Figure:	0.35-dB typically at 2320 MHz
Gain:	15 dB typically at 2320 MHz
Input RL:	6 dB
Output RL:	22 dB
Bandwidth:	NF<0.4 dB from 2220 through 2500 MHz
Stability K:	>1.2 from 0.2 through 20 GHz
Supply Current:	20 mA

13 cm: Two-Stage Version

Devices:	NE42484A and MGA86576
Noise Figure:	0.45 dB typically at 2320 MHz
Gain:	41 dB typically at 2320 MHz
Input RL:	5 dB
Output RL:	20 dB
Bandwidth:	NF<0.5 dB from 2000 through 2500 MHz
Stability K:	>4 from 0.2 through 20 GHz
Supply Current:	36 mA

portions of the 13-cm amateur allocation from 2300 to 2450 MHz without retuning.

The real surprise is the performance of the C-band PHEMT NE424A. It performs better than several other HEMTs (FHX35, FHX06, NE324, NE326) tried in this circuit, and it measures 0.15 dB better than its published noise figure. In fact *Microwave Harmonica* simulation predicts a 0.5-dB noise figure based on the data sheet value. The lower measured noise figure seems to be due to a special bias current and the lower magnitude of $|\Gamma_{OPT}| \approx 0.75$, which is caused by the gate length of 0.35 µm and a gate periphery of 500 µm. This provides optimum properties for application in 2 through 4 GHz LNAs.

Stability

Stability is excellent. This has been achieved by a carefully controlled combination of inductive source feedback, resistive loading in the drain and nonresonant dc-feed structures for drain and gate. A broadband sweep from 0.2 to 20 GHz showed a stability factor K of not less than 1.2, and the B1 measure was always greater than zero. These two properties indicate unconditional stability. At the operating frequency of 2.3 GHz, the stability factor is about 1.6. The two-stage version with the MGA865 measures K>4 at all frequencies.

Conclusions

The new preamp provides another quantum leap toward the perfect noiseless preamp. It uses a low-cost and rugged C-band PHEMT instead of relying on expensive X-band HEMTs. An improvement of about 0.2 dB in noise figure has been achieved in comparison to a no-tune HEMT preamp.[2] This improvement provides roughly 1.5 dB more S/N in EME or satellite operation but is not noticeable in terrestrial links. However, the new preamp has to be tuned. This requires a noise-figure meter for alignment. For those who like a no-tune device, the HEMT preamp provides adequate performance. The preamp described in note 2 measures 0.55 dB of NF typically.

Acknowledgements

I have to thank Dr U. L. Rohde, KA2WEU/DJ2RL, from Compact Software Inc, and its German distributor, Klaus Eichel, DL6SES/KF2OO, from TSS, for lending the *Microwave Harmonica* software, which proved to be an excellent tool for the design; Rainer Jäger, DC3XY, for providing kits for these preamps; and last but not least, Dieter Briggmann, DC6GC, for the professional measurement of S-parameters and noise figures. Without their help this work would not have been possible.

Parts list for the LNAH 2.3 N424A/M865

Teile-Nummer/Part-No.	Art/Sort	Wert/Value	Hersteller/Manufacturer	Herst.-Bez./Manuf.-No.
C1	Chip-C 50mil	4.7pf (500 CHA 4R7 JG)	Tekelec	CHA
C2,3,6	SMD-C	100 pF	Sie	0805
C4	SMD-C	5.6 pF	Sie	0805
C7,8,19	SMD-C	1000 pF	Sie	0805
C9,18,20	SMD-C	10 nF	Sie	0805
C10,12,17	SMD-C	0.1 µF	Sie	1206
C11,14,15	SMD-Elco	10 µF	Sie	1210
C13	SMD-Elco	1 µF	Sie	1206
C16	Feed-Thr.	1000 pF	Sie	
R1,3	SMD-R	47 Ω	Sie	1206
R2,14	SMD-R	39 Ω	Sie	1206
R4,5	SMD-R	10 Ω	Sie	1206
R12	SMD-R	6.8 kΩ	Sie	1206
R13,15	SMD-R	10 kΩ	Sie	1206
R16,17	SMD-R	22 kΩ	Sie	1206
P1	SMD-Pot	100 Ω	Murata	4310
Dr.1	Printed	λ/4		
L1	Wire Loop	0.5 mmCuAg, 15.5 mm long, 1 mm above PCB	Homemade	
L2	Wire Loop	0.5 mmCuAg, 8 mm long, on PCB	Homemade	
D1	Diode	1N4007	Mot	
FET	GaAs-FET	NE42484A	NEC	
MMIC	GaAs-MMIC	MGA-86576	HP	
T1	PNP	BC807,856,857,858,859	Sie	SOT-23
IC1	Regulator	uA7805A	Mot	TO-92
IC2	Inverter	LTC1044SN8 (ICL7660SN8)	LT (Intersil)	SO8
Bu1,2	Coaxial	N-Small Flange or SMA	Radiall/Suhner	
PCB	Teflon PCB, Taconix TLX	35 x 72 mm, 0.79 mm, Er=2.55, -LNAH-2.3-N424	DC3XY	
G	Box, Weißblech (Tinplate)	35x74x30 mm		

All Parts except D1, C20 and uA7805A are SMD-Parts

Notes

Parts, kits and PC boards are available from Rainer Jäger, DC3XY, Breslauer Str 4, D-25479 Ellerau, Germany, tel: +49 41 0673430. Ready-made and calibrated units are available from Frank Schreyer, DD1XF, Maimoorweg 32, D-22179 Hamburg, Germany, tel: +49 40 6428253.

[1]Bertelsmeier, R., DJ9BV, "HEMT LNAs for 23 cm," *Dubus Technik IV*, pp 193-206.

[2]Bertelsmeier, R., DJ9BV, "No-Tune HEMT Preamp for 13 cm," *Dubus Technik IV*, pp 207-213.

A High-Performance AGC System for Home-Brew Transceivers

Ham-band conditions create a severe strain on any receiver. This AGC system provides smooth gain control with no ear-splitting pops and clicks.

By Mark Mandelkern, KN5S

Amid the glowing reviews and happy reports of the newest developments in receiver technology, one still sometimes finds complaints of AGC troubles—pops, clicks, and other characteristics of poor AGC performance. A ham shack is an environment totally different from a lab test bench or a commercial station. A receiver that functions beautifully when connected to a signal generator, or even several generators at constant level, or when tuned to a single station, may be completely unusable with a ham antenna attached. For real-world amateur operation we need immediate, silent, automatic adaptation to dynamic signals of vastly different levels.

A good AGC system should react instantly, with no popping noise, to signals suddenly appearing at a level 100 dB over the residual noise in a quiet receiver. One should not hear receiver rushing noise between CW dits or SSB syllables. When a strong signal disappears, the receiver should be almost instantly ready to hear a weak signal right down at the noise level.

Although it took three years to design and build, most portions of my home-brew transceiver (Fig 1) caused no special trouble. But obtaining the desired AGC performance required more elaborate measures than expected and even a special AGC test device. The results were well worth the effort; the resulting AGC system performs beautifully, and the home-brew transceiver has been in constant use for the last three years. The AGC system and the special test device will be described here.

5259 Singer Road
Las Cruces, NM 88005

Fast or Slow?

It can be quite misleading to label an AGC mode as simply fast, medium or slow. In fact, there are three timing periods involved: attack time, hang time and recovery time. These are sketched in Fig 2. While the mode designation should refer to the hang time, most receivers unfortunately have no hang circuit, and the designation thus refers to the recovery time.

The attack time is perhaps the most crucial; trouble here is often responsible for clicks and pops on the leading edge of a strong CW or SSB signal. Filter delay and incorrect attack time can also result in overshoot, where the leading edge of a dit causes a pop, because of AGC lag, followed by overcorrection and excessive receiver gain reduction. Just what you're listening for—perhaps a DX signal report—is made to sound weaker! The fast, medium and slow designations do

not apply to this first timing period. A receiver should be designed for immediate adaptation to any signal level. Unfortunately, some receivers employ an excessive recovery time to compensate for inadequate attack performance. This leaves the pop on the first dit but reduces the receiver gain during the rest of the transmission so that more pops are not heard. The great disadvantage of this band-aid method is slow recovery. When the strong locals stop calling, the receiver is not ready for the weak DX station for maybe one or two seconds. Too late to hear him come back to you! A common practice for circumventing this problem is to turn the AGC off; hearing damage can result! The proper attack time for a given receiver depends on the selectivity, the nature of the filters and the resultant filter delay.

The hang portion of a proper AGC system is not always included in modern receivers. It is simpler to include a slow recovery—just a capacitor—but the results are quite undesirable, as explained above. A slow recovery involves a simple R-C circuit with a gradual decay in AGC voltage, perhaps several seconds being required for full receiver gain recovery and reception of the weakest DX signals. On the other hand, a proper hang circuit maintains a nearly constant AGC voltage between dits or syllables, then cuts out completely, allowing the recovery circuit to quickly bring the receiver up to full gain. It is the hang circuit that should be adjustable because of the differences between competitive and casual operation. For fast, medium and slow, I use hang times of 100 ms, 300 ms and 3 s. Some operators choose different AGC timings for CW and SSB; however, this usually means that recovery time is being used to compensate for other AGC deficiencies. With the system described here, performance on CW and SSB is the same, as it should be. I almost always use medium; sometimes slow for ragchewing, and occasionally fast for unusual noise or QRM conditions. The AGC is turned off only for tests and measurements.

The last timing period, the recovery, is very simple, provided it is not improperly used to compensate for the lack of a hang circuit, or for inadequate attack performance. When the strong signal is gone, and the hang circuit has held for as long as you've asked it to, you want full recovery as quickly as possible. A 100-ms recovery does this smoothly.

Filter Delay

The IF strip in this receiver uses very sharp CW and SSB filters, both at the input *and near the output*. No AGC is applied to the receiver front end before the first filter for optimum weak-signal performance. The AGC detector senses signal level after the second filter; otherwise it would sense signals that you don't hear and cause an unwarranted decrease in gain for the weak signal you want. In order to prevent a pop on the leading edge of a CW dit or an SSB syllable, the system must employ a very fast attack time. But there is a considerable delay through the second filter. This means that the signal at the IF output builds up to a high level before the AGC has a chance to decrease the IF gain; this produces the pop. Even worse, this large signal then appears at the AGC

Fig 1—In my home-brew transceiver shown here, the AGC switch is labeled OFF-F-M-S. The SQUELCH (down) switch is part of the OPERATE (up) and STANDBY (center) switch, which is labeled merely OPER-SQ. The meters read signal level in dB and squelch integrator charge. Not shown here are the three separate transceiver front-end sections for MF/HF, 6 meters, and 2 meters.

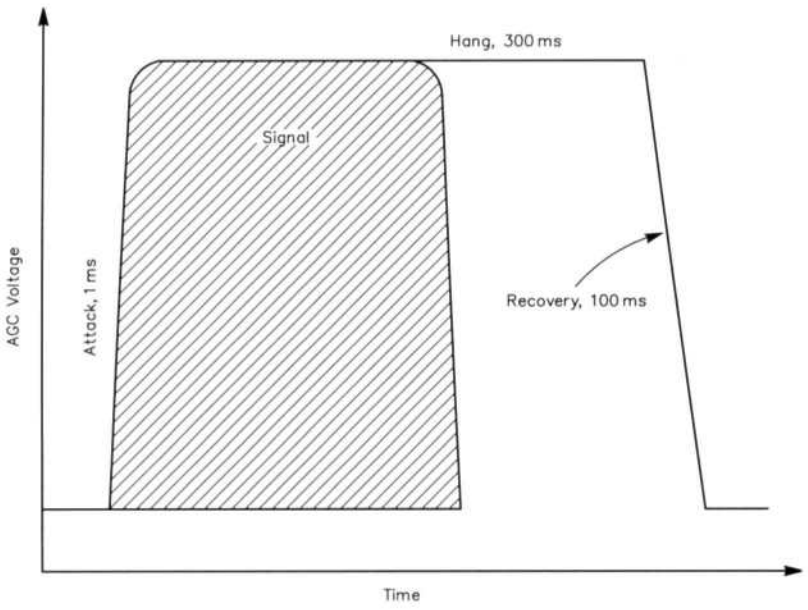


Fig 2—The three AGC timing periods—attack, hang and recovery—shown here in concept, but not to scale.

detector, producing excessive AGC voltage and decreasing the receiver gain, often causing a noticeable dip in AF output; this is the overshoot. The combination of delay and overshoot can even result in AGC oscillations producing distortion in the receiver audio output. Some of these AGC malfunctions are sketched in Fig 3.

Dual-Attack Timing

This, then, is the problem. Filter delay makes it impossible for any simple AGC system to maintain instantaneous gain control. The result is either popping, or overshoot, or both. R. L. Drake's solution was a dual system (see acknowledgments at the end of the article). The circuitry is surprisingly simple. The IF strip is separated into two parts, called IF1 and IF2. The output filter is moved to a position between them where it performs its function just as effectively. The two portions of the IF strip are then provided AGC voltages with different characteristics.

A block diagram of the IF system is shown in Fig 4. The first portion, IF1, consisting of the amps before the second filter, receives a delayed AGC voltage, denoted AGC1. The time constant is chosen, using the special test device described below, to eliminate overshoot and obtain smooth control of IF1. Now this leaves a pop at the input of IF2, but it doesn't reach the headphones because an undelayed AGC voltage, denoted AGC2, controls IF2 almost perfectly. The AGC detector is at the end of IF2, so there is no filter in the IF2-AGC2 loop. In my home-brew transceiver, the 9-MHz IF strip consists of six MOSFET amps, split four and two into IF1 and IF2. The action of AGC1 on IF1 is sluggish, but smooth, in its response to signals at different levels, while IF2 reacts almost instantaneously to AGC2. During the leading edge of an initial dit or syllable, only AGC2 at IF2 functions, maintaining constant receiver output level while giving IF1 a chance to catch up. On this leading edge, the AGC2 voltage applied to IF2 may be very high, but it's all too quick even to be seen on the S-meter. As the AGC1 voltage to IF1 rises gradually (meaning over several milliseconds), the AGC2 voltage drops. During this process the overall IF gain is constant, but shifts from being derived mostly from IF1 to a balanced state.

An additional valuable feature of this system is that AGC2 reduces a short static pulse to the receiver operating level, even more effectively than noise-clipping.

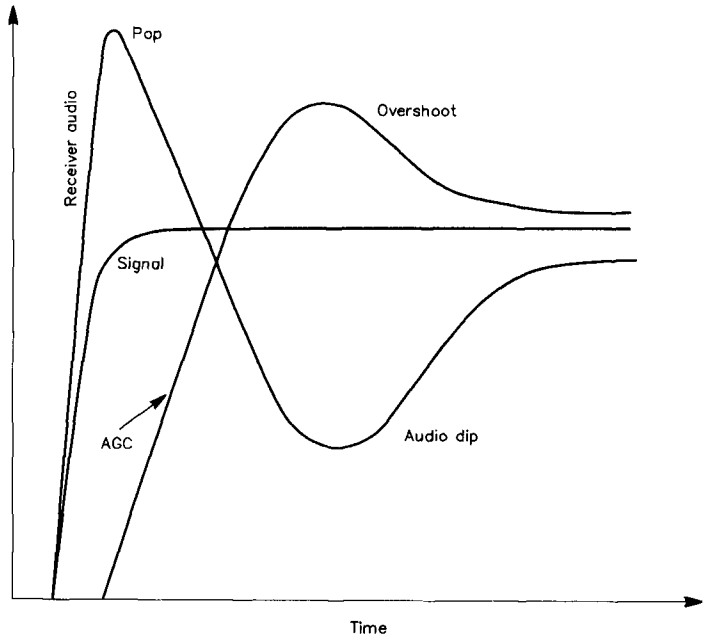


Fig 3—AGC problems to be avoided—slow attack time and AGC overshoot. This rough sketch is not to scale.

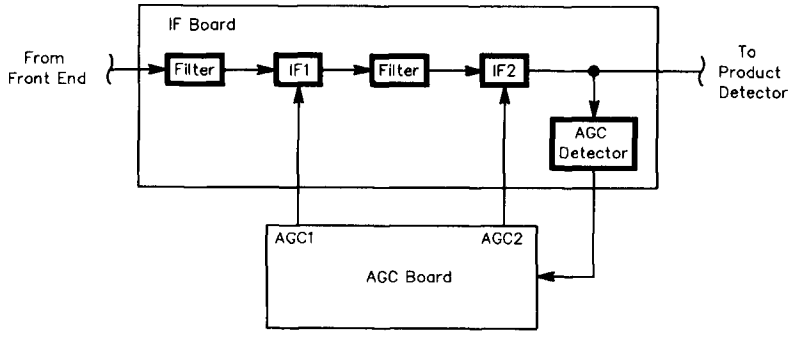


Fig 4—Block diagram of the IF system.

Circuit

A block diagram of the AGC system is shown in Fig 5. A general description of the system will be given here. The block diagram shows all the active circuit elements and certain other important components mentioned in this general description using a symbolic pseudo-schematic abbreviated representation. The five sections will be discussed in detail under separate headings; complete schematics are shown in Figs 6-9 and 11.

The detector section includes an AGC amplifier, which ensures that

Fig 5 (right)—Block diagram of the AGC system. This shows the active circuit elements and certain other important components using a symbolic pseudo-schematic abbreviated representation. Circles are transistors, triangles are op amps. For the actual circuits, the schematics in Figs 6-9 and 11 must be used. Potentiometers labeled in CAPITALS are front panel controls; those labeled in lower case are trimpot adjustments on the circuit board inside the radio.

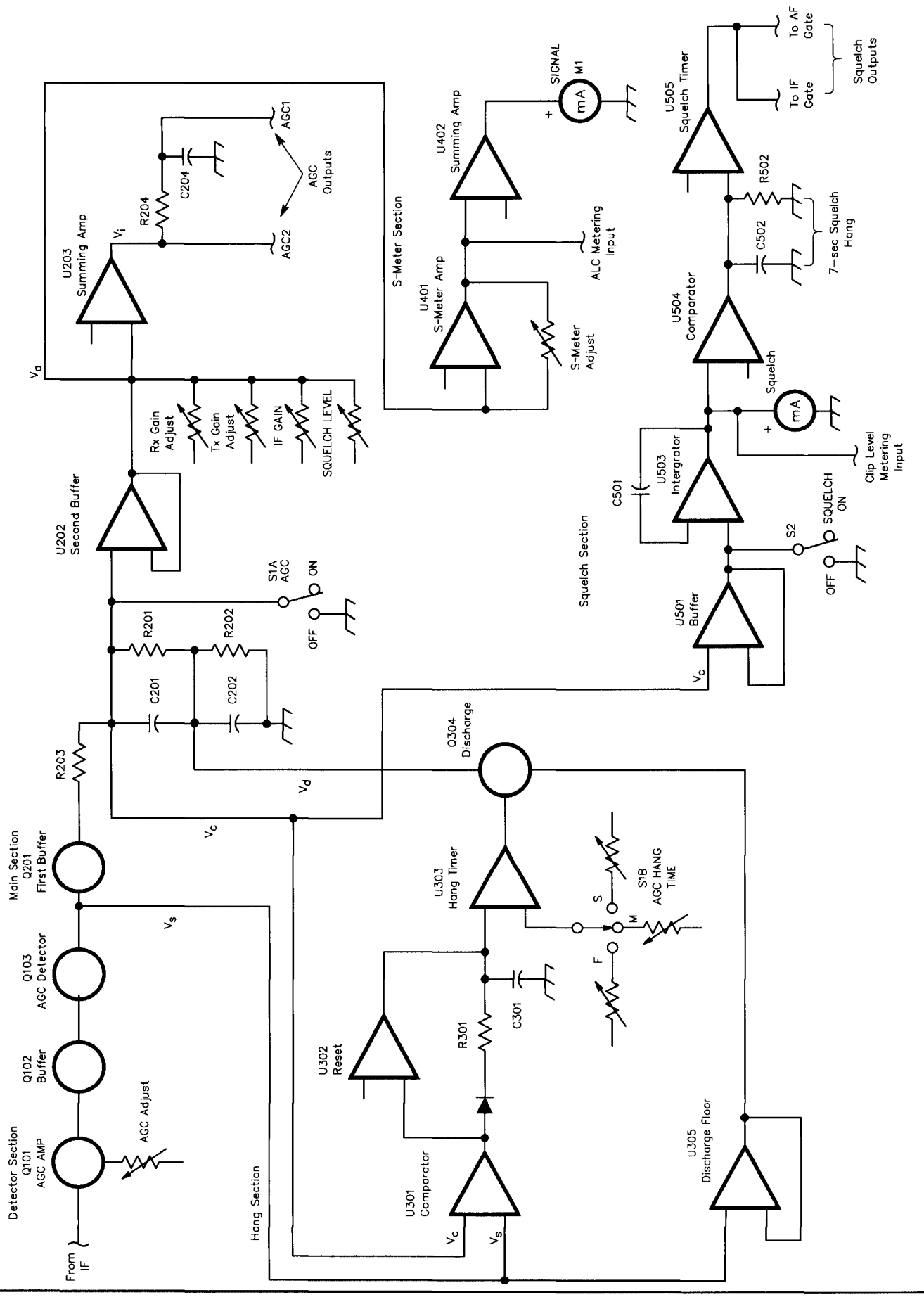
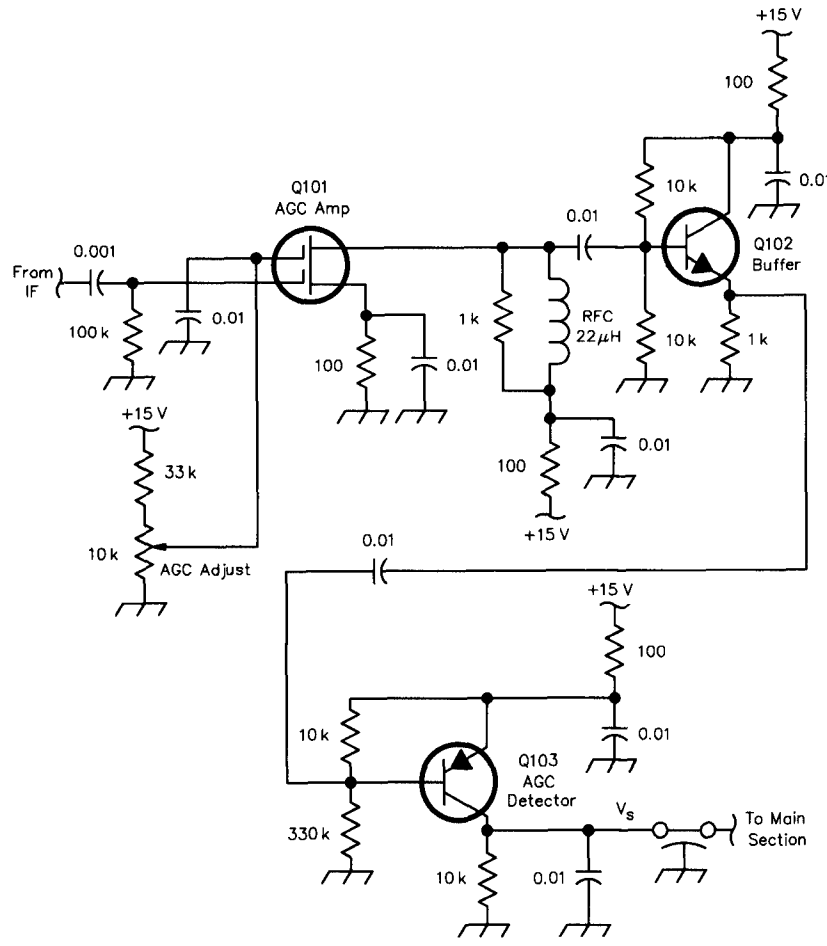

From IF
Detector Section
Q101
AGC AMP
Q102
Buffer
Q103
AGC Detector
Main Section
Q201
First Buffer
AGC Adjust
R203
C201
C202
R201
R202
S1A
AGC
ON
OFF
U202
Second Buffer
Rx Gain Adjust
Tx Gain Adjust
IF GAIN
SQUELCH LEVEL
U203
Summing Amp
R204
C204
AGC1
AGC2
AGC Outputs
Hang Section
U301
Comparator
U302
Reset
R301
C301
U303
Hang Timer
S1B
AGC HANG TIME
Q304
Discharge
U305
Discharge Floor
S-Meter Section
U401
S-Meter Amp
S-Meter Adjust
U402
Summing Amp
SIGNAL
M1
ALC Metering Input
Squelch Section
C501
U503
Intergrator
S2
SQUELCH ON
OFF
U501
Buffer
U504
Comparator
Squelch
Clip Level Metering Input
R502
C502
7-sec Squelch Hang
U505
Squelch Timer
To AF Gate
To IF Gate
Squelch Outputs
V_a
V_c
V_d
V_s
V_i

Fig 6—Detector section schematic diagram. This section is located on the IF board, while the remainder of the AGC system is on the AGC board. Each board in the transceiver is mounted in a separate copper box; the feed-through capacitors, 0.001 μF, indicate where leads leave the box. In addition to the feed-throughs, each lead is filtered outside each box, using a π-section filter consisting of a 1-mH RFC and two 0.1-μF monolithic ceramic bypass capacitors. Almost all components are available from Digi-Key Corp, Box 677, Thief River Falls, MN 56701-0677, tel: 800-344-4539, 218-681-6674; fax: 218-681-3880. All resistors are 1/4-W, 5% carbon-film types. The diodes are small-signal types, such as 1N4148. The 1-μF capacitors are monolithic ceramic types; those of higher capacity are 20-V electrolytics, tantalum if 10 μF or less. The bipolar transistors may be any small-signal types, such as the 2N4400 (NPN) and 2N4402 (PNP). The MOSFETs used here are type 3N140, but any small-signal RF-type dual-gate MOSFET may be used; they all have roughly the same characteristics at IF frequencies.

Since these circuits are intended for incorporation into other transceiver designs rather than for exact duplication, pin-outs and package arrangements are not given. The op amps are of two types, the regular LM324 op amp and the open-collector comparator LM339. In this circuit all these have the upper supply connection from the +15-V rail, and the LM339 types all have ground as the lower rail. But the LM324 types are used in two different ways; either with the lower supply connection from the –15-V rail or at ground. Although it is conventional to label the supply rails for only one of a package of four op amps, here all rail connections are labeled; this shows the functioning of each device most conveniently. The LM339 types are indicated by a black dot at the output. The stages labeled "comparator" may be either regular op amps used as comparators or actually the open-collector types commonly called "comparators."



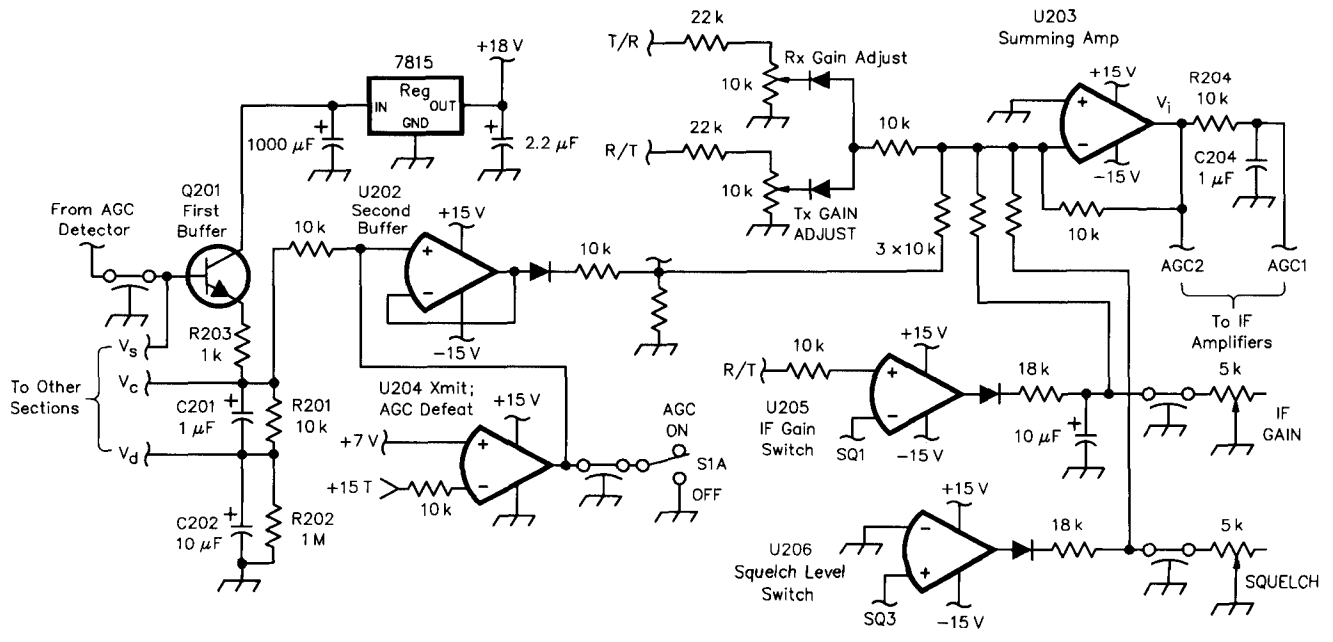


Fig 7—Main section schematic diagram. For schematic conventions used here, see the caption to Fig 6.

there will be AGC voltage available at even the weakest signal levels. The bipolar detector provides the dc signal that is to be processed by the rest of the AGC system.

The main section includes a bipolar buffer for current gain, the main timing capacitors C201 and C202, panel IF GAIN provision, trimpot IF gain adjustment for receive and transmit, panel SQUELCH LEVEL control, and the dual attack timing circuit feeding AGC voltage to the two separate portions of the IF amplifier chain.

The hang section provides three different hang times, set by trimpots and selected by a panel switch. A comparator compares the AGC detector dc level V_s with the level V_c at the main timing capacitors, so that hang timing does not begin until the signal level drops.[1] Further, a voltage follower provides a floor to a bipolar discharge transistor, so discharge proceeds only down to the present signal level.

The S-meter section provides signal level read-out in actual dB. There is no irksome "S-meter zero" adjustment. The S-meter also reads transmitter ALC voltage.

The squelch section is an adaptation of the integrating squelch circuit previously described in *QST*.[2] The previous design, an outboard unit designed for insertion in the speaker line, dealt with receiver audio. Best performance required turning the receiver AGC off and very careful adjustment of the RF and AF gain controls. This was not so bad in itself, and sensing 50-MHz F_2 DX signals less than 1 dB above the noise made this well worth the effort. But switching back and forth to operating mode was rather tedious.

The squelch system used now is built into the transceiver and works off the AGC system. This has facilitated a number of improvements. A panel switch turns on the squelch; this mutes the audio, defeats the IF GAIN control and activates the panel SQUELCH LEVEL control in its place. This latter is set to hold the IF strip just below the AGC threshold. The integrator op amp is biased at just a few millivolts, so any signal that produces a bit of AGC voltage begins to charge the integrator capacitor. When the squelch opens, the AGC is fully functioning. Compared with the older method, with the AGC off, it is easy to imagine what a great advantage this is when a local rock-crusher comes on the calling frequency.

[1]Notes appear on page 22.

Another improvement in the squelch circuit is a fixed 7-second hang. The old method did provide some hang time because the integrator capacitor would charge beyond the threshold, and then slowly decay to the threshold, before the squelch would drop out. But this action depended on the strength and duration of the received signal.

A final improvement is a squelch discharge circuit. While you are fussing with the SQUELCH LEVEL setting, flicking the squelch switch off and on will discharge the integrator capacitor and the squelch hang capacitor imme-

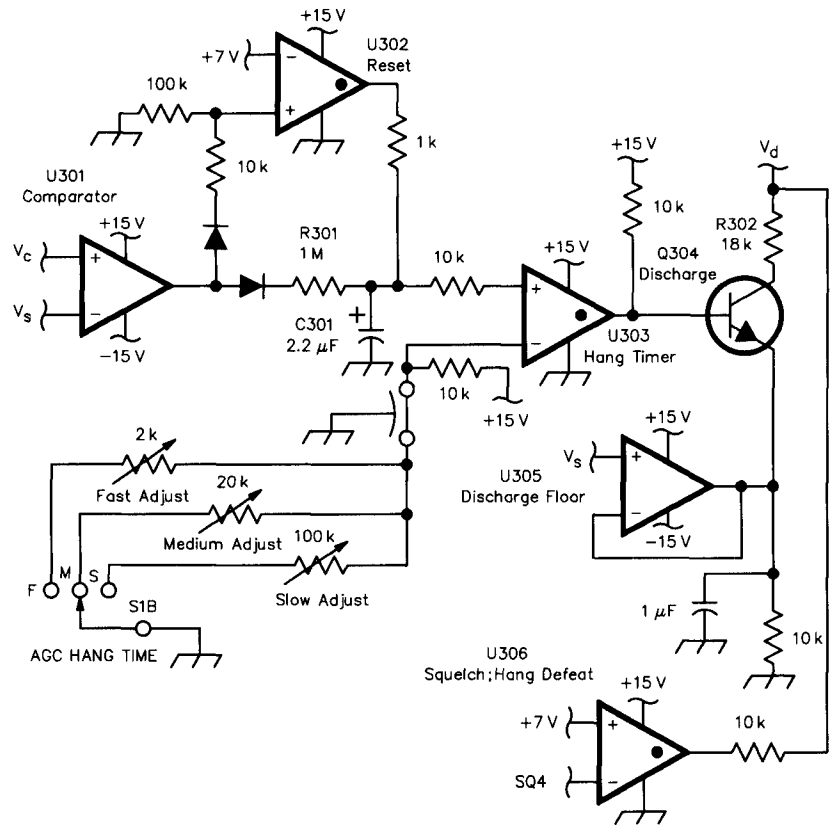


Fig 8—Hang section schematic diagram. For schematic conventions used here, see the caption to Fig 6.

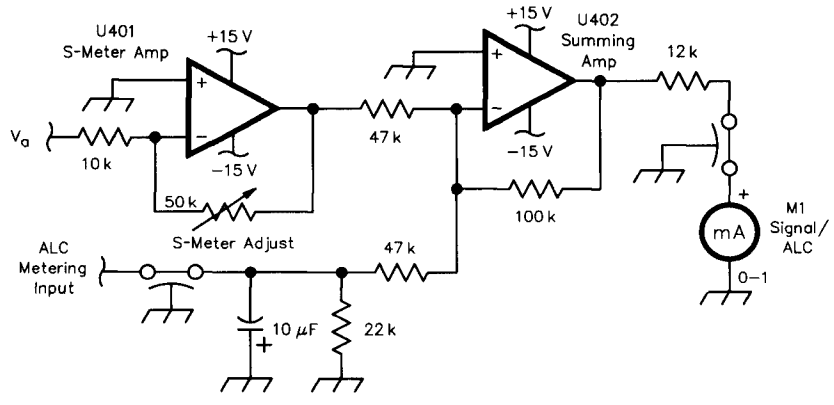
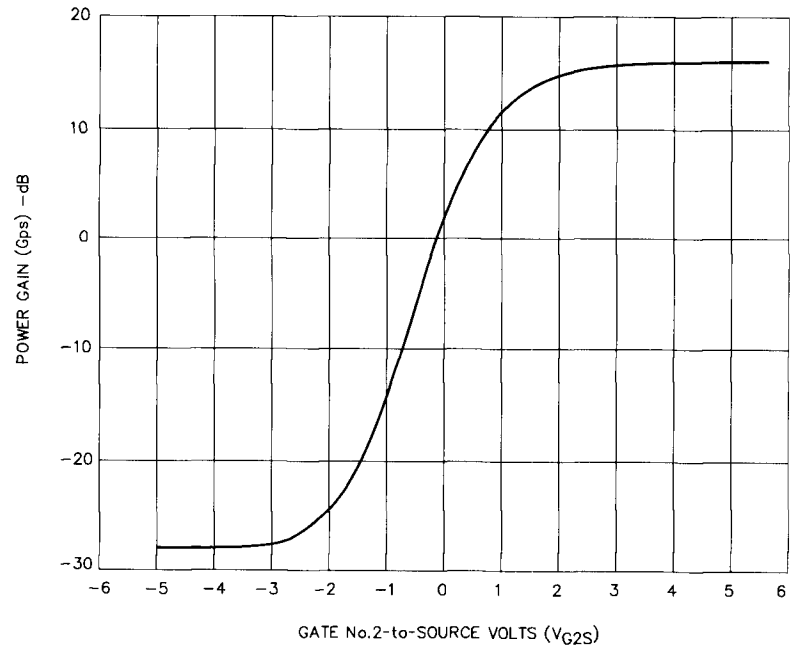


Fig 9—S-meter section schematic diagram. For schematic conventions used here, see the caption to Fig 6.

diately, without waiting 7 seconds.

Detector Section

The schematic of the detector section is shown in Fig 6. Q101 is a simple MOSFET amplifier; the trimpot adjusts the gain of this stage and, in effect, sets the output level of the IF strip. Because of the high gain of the AGC amps, the AGC characteristic is almost perfectly flat, so the question is not "how much AGC voltage do we get?" but simply "what level is required at the input to Q101 to turn on the AGC detector Q103?" The IF output level, at the input to Q101 and at the product detector, is 100 mV P-P (–16 dBm). The Q101 stage receives the IF signal through a buffer that is switched off during transmission. The buffer Q102 is an emitter-follower stage that provides signal current for the AGC detector without excessive loading of the Q101 drain circuit. The PNP detector Q103 is forward biased to V_{be} =0.44 V, just below the conduction point, giving it good sensitivity.



Common-Source Circuit, Gate No.1 Input
Ambient Temperature (T_A) = 25°C
Frequency (f) = 200 MHz
Gate No.1-Votage (V_{G1S})
is Adjusted for I_D = 8 ma
when V_{G2S} = 4 V
Gate No.2 at AC Ground Potential

Fig 10—MOSFET gain versus control gate voltage curve.

Main Section

In the main section, shown in Fig 7, Q201 is another emitter-follower, providing charging current for the timing capacitors C201 and C202. The fast attack and release times, set by R203-C201-R201, are 1 ms and 10 ms, respectively. The hang capacitor C202 charges more slowly. Thus the hang circuit functions only with real signals, not short noise pulses. This prevents AGC hang-up during static conditions. The buffer Q201, with the timing capacitors C201 and C202, form the heart of the system.

The supply voltage for Q201, and thus the charging current for the timing capacitors, is provided by a separate 7815 voltage regulator. In

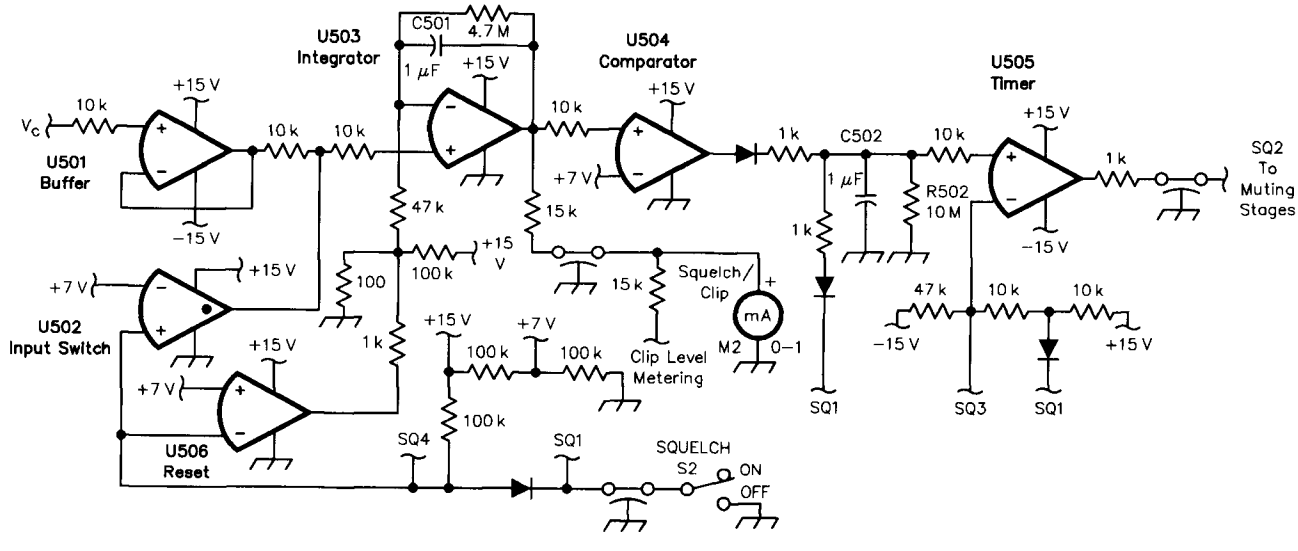


Fig 11—Squelch section schematic diagram. For schematic conventions used here, see the caption to Fig 6.

some receivers, pops, clicks, audio distortion and erratic behavior with signals at the edge of sharp IF filters are caused by transient pulses in the dc supply lines. The circuit that charges the AGC capacitors can cause some of this. The problem is avoided here with the separate regulator and its large filter capacitor. In effect, the initial leading-edge charging current for the timing capacitors comes from this filter capacitor.

To further avoid this and other transient problems in the receiver, the power supply on the rear panel produces regulated +18 and −18-V lines fed to each circuit board. Each board then has on-card regulators for +15 and −15 V. The IF board also has the separate AGC regulator for isolation of Q201, as mentioned. And the power supply also has a separate +18-V supply for the discrete class-AB1 audio output stage, since transients from this stage could otherwise find their way into other circuits. The 5-V supply for the logic circuits and the counter is also separate. These details are mentioned here because providing a pop-free AGC system is not enough; the rest of the radio must also be clean. Transients have even been found to leak between separate power supply circuits run from separate windings on a single transformer. Thus this radio uses four separate small transformers for its four supplies. These comments apply to the basic 39-40 MHz radio shown in Fig 1. The 200-W MF/HF front-end section and the VHF CW/SSB weak-signal front-end sections and driver amplifiers are all separate units.

In this section we identify and designate three distinct system lines. The first two carry dc signals that are sent to other parts of the AGC system. The V_s line carries the voltage developed at the AGC detector and thus represents the actual *signal* level in the IF system. The V_c line carries the voltage at the timing capacitors; it differs from V_s because of the drop in Q201 and the action of the capacitors. The discharge line V_d is used to discharge the hang capacitor C202 at the end of the hang period.

Op amp U202 is a voltage-follower buffer that isolates the timing capacitors, so they are not loaded by the rest of the circuit. The voltage V_c is reduced here to a level we'll call V_a, which is fed to the rest of the AGC system.

The next buffer, U203, the last in the main path of this section, is of a very useful type—an inverting summing amplifier. The key features of this type of amplifier are the grounded noninverting input and the inverse feedback. This results in what is called

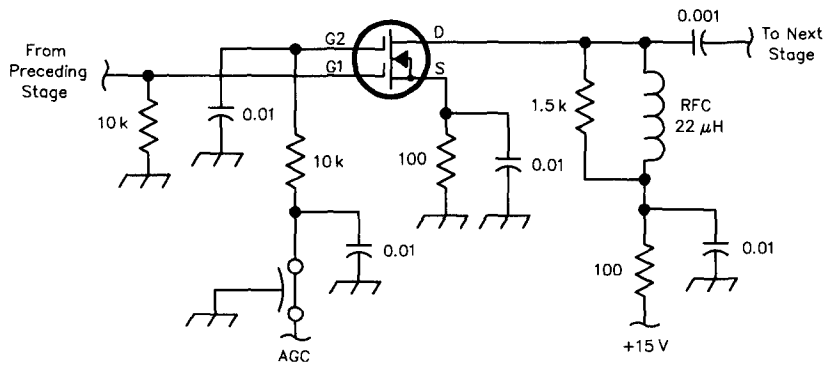


Fig 12—MOSFET IF amplifier schematic diagram of a typical 9-MHz stage. The MOSFETs used here are type 3N140, but any small-signal RF-type dual-gate MOSFET may be used. Each stage in the IF strip is built into its own shielded copper compartment.

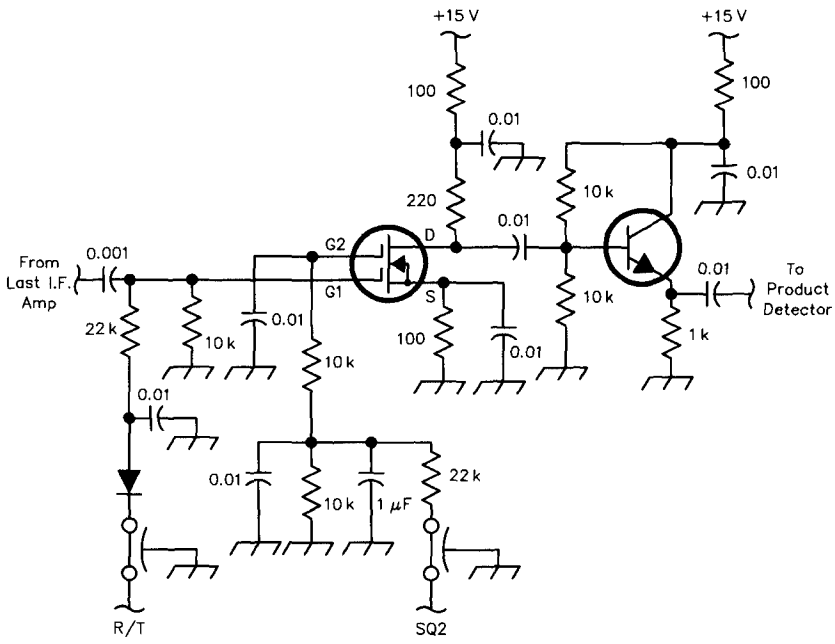


Fig 13—MOSFET IF squelch gate schematic diagram.

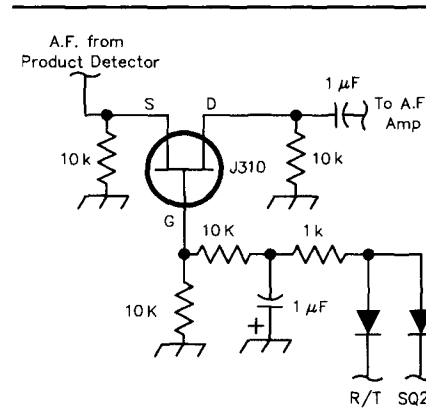


Fig 14—JFET AF squelch gate schematic diagram.

a *virtual ground* at the inverting input. There are five separate inputs to this buffer circuit, but because of the virtual ground, none of these inputs affects the others. Here the stage gain is set at −1, although an inverting summing amplifier may be set up for any negative gain desired. The result is that the op-amp output is the (inverted) sum of all five inputs. Because the IF strip with its crystal filters is also used for SSB transmissions, the T/R and R/T lines (−15/0 V and 0/−15 V in receive and transmit, respectively) are used to switch the receive and transmit IF gain adjustment trimpots.

While transmitting, op amp U204 further disables the AGC system and keeps the timing capacitors discharged, and U205 disables the panel IF GAIN control. During normal receive conditions, the receiver gain trimpot, the panel IF GAIN control and the AGC voltage V_a all sum to produce the control voltage, called V_i, for the IF strip. When the squelch circuit is enabled, the panel IF GAIN control is disabled by U205, and the panel SQUELCH LEVEL control is enabled by U206.

The IF strip uses dual-gate MOSFETs; the AGC lines connect to the gain-control gates. The no-signal AGC line V_i level is nominally +2 V; this is set by the receiver gain trimpot. The AGC voltage V_a from U202 runs nominally from 0 to +4 V, increasing with increasing signal. Since U203 is inverting, V_a subtracts from the +2 V, giving us a +2 to −2-V range for V_i, which will take the MOSFETs from near full gain to near cut-off. These ranges represent the design maximums, for fullest possible gain and fullest AGC control. In my six-stage IF strip the adjustments result in V_i at +1.4 V for no signal and −0.6 V for 120-dB gain reduction. The overall IF strip gain, including filters and pads, is 100 dB.

It is finally at the output of U203 that the dual-attack timing circuit appears. Easily overlooked, though crucial, it consists merely of R204-C204, delaying the AGC1 voltage to the first IF section, IF1. This prevents overshoot, while the nearly instantaneous AGC2 voltage is applied to IF2, keeping pops and clicks from initial dits and syllables out of the headphones.

Hang Section

In the hang circuit, shown in Fig 8, U301 compares the signal level V_s with the capacitor level V_c. Only when the signal drops or disappears, when V_s drops below V_c, does U301 begin to charge the hang timing capacitor C301 to begin the hang period. Note that C301 is merely a timing capacitor controlling the length of the hang period, not the AGC voltage itself; the voltage on C301 increases as the timing period proceeds. Comparator U303 is the hang timer; when the voltage on C301 reaches the level set by one of the fast, medium or slow trimpots, U303 turns on the discharge transistor Q304. Note that the trimpots merely set a dc voltage reference level; they are not actually in the R301-C301 timing circuit. Comparator U302 has a special purpose. Consider the circuit as described so far without U302. Suppose there is a pause in a received transmission, and C301 has already partly charged, say half-way to the set level. A fraction of a second later the transmission resumes and then ends. C301, with no significant load, is still at the half-way point and continues to charge from there. The result is a shortened hang period. U302 corrects this problem. As soon as V_s exceeds V_c, U302 discharges C301, so it is ready to begin the next hang period anew. (The usual way to solve this problem, letting U301 discharge C301 through a diode, will not work easily here. The diode drop is too high in comparison with the low reference level set by the fast trimpot.)

At the end of the hang period, the timer U303 turns on the discharge transistor Q304, which discharges the V_d line through R302. The recovery period is set by C202-R302. The discharge line is not brought to zero, however. After all, only the loudest signal has dropped out; weaker signals may still be in the passband. Dropping the AGC line to 0 at this time could result in AGC pumping (alternating louder receiver output, then over-correction and insufficient output). Voltage follower U305 takes care of this. Without loading the V_s line, it provides a solid floor for discharge transistor Q304, at the V_s level. For example, if an S9 signal disappears and leaves an S5 signal in the passband, after the hang period the AGC line will drop precisely to the S5 level.

S-meter Section

In the S-meter section, shown in Fig 9, U401 senses the AGC voltage V_a from U202 rather than from one of the AGC lines to the IF strip. Thus, the S-meter responds only to signals, and is not affected by the panel IF GAIN or SQUELCH LEVEL controls, or the receive and transmit gain trimpot settings. This method has a great advantage in operating convenience over RF gain controls that push the S-meter up: it

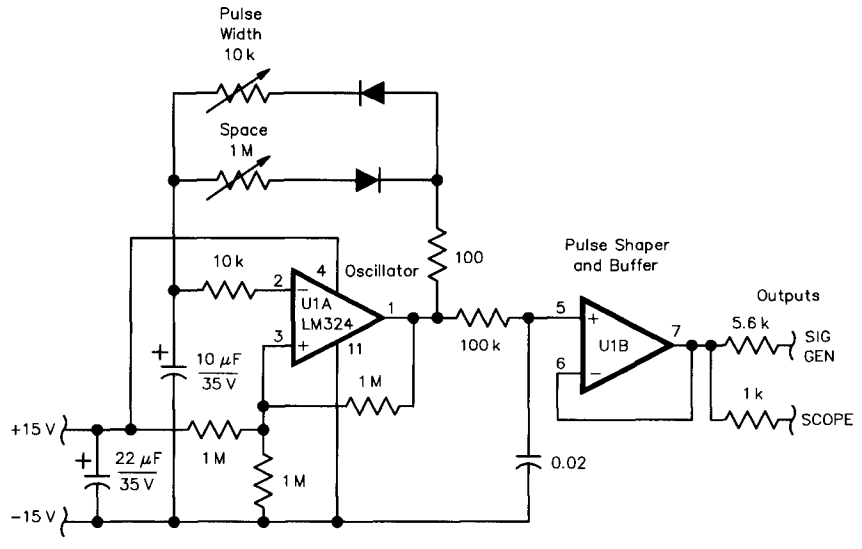


Fig 15—AGC test pulse generator schematic diagram. The 0.02-μF timing capacitor is an accurate, stable type, such as mylar or polypropylene.

allows the S-meter to indicate the signal level relative to the IF gain setting without need for the operator to remember where it was set. It also allows the AGC threshold to be set at the noise level, if desired, with S-meter monitoring of the setting, although there is no need to employ this method. The front-end sections have antenna attenuators and IF output level controls to allow adjustment for optimum gain distribution and dynamic range.

At op amp U401, the trimpot adjusts the gain so the actual 120-dB range of the AGC system produces a voltage of 0 to –6 at the U401 output. The inverting summing amplifier U402 doubles and inverts this, resulting in 0 to +12 V for the S-meter circuit: the 12-kΩ resistor then drives the 1-mA meter M1. With a maximum possible op-amp output of +14 V, this method limits meter overdrive, under any unusual conditions, to 17%.

The MOSFET IF amplifiers are operated in a fairly straight portion of their logarithmic gain curve (see Fig 10). This results in an S-meter that reads very close to actual dB. The MOSFET curve has a very pronounced knee near full gain; if we ran full gain at no signal, S1 might be mid-scale on the S-meter!

The circuit for op amp U402, with virtual ground, causes no interaction between the two input signals: signal level in receive or ALC level in transmit. In transmit the meter reads ALC voltage from the separate front end sections, the station driver amplifiers or the high-power amplifiers. All these are designed to produce –6 V for full-scale meter indication at 20 dB of ALC compression. (In operation about 2 dB is used.) Actual ALC control takes place in the separate front-end sections at signal-frequency stages, but meter read-out is on the main radio panel (Fig 1) for convenience.

Squelch Section

Adapting the original integrating squelch circuit to a squelch system internal to the receiver allowed a great improvement in operating convenience.[2] Here AGC levels are used rather than receiver audio output.

The schematic of the squelch section is shown in Fig 11. Op amp U501 is a voltage follower buffer, which relays V_c to the squelch circuit without loading the timing capacitors. The comparator U502 acts merely as a switch keeping AGC voltage off the integrator when the squelch is off.

The integrator U503, comparator U504 and the metering circuit all function as described in Note 2. The panel SQUELCH LEVEL control, shown in the main AGC section, is set to hold the IF strip gain just below the AGC threshold. When a signal appears, the developed AGC voltage $V_{c'}$, buffered by U501, causes the integrator capacitor C501 to begin charging. When the voltage at the output of integrator U503 reaches the 7-V reference level of comparator U504, the comparator output goes high, quickly charging the squelch hang capacitor C502 fully. In turn, the output of timer U505 goes high. The resulting voltage, called SQ2, turns on a MOSFET muting buffer before the product detector, and a JFET muting switch in the receiver audio circuit; these are described below. The R502-C502 circuit provides the seven-second squelch hang time.

The squelch circuit is enabled by opening switch S2. This accomplishes several things. The voltage, SQ3, at the inverting input to timer U505 is switched from –3 V, for normal receiver operation, to +6 V for squelch functioning. This same SQ3 is also used with U206 in the main section to enable the panel SQUELCH LEVEL control. The squelch switch, S2, with U205, disables the panel IF GAIN control. Switch S2 also controls the squelch input switch U502 and the hang defeat switch U306, in the hang section. When the squelch is turned off, S2 discharges the squelch hang capacitor C502 and, using U506, resets the integrator. This elaborate squelch on/off switching is required for convenience in setting the SQUELCH LEVEL control because of the time hysteresis action of the integrating squelch circuit, as described in Note 2, and because of the hang action now incorporated.[3] The integrator capacitor voltage is monitored by the squelch meter, M2. The squelch threshold is about midscale on the meter. When transmitting SSB, this meter monitors the RF speech clipping level. No switching of meter function is required, nor is a summing op amp needed. For clipping level, the meter is driven similarly by an op amp in the transmitter section of the radio, which is disabled during receive. The driving circuit not in use merely presents a 15-kΩ load to the meter, which means nothing to a 100-Ω, 1-mA meter.

Associated Circuits

The MOSFET IF amplifiers controlled by this AGC system have no unusual features; the schematic of a typical 9-MHz stage is shown in Fig 12. Gain control is by means of gate 2, known as the "gain control gate." A typical curve of gain versus control gate voltage is shown in Fig 10, taken from the RCA 3N140 spec sheet. Notice the pronounced upper and lower knees. With the range of control voltage used, operation is in a fairly straight portion of the curve; this results in a nearly linear voltage-versus-dB relationship for easy S-meter calibration. The MOSFETs used here are type 3N140, but any small-signal RF-type dual-gate MOSFET may be used; they all have roughly the same characteristics at IF frequencies.

After the six gain-controlled stages, and before the product detector, a MOSFET buffer is used as a squelch gate, as shown in Fig 13. The squelch circuit produces a +15/–15 control voltage, SQ2; the voltage divider at the buffer reduces this to +4/–4 V, yielding full-gain/cut-off for gate 2 of the MOSFET. This buffer is also used for T/R muting using gate 1. With the resistive load in the drain circuit, this MOSFET circuit is convenient for unity-gain buffering and switching. The value of the drain resistor may be varied somewhat for small gain adjustments. Another squelch and T/R muting gate is in the audio section; it uses a JFET, as shown in Fig 14.

An AGC Test Device

Although a QRP transmitter can be used to generate the initial dits required for testing an AGC circuit, it was much more convenient to use a special pulse generator with a signal generator. A keyer producing a string of dits cannot be used. We need to monitor the AGC action on the *first* dit, then allow the AGC system to recover fully, and the receiver to resume maximum gain, before confronting the receiver with the next dit.

The pulse generator will produce spaced dits, with both the dit width and the spacing adjustable. It is used to select the proper values of R204-C204. The make/break timing for the pulse is 2 ms, soft enough so that any click heard, or seen on the scope, would be receiver-generated rather than the

actual signal. But too-soft timing here would make it *too easy* for the AGC system. The generator can be adjusted for pulses up to 100 ms, with spaces up to 10 s. I find that settings for 40-ms pulses (corresponding to dits at 30 wpm), spaced two seconds, work well.

The schematic is shown in Fig 15. The pulse generator is used to control an HP8640B signal generator. The PULSE input to the generator cannot be used because in this mode the generator produces very fast rise and fall times, merely triggered by the pulse input. The generator output does follow the level at the AM input, however; we use the AM-dc input. (This supports the idea that CW is really a form of AM.) The SIG GEN output of the pulse generator is configured to produce ±1 V at the 600-Ω AM-dc input to the HP generator, which has a control for further adjustment. The SCOPE output of the pulse generator is used to monitor the pulse width and space time. The two scope traces are then variously used to monitor the actual signal at points in the IF strip, the two AGC voltages and the receiver AF output. The pulse generator SCOPE output is used for triggering at the *end* of one pulse, using the delayed sweep to monitor the next complete pulse.

The pulse generator is powered by a ±15-V bench supply. There is no ground connection to the pulse generator; the ground reference is the ground connection at the bench supply.

The CW waveform shaping is obtained with the 100-kΩ, 0.02-μF timing circuit. The 2-ms timing produces a fairly hard CW keying waveform, but this is realistic for nearby signals heard in the DX bands. To distinguish AGC clicks from the natural sound of sharp CW, turn off the AGC and use the RF gain to hear the actual signal.

Acknowledgments

The idea for the hang AGC circuit was found in the Signal/One CX7 transceiver (1969). The AGC detector, first buffer, timing capacitors and discharge transistor (including the floor idea) are essentially as found in the CX7. The CX7 AGC system used 10 transistors and no op amps. The idea for a dual-attack AGC to eliminate pops, clicks, and overshoot, was found in the Drake 2-B receiver (1958).

Summary

Ham radio operation places special demands on a receiver. One of the most difficult requirements to meet is adequate AGC performance. Ironically, at times we really don't need any AGC for the S1 DX signals we want to hear; we need it to keep the domestic stations, whom we'd rather not hear at all, from cracking our skulls. This AGC system deals with the attack, hang and recovery problems, and eliminates pops, clicks and overshoot.

Notes

[1]The term *comparator* is ambiguous. Referring to devices, it means an op amp with an open collector output, such as the LM339. Referring to circuit function, however, the term may refer to such a comparator, or, as in this instance, an ordinary op amp used to compare levels.

[2]Mandelkern, Mark, "A Sensitive Integrating Squelch Circuit," *QST*, August 1988, pp 27-29.

[3]One design requirement was to provide switching of the squelch circuit with a single wire to the front panel. Wire harness overload was perhaps the toughest problem that arose in the three years of building this transceiver. This also explains the circuits used for IF GAIN, SQUELCH LEVEL and AGC HANG TIME. □□

Digital Communications

By Harold E. Price, NK6K

Recharging the Batteries

No, this isn't a column on the facts and fiction of "NiCad Memory." We're talking about *my* batteries. As anyone who writes a column will tell you, it takes longer than you'd think. Pressures of work and several upcoming satellite projects, including P3D Rudak, have led to a lack of on-air time—and a lack of project time. Rather than let the "Digital Communications" column lose relevancy, I'm turning in my columnist's credentials and letting someone else take the lead. But before I do, there are some loose ends that need to be tied up.

I had several requests for contact information on the quadifilar antennas I mentioned in a previous column. They were from Satellite Data Systems, PO Box 219, Cleveland, MN 56017, tel: (507) 931-4849. The Ham Radio Outlet home page, with searchable price list (I still love that) has moved to http://www.hamradio.com.

The BASIC Stamp people have come up with a follow-on product that is now available: more memory, more I/O lines, more power, more built in functions—and more money.

In the area of tools, Intel has a product called "Data on Demand." This two-CD-ROM set contains the contents, including graphics, of all of Intel's product data books. This is well worth the price—free, or at least it was a few months ago.

For my last act here with the column, I present a report on the AMSAT general meeting held in Orlando, written by Steve Ford, WB8IMY. Enjoy.

Phase 3D Showcase in Orlando

It's easy to understand why Phase 3D was the star of the recent AMSAT-NA Space Symposium in Orlando, Florida. Depending on the launch schedule, this may have been the last opportunity for many amateurs to see the satellite before it goes to orbit.

At the meeting, Dr Karl Meinzer, DJ4ZC, AMSAT-DL President and Phase 3D International Satellite Project Leader, announced the signing of a contract with the European Space Agency (ESA) to launch the satellite. According to the agreement, Phase 3D has a primary launch opportunity on ESA's new Ariane V rocket in September 1996. If this is not possible, ESA has committed to orbit Phase 3D on an Ariane *IV* booster by mid 1997.

Ariane V is a more powerful booster and will lift the bird to a high transition orbit. However, the final-stage engine delivers a powerful kick when it ignites. Although Phase 3D is designed to withstand the anticipated G forces, the risk of damage is somewhat greater with the big rocket. Ariane IV offers a much "gentler" ride but will not take Phase 3D as high. As a result, the satellite will require an extra kick-motor burn to maneuver into a stable orbit. The cost is higher fuel consumption.

The launch delay gives the Phase 3D teams some much-needed breathing room. They've been working frantically to stay on schedule, and there was some concern that portions of the project—such as the GPS receiver

5949 Pudding Stone Lane
Bethel Park, PA 15102
email: nk6k@amsat.org

system—may not make the launch date. The extra months will go a long way to ensure that everyone has plenty of time to meet the deadline.

Phase 3D received a big financial boost when ARRL New England Director Bill Burden, WB1BRE, presented AMSAT-NA with a check for $305,000 at the Symposium banquet. The check represented the contributions of ARRL members, matched dollar-for-dollar by the League. (Although the solicitation has been fully subscribed, ARRL will continue to match contributions through the end of 1995.)

Integrated Housekeeping Unit

Lyle Johnson, WA7GXD, and Chuck Green, NØADI, updated the attendees on progress with Phase 3D's Integrated Housekeeping Unit, or IHU. Based on the humble COSMAC 1802 microprocessor, the IHU is responsible for the overall management of the most complex amateur spacecraft ever assembled.

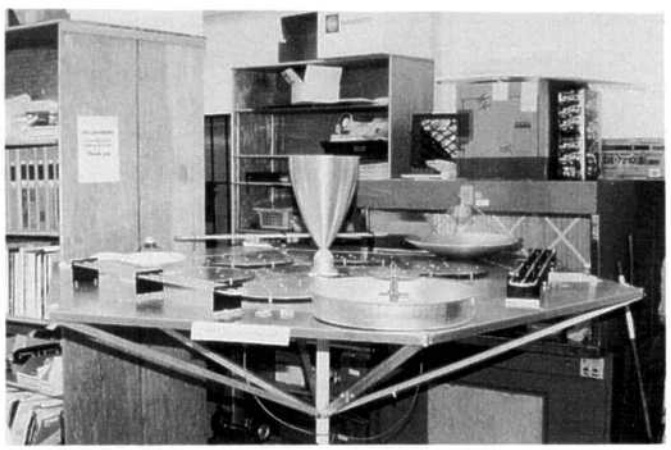
The 1802 microprocessor actually represents 1970's technology and is in some ways typical of early 8-bit microprocessors. It has a 64-kbyte memory addressing capability and deals with 8-bit quantities very well. More modern features include an internal array of sixteen 16-bit general-purpose registers and a direct-memory access (DMA) mode. The downside is that the COSMAC 1802 runs rather slowly.

So why use such "ancient" technology in an advanced satellite? Reliability was an overriding concern. The 1802 has proven itself in OSCARs 10 and 13, and a number of radiation-hardened 1802 chips are still available. Since the fate of the Phase-3D mission rests on the IHU, there is an obvious reluctance to switch to a new, unproven design.

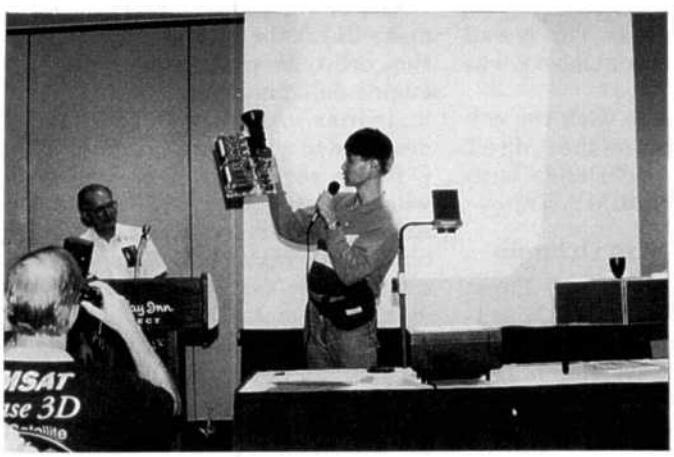
The resulting Phase-3D IHU still differs substantially from the one used for OSCARs 10 and 13:

- memory space is double that of OSCAR 13's IHU;
- a four-layer PC board with reduced line geometry, similar to those employed on the Microsats, is used;
- the previously separate CPU and memory boards have been combined into a single board in the Phase-3D IHU;
- the command decoder has been integrated into the IHU;
- a serial bus is integrated into the IHU for communicating with secondary experiments; and

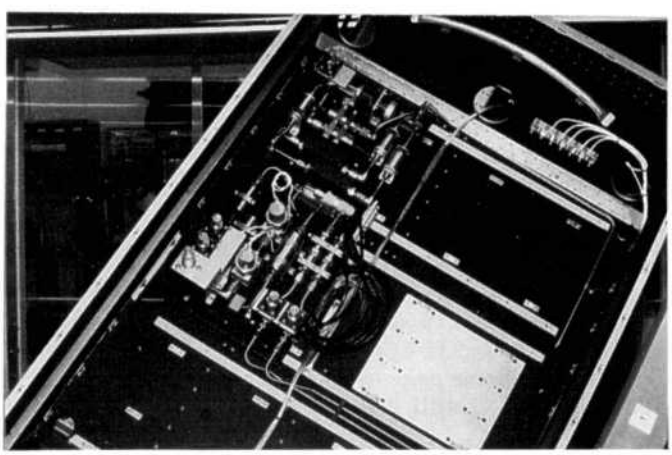
Chuck Green, NØADI, displays the engineering flight model of the Phase-3D IHU.



The full-scale Phase 3D antenna test mock-up. The cone in the center represents the engine nozzle.



Hiroyuki Ohata, JM3MAJ, describes the SCOPE color imaging module for Phase 3D. This flight model has already been test fitted within the satellite.



A close-up view of the Propellant Flow Assembly (PFA) installed in Phase 3D. The PFA regulates the flow of propellants to the kick motor and the arc-jet positioning motor.

- PC board-mounted connectors are used, completely eliminating wiring harnesses within the IHU.

As with earlier units, the Phase-3D IHU will send telemetry at 400 bit/s using differential binary phase-shift keying. This means those telemetry decoders presently used to monitor the status of OSCAR 13 will also work with Phase 3D.

GPS Receiver System

Although not critical to the success of the Phase-3D mission, the GPS payload module has attracted quite a bit of interest. The goal is to allow the satellite to generate its own orbital elements based on position data obtained on the fly. The data would subsequently be available as telemetry.

The idea was first proposed by Tom Clark, W3IWI, a few years ago. In 1993, a group of interested individuals met to get the project underway. At this year's AMSAT symposium, Tom Clark and Bdale Garbee, N3EUA, presented a summary of their progress.

The project is even more ambitious than it seems. To meet the peculiar requirements of Phase 3D, the team had to design a new receiver and software set. As of this date, the prototype CPU board has been tested and a revision is underway. The team is hopeful that this revision will become the Phase-3D flight model.

Low-gain patch antennas are in hand and appear to work well. High-gain "helibowl" antennas (using a $1.98 steel salad bowl as a parabolic reflector!) have tested to specifications. Flight models come next.

Speaking of Antennas...

Most of the Phase-3D antennas have been fabricated and tested on a full-scale antenna mockup at the Orlando integration facility. Squeezing so many antennas into a finite space was a challenge, but the results are very encouraging. The assembly team actually worked OSCAR 13 on modes B and S by using the antennas on the mock-up!

Summary

It's clear from the evidence in Orlando that Phase 3D is coming together on schedule. Fabrication of the wiring harness is under way, and the propulsion plumbing system is complete. Several RF packages are ready and others (such as the 24-GHz transmitter) are nearing completion. Several PC boards for the RUDAK-U module are finished, and all component parts are in hand.

Whenever the ESA decides which rocket Phase 3D will occupy, the satellite will be ready! □□

Conference Proceedings

The following Conference Proceedings are now available from ARRL:

14th ARRL Digital Communications Conference Proceedings; cost $12 plus shipping; ISBN: 0-87259-526-9; ARRL Order Number: 5269

Availability of Seventy 9600 Baud Packet Channels on Two Meters, Bob Bruninga, WB4APR

The WA4DSY 56 Kilobaud RF Modem, Dale A. Heatherington, WA4DSY

Extended Sequence Number (Modulo-128) Option for AX.25, Rob Janssen, PE1CHL

DSP-93 Update: The TAPR/AMSAT Joint DSP Project, Greg Jones, WD5IVD, Bob Stricklin, N5BRG, and Robert Diersing, N5AHD

Introduction to Programming the TAPR/AMSAT DSP-93, Ron Parsons, W5RKN, Don Haselwood, K4JPJ, and Bob Stricklin, N5BRG

An Introduction to FlexNet, Gunter Jost, DK7WJ

Convolutional Decoders for Amateur Packet Radio, Phil Karn, KA9Q

Data Radio Standard Test Methods, Burton Lang, VE2BMQ, and Donald Rotolo, N2IRZ

Modeling Some Data Communications functions Using Microsoft Excel 5.0, Thomas C. McDermott, N5EG

Building a Packet Network, Karl Medcalf, WK5M

DAMA—Another Network Solution, Karl Medcalf, WK5M

The Tulsa National Weather Service TexNet Interface Project, Bob Morgan, WB5AOH, and Greg Jones, WD5IVD

An Update on TexNet and the Texas Packet Radio Society, Bob Morgan, WB5AOH, and Greg Jones, WD5IVD

DSP-93 Programming Hints, Frank H. Perkins, Jr., WB5IPM

NETMGR: A Graphical Configurator for ROSE X.25 Packet Switch Networks, William Slack, NX2P, and Donald Rotolo, N2IRZ

Graphical Information Systems and Ham Radio, Keith Sproul, WU2Z

AX.25 Transport Layer Drivers for TCP/IP, Mark Sproul, KB2ICI, and Tim Hayes, N2KBG

The Puget Sound Amateur Radio TCP/IP Network, Steve Stroh, N8GNJ

6PACK—A "Real Time" PC to TNC Protocol, Matthias Welwarsky, DG2FEF

Skimming the Layers, Ken Wickwire, KB1J

Proposed Recommendation for Hierarchical Addressing Protocol, Dave Wolf, WO5H, Greg Jones, WD5IVD, Roy Engehausen, AA4RE, and Hank Oredson, WØRLI

AMSAT Space Symposium Proceedings and Annual Meeting; cost $12 plus shipping; ISBN: 0-87259-535-8; ARRL Order Number: 5358. This book is also available from AMSAT, PO Box 27, Washington, DC 20044.

Welcome to the 1995 AMSAT-NA Space Symposium & Annual Meeting, Bill Tynan, W3XO

Keplerian Element Estimation for Radio Sputnik 15 (RS-15), Ken Ernandes, N2WWD

AMSAT-NA Operations Report '95, Keith Pugh, W5IU

The World Wide Web Amateur Satellite Ground Station, Steven R. Bible, N7HPR

The Phase 3D Integrated Housekeeping Unit, Lyle Johnson, WA7GXD

RUDAK-U, Lyle Johnson, WA7GXD, for the RUDAK Team

DSP-93 Update: The TAPR/AMSAT Joint DSP Project, Greg Jones, WD5IVD, Bob Stricklin, N5BRG, and Robert Diersing, N5AHD

Intruction to Programming the TAPR/AMSAT DSP-93, Ron Parsons, W5RKN, Don Haselwood, K4JPJ, and Bob Stricklin, N5BRG

Mechanical and Thermal Design, Dick Jansson, WD4FAB

Phase 3D Propulsion Systems, Dick Daniels, W4PUJ

Wither the HAMSATs?, Keith Baker, KB1SF

Extending the Lifetime of Scientific Satellites Using AMSAT Techniques, Philip Chien, KC4YER

Phase 3D GPS Receiver Progress Report, Bdale Garbee, N3EUA

Participate in Picosats!, Peter Vekinis

AMSAT Net Via Commercial Satellite, Bruce Paige, KK5DO

Developing and Utilizing Satellite Gateway Nodes: A Sysop's Perspective, Barry A. Baines, WD4ASW

APRtrack, A Program for Determining the Locations of Ground Stations and Spacecraft, Bob Bruninga, WB4APR

MicroSat Ground Station Software for Linux and X-Windows, John Melton, GØORX/N6LYT

Iowa Satellite Project's Spacecraft Systems and Operations Laboratory's Involvement with BREM-SAT, Mark A. McKeown

Shuttle Amateur Radio EXperiment (SAREX) Status 1995, Frank H. Bauer, KA3HDO and Matt Bordelon, KC5BTL

Benbrook Elementary's Experience with the Shuttle Amateur Radio EXperiment, Donna McKinney, N5WOE □□