QEX

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May/June 2008

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A Forum for Communications Experimenters

Issue No. 248

MØMWA presents a computer-controlled tunable bandpass filter (preselector) for use with software defined radios.

ARRL The national association for AMATEUR RADIO
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TOKYO HY-POWER

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The HL-450B has a built-in auto band-select function. It uses a newly developed micro-processor based technology, and works a smooth automatic operation when driven by RF from the radio in either SSB or CW mode. In addition, manual band setting is possible as well. It is designed to be "user friendly".

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- The HL-450B has various protection circuits such as for high antenna SWR, over drive, over current, etc. When any abnormal condition is detected, operation is automatically shut down.
- The large analog power meter is easy to read and the output can always be monitored.

Built-in functions

1. Send / receive switching terminal (hard key)
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3. Output power meter
4. ALC terminal
5. External controller (HRC-60, optional) terminal.

Specifications

Freq. Band:
All HF amateur bands of 3.5 - 28MHz

Operation Mode:
SSB, CW, FM

Output:
SSB (PEP) / CW 400W max.
350W typ., 300W min.

RF Input
50W

DC Power Supply
DC 13.8V 60A max.

Input / Output
50 ohms

Final Transistor
THP - 120 x 4

Cooling System
Forced-air cooling

Input / Output Connector
UHF (SO-239)

Accessories
DC power cord (red / black pair) 6' x1,
Coaxial jumper cable: 2' x1,
Stand-by cable (with RCA plug) 4' x1,
Spare fuses: 30A x4, Instruction manual, warranty card

Dimensions
8.7 x 3.5 x 13 inches (WxHxD)

Weight
Approx. 11lbs.

Option
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Matching DC power supply – HP-450
(Light weight switching mode, 13.8V 60A)

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About the Cover

Juan José de Oñate, MØMWA describes a tunable bandpass filter (preselector) for use with software defined radios. A computer program with graphical user interface provides control of the unit. The preselector covers 1.8 to 30 MHz in five selectable bands.

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The purpose of *QEX* is to:

1) provide a medium for the exchange of ideas and information among Amateur Radio experimenters,

2) document advanced technical work in the Amateur Radio field, and

3) support efforts to advance the state of the Amateur Radio art.

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Larry Wolfgang, WR1B

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Empirical Outlook

Ah, spring! Here in Connecticut, it seems like it's been a long winter, and without much snow to brighten the landscape or lure us out to play. Instead of snow, we've had much rain, making for muddy ground and a "pond" where my back yard and garden are supposed to be! As I write this, a few days into the new season, high temperatures still haven't made it out of the 50s, or at least not on more than two or three occasions. Low temperatures have dipped into the low 20s many mornings, though. Ah, spring. How great it will be to venture out into the warm sunshine!

Of course outdoor activities don't have to mean a lack of ham radio, even if there are many yard chores and other activities to take our attention. I have many antenna-related plans for this spring, and hope to accomplish at least a few of them. An old 80 m dipole should probably be pulled down and the coax connections checked or replaced. Then I have to re-string that antenna around and between a couple of trees (that probably need some pruning) and over a higher branch at the back of my yard. An old limb broke, dropping the support rope so the antenna is a mere 15 feet off the ground at the back end.

Before the leaves come out, I should shoot a new line higher in the tree. That has me wondering about the best way to do that. I normally use a bow and arrow, with a helper to hold a fishing rod and reel. It works well, and is certainly safe in my yard, but always requiring a helper can be a small problem. I've tried the slingshot and attached fishing reel but have been less than satisfied with the results, at least as compared to shooting an arrow. Still, there remains a certain feeling that there must be a better way. When I head out to Scout campouts and other activities, sometimes it isn't as safe to pull out the bow and arrow, either because of the location or the number of Scouts running around "down range."

I've seen the tennis ball slingshot, and thought about how much less alarm I'd create by shooting a tennis ball instead of an arrow, or even a lead weight with a slingshot. The units I've seen cost a bit more than I have wanted to spend — at least so far.

What other options are available? A few months ago, someone sent a link to a YouTube video showing some hams using a compressed air tennis ball "gun." Now that looks slick! Several Web sites include some directions for building similar devices using common materials, except a few "specialty" hardware items. The available kits and assembled units are quite pricey, though. The PVC pipe and fittings should be easy to come up with, so I find myself wondering what other standard plumbing items might serve as the pressure release valve/trigger system. If I find something reasonable and experiment with this idea, I'll let you know what I find. If someone else has a solution, send it in. This is one article that may take more photos than words! I know a few people who seem to have a knack for finding PVC pipe fittings and assembling a variety of "accessories," so maybe with some help, we can come up with a reasonable solution.

I've also got a 6 m antenna waiting to be assembled and deployed at the top of my tower (or maybe even fixed on the side of the tower for a while, just to get it in the air). There is even a coil of discarded cable TV hard line ready to replace the RG-8 run to the top of that tower. Ah, the things I could accomplish with more time or energy!

I have an APRS transmitting station that I put in my car occasionally, but I have not put together a full transceive station, either for in the car or at home. That is another short-term goal that I would like to accomplish this summer. It has been quite a few years since I had a 2 m antenna at home for repeater or packet operation, so maybe the APRS interest will push me to hang something outside my house again.

This is also a good time to start thinking about Field Day plans. Several years ago my wife Jean, WB3IOS, and I started a tradition of going camping for that weekend and setting up a portable station. We've enjoyed that quite a bit, especially when it meant an extra two or three days of camping, for a mini vacation. It doesn't look like the camping trip will work out for us this year, for a variety of reasons, so we are looking at some alternatives. I may end up in my mother's yard in Eastern Pennsylvania, or going with one of the club groups in that area. If you hear WB3IOS on the air for Field Day, it means we are in PA. Give us a call! We'll be happy to hear from our DX readers, too.

I will be attending the Dayton Hamvention this year, and look forward to meeting with many *QEX* readers and authors. I expect to spend quite a bit of time in the ARRL Expo area. My plans are also to roam the Hamvention looking for potential authors and article ideas, as well as attending a number of meetings and forums. Wherever you see me, be sure to stop and say hello!

Ah spring: Time to venture out and enjoy ham radio from many perspectives. It means so much more than sitting hunched over a desk in front of a radio, ears glued to a set of "cans." Enjoy!

James Ahlstrom, N2ADR

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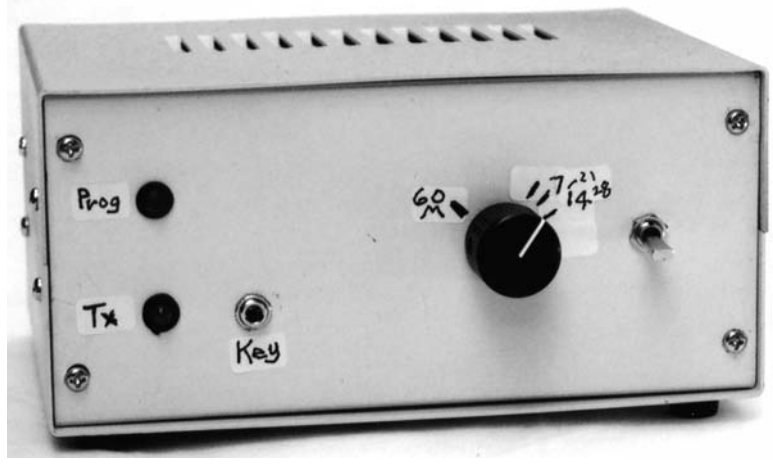
An All-Digital SSB Exciter for HF

Build your own SSB exciter to go with your software defined radio receiver by using an FPGA and software.



These are exciting times to be involved with radio. The digital revolution that has transformed music and photography, and that will soon transform television, is finally making its way to the HF bands. Each year brings new and better digital integrated circuits. Now more and more of radio "construction" can happen in software rather than in hardware. Instead of drilling a panel and mounting knobs and switches, the radio "panel" can be a computer display. Tuning, modulation, demodulation and most filtering can be software too. As the hardware part shrinks, it also becomes more generic, and major modifications can be done in software without altering the hardware at all. The software can be shared using the Internet. I think that software defined radio (SDR) and digital signal processing (DSP) techniques provide the easiest way to homebrew your own equipment, even considering the need to work with surface mounted parts. Home construction can again be a viable and enjoyable part of ham radio.

In 2004 I started building a software defined radio receiver. I was inspired by the work of Leif Åsbrink, SM5BSZ; Gerald Youngblood, AC5OG; Pieter-Tjerk de Boer, PA3FWM, and many others.[1, 2, 3, 4] I had been licensed as a teenager, and I built some of my own equipment, as was common at the time. My license lapsed while I was raising my family, however. I always enjoyed electronics projects, and when I got my ticket back, I wanted to homebrew my own station. Of course electronics had changed substantially and there was much to learn. By 2006 I had a working CW station that offered full break-in (QSK) operation. The receiver hardware was based on Gerald Youngblood's design, but the software was my own. I named the software QUISK, a more pronounceable version of QSK. The CW exciter was the receiver VFO, and used the Analog Devices AD9953. Then it was time to design an SSB exciter.

The project described in this article is my current (October 2007) SSB and CW exciter. I have been operating it on 40 meter CW and phone. Signal reports have been favorable, with good audio and no reports of clicks or noise.

This design is completely independent of my receiver and old CW exciter. In the past, I would have tried to share components between the transmitter and receiver to reduce cost and complexity, but as pointed out by Wes Hayward and others, there are advantages to a design in which the receiver and transmitter are independent.[5] This is especially true for those of us without extensive test equipment, because the receiver can be used to listen to and test the transmitter. A block diagram of a digital transceiver will show few common components except for the VFO anyway, and there are no expensive crystal filters to share.

Although my receiver is based on Gerald Youngblood's design, I decided to move his transmit mixer to the digital domain and use a second independent VFO. That way I could continue to operate CW while building my new exciter, and I could test it with my existing receiver. So, my receiver and new exciter share nothing but the power supply.

The digital mixer and VFO are both provided by a field programmable gate array (FPGA). In case you don't "get" FPGAs, let's take a few minutes for a brief introduction.

What is an FPGA?

The heart of this exciter is the FPGA, and learning to work with it was one of the most fun parts of this project.[6] I used to think that an FPGA was like one of the old PAL chips; a way to replace a few gates and maybe a shift register with one chip and an embedded design. Progress in FPGA technology has been just crazy, though, and the FPGA has evolved into a fast general-purpose computing engine; one more than capable of digital signal processing tasks. [7]

The FPGA consists of a few thousand "cells" that can function as four-input, one-output gates. The logic function for each gate is programmed into a lookup table. For each input, the table determines the output. So the cell can be an AND gate, an OR gate, or any other sort of gate. The cells can also be programmed as adders, or as registers of any width. Complicated digital circuits can be built up as combinations of these cells. The FPGA has a couple dozen dedicated hardware multipliers to speed up multiplication,

[1]Notes appear on page 10.

and it has several kilobytes of memory. The FPGA has busses and connection resources to connect everything, and these act like programmable wires. The FPGA "program" is a list of what cells to use and how to connect them. The FPGA has a hundred input-output (IO) pins, and the IO connections are programmable too. The FPGA is fast. It can operate at a clock rate of 150 MHz, which is much faster than a microcontroller. Of course these numbers are rough. FPGAs come in sizes with greater or lesser amounts of resources.

Programming an FPGA is different from programming a microcontroller or a personal computer because the program does not describe a sequence of instructions for a CPU; it describes the wiring of a digital design. Standard sequential languages like *C* or *Python* are not appropriate for this, and generally you would write an FPGA program in the *Verilog* or *VHDL* languages. The FPGA program for this project was written in the *Verilog* language. If you are used to programming computers, keep in mind that an FPGA is a parallel device. An FPGA does not execute its program a line at a time. It executes multiple lines, and maybe even all lines, simultaneously. With a computer it is difficult to get several things to happen at once, but with an FPGA it is hard to get them to happen sequentially. The ability to write several independent code modules, compile them into different parts of the same FPGA, and then execute the modules in parallel gives the FPGA great computational power. This is what CPU manufacturers are doing with the new multi-core processors, but with an FPGA you get as many special purpose cores as you care to program. FPGAs lend themselves to pipelining. That means you can convert a 50-line program into 50 one-line programs that run in parallel. Once the pipeline fills up, you get one output per clock tick.

FPGAs provide great computational power, but programming them takes a while to get used to. *Verilog* bears a superficial resemblance to the *C* language, and that caused me some trouble because *Verilog* does not act like *C*. It helps to think in terms of digital design elements like adders, multiplexers and registers because that is what the FPGA program represents, and the *Verilog* compiler writers were digital designers who think in those terms.

In the computer business it sometimes happens that a language or program is pressed into service in an area it was not designed for. For example, *Java* started out as a language to program set top boxes. *Verilog* started out as a language to model digital circuits. A standard *Verilog* reference book is full of language features that are illegal in an FPGA program, such as the ability to enter gate delays. To program an FPGA, we are using a subset of the *Verilog* language in a special-purpose way, and this is called "*Verilog* for synthesis." Maybe someday there will be a good book on this, but I haven't seen one yet. Meanwhile, you will have to rely on the documentation provided by the FPGA manufacturer.

Of course, to duplicate my SSB exciter you don't need to program the FPGA. The object code is provided. If you do want to program it, the source code is also provided. The program is a modest one, and consists of only a few hundred lines of *Verilog* code.

Apparently, an FPGA is a very advanced piece of silicon. But it has (at least) two features that make it a very friendly component for the amateur homebrewer. Typically, we are limited to one or two sided printed circuit

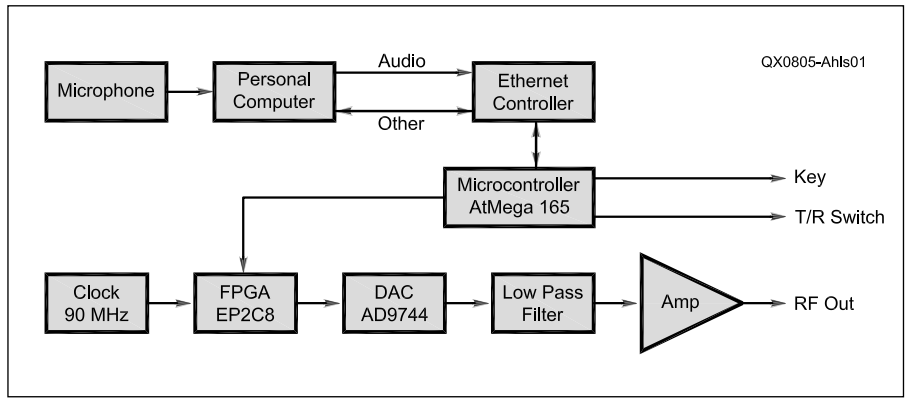


Figure 1 — This is a block diagram of the exciter.

PC Software

- Microphone samples at 48 kHz, 16-bit samples
- SSB speech processing
  - High pass IIR filter to shape passband
  - Bandpass filter (FIR) and separate into I and Q
  - Tune up to 12 kHz
  - Clip audio 12 dB
  - Bandpass IIR filter to reestablish bandwidth
  - Tune back down to baseband
  - Normalize amplitude (AGC)
- Send 16-bit I and Q audio samples using UDP over Ethernet
- Send FPGA program and FPGA transmit frequency
- Receive key status to mute audio and substitute sidetone

Microcontroller Software

- Fixed IP address 192.168.1.44
- Known UDP ports 0x553A, B, C
- Process all Ethernet traffic
  - Ethernet Address Resolution Protocol (ARP)
  - ICMP echo request (Ping)
  - FPGA program: SSB, CW, etc.
  - Audio data — copy to FPGA
  - Frequency control — send to FPGA
- Send key up/down status back to PC

FPGA Software

- Write audio samples to memory
- Memory holds 4608 samples, 96 milliseconds
- When memory is half full, turn on transmitter
  - Read audio from memory; write to memory continues
  - Interpolate to 90 MHz
  - Tune to output frequency with CORDIC
  - Send RF data and clock to 14-bit DAC
- Audio will eventually stop
- When memory is empty, turn off transmitter

Figure 2 — The exciter software outline.

boards. These are the only boards that can be made at home, and even then only one side can be accurately etched. Multilayer boards are very expensive in small quantities, and the cheapest two sided commercial prototype board I have found costs about $70, as much as all the advanced ICs combined. Maybe some day I will understand why the box and the circuit board cost more than the contents. Anyway, some of the connections on a homebrew board may be longer than desired or may be made with an actual wire instead of a board trace. These lines may "ring"; that is, you may have multiple pulse reflections on them. With a dedicated chip you are out of luck, but with an FPGA you can program around the problem. For example, you can count up a counter when a line goes high, and count down when it goes low. You don't accept the value of the line until some counter value is reached; that is, after a known delay. Essentially you have de-bounced your faulty line, just as you might de-bounce a mechanical switch.

The other homebrew advantage of an FPGA is the programmable IO pins. Suppose you need to connect an eight-bit port to another chip. With a dedicated chip it might happen that the port pins go up on one chip and down on the other, so if you connect them with eight parallel traces on the board, the port bits will be reversed. This never happens with an FPGA. You simply connect all the traces to any convenient pin on the FPGA, and program the pins as desired.

Exciter Block Diagram and Schematic Diagram

The block diagram of the exciter hardware is shown in Figure 1. Figure 2 is an outline of the software. Figure 3 shows the exciter schematic diagram. In this discussion, I will be giving some background on the design decisions and why they were made, in case you want to use this project as a starting point for your own design.

We start with the microphone. I am using a Logitech USB microphone from RadioShack, catalog number 33-101. This plugs into the computer and appears as another sound card. It can capture audio data but not play back. The mic captures 16-bit samples at 48 kHz, a standard rate for most sound cards. This is greater than CD quality, but the CIC filters (see below) need this high rate. An alternative is a sound card with a mic input, but the mic inputs of some sound cards are noisy, and you may need an external preamp or volume control to adjust the level. My receiver uses my only sound card, so I am using the USB mic. The computer filters and clips the mic audio and divides it into in-phase (I) and quadrature (Q) signals (I/Q signals). Other designs would send the I/Q signals to sound card left and right channels, and then to an analog I/Q mixer to generate RF. My design uses exactly the same I/Q signals, but they remain digital data.

The software I use to generate these I/Q signals is part of my QUISK receiver, and is programmed in *Python* using a Tkinter graphical user interface (GUI), and also in *C*. You are welcome to use QUISK if you can run *Linux*. If you want to run *Windows*, the GUI is portable and the *C* is quite generic, so only the sound card access *C* code would need to be changed. You could also cut the relevant code (microphone.c) out of QUISK and use it in your own software. The I/Q signals required are the usual ones generated in other software, such as that used with the SDR-1000. Many software packages can generate them.

We now need a way to get the digital audio data out of the computer and into the exciter hardware. The data is two 16-bit samples (I and Q) at a 48 kHz rate, a bit rate of 1.5 megabits per second. Lots of people use USB, and I see that the new FlexRadio 5000 uses firewire. Although I like USB when someone else does the programming, USB is difficult to program even with a special controller IC. On the exciter side, the initial handshaking between the exciter and the host computer is complicated. On the computer side, the problem with USB is the drivers. I use both *Linux* and *Windows*, and they require different USB drivers. It always seems that the Linux drivers are missing or are an afterthought. Once you have the drivers, the problem is sharing the device between two or more programs on the computer. Only one program can use a USB interface at once unless you write the multiplexing (sharing) code yourself.

In this design I decided to use Ethernet, or, more specifically, UDP packets within the Internet Protocol (IP) carried by an Ethernet local area network. This is what your computer is no doubt using now for Internet connectivity, and you may know it as TCP/IP. But we are using UDP (another IP data type) instead of TCP. To connect the exciter and the computer, you just plug their Ethernet connectors into the same hub or switch. Figure 4 shows the back panel of my exciter, with the various connectors, including the Ethernet connector.

The programming is very simple. On the exciter side there is no startup code for UDP. Data packets just arrive at the Ethernet controller, and the microcontroller processes them. On the computer side, the code for UDP uses the "sockets" interface and the same *C* code can be used for *Windows* and *Linux*. UDP socket code can be written in many different computer languages, not just C. I have UDP code in C and in Python. Any code written in *Python* automatically runs on *Linux* and *Windows*, including UDP code. Unlike USB, multiple programs can talk to the interface at once, just by using different UDP ports. UDP can also be routed over the Internet. In case anyone thinks UDP is not suitable for audio data, remember that it is the protocol used by voice over Internet protocol (VOIP) providers such as Vonage and Skype.

We are using the Ethernet connection for other data besides the audio data. Since the exciter is on an IP network, it answers ping requests. Pinging the exciter is the first debug step to see if it is alive. The exciter also participates in the address resolution protocol (ARP), a way for the computer to discover its Ethernet address given its IP address. If you don't know what ARP is, don't worry; it just means the exciter is working politely with your local area network. The computer uses Ethernet to send the frequency tuning data to the FPGA, and to request a status reply. The exciter uses Ethernet to send the key up or down status to the computer, to mute the receiver during transmit. Note that the key is connected to the microcontroller. In CW, key up/down messages also substitute a sidetone.

Ethernet is also used to program the FPGA. Since the FPGA does not have permanent memory, the FPGA must be programmed on every power up. A program for an FPGA is a several hundred kilobyte file. I have three FPGA programs available on my computer; one for SSB, another for CW and a third for a two-tone test. The chosen program is downloaded from the computer to the microcontroller using UDP, and the microcontroller programs the FPGA. An alternative design would be to store the program in a special memory chip connected to the FPGA. My design avoids the small cost of the memory chip, however, and the several hundred dollar cost of the special memory programming cable. There are also other advantages. You can debug the microcontroller and Ethernet code first without having to deal with the FPGA. It makes it easy to write new FPGA programs while still using the old ones. I can imagine programs for PSK31, FM and other modes being added in the future.

The microcontroller now copies the audio samples to the FPGA. But before we discuss that, let's take a look at the FPGA clock. If you are used to microcontrollers it will be no surprise that an FPGA has a clock, too, and that operations occur on clock edges. In fact, FPGAs have special dedicated clock inputs, and you must use these to keep clock skew to a minimum. In our case, the FPGA clock is also used for the digital to analog converter (DAC), and that means you need a really good clock. Any noise on the DAC clock

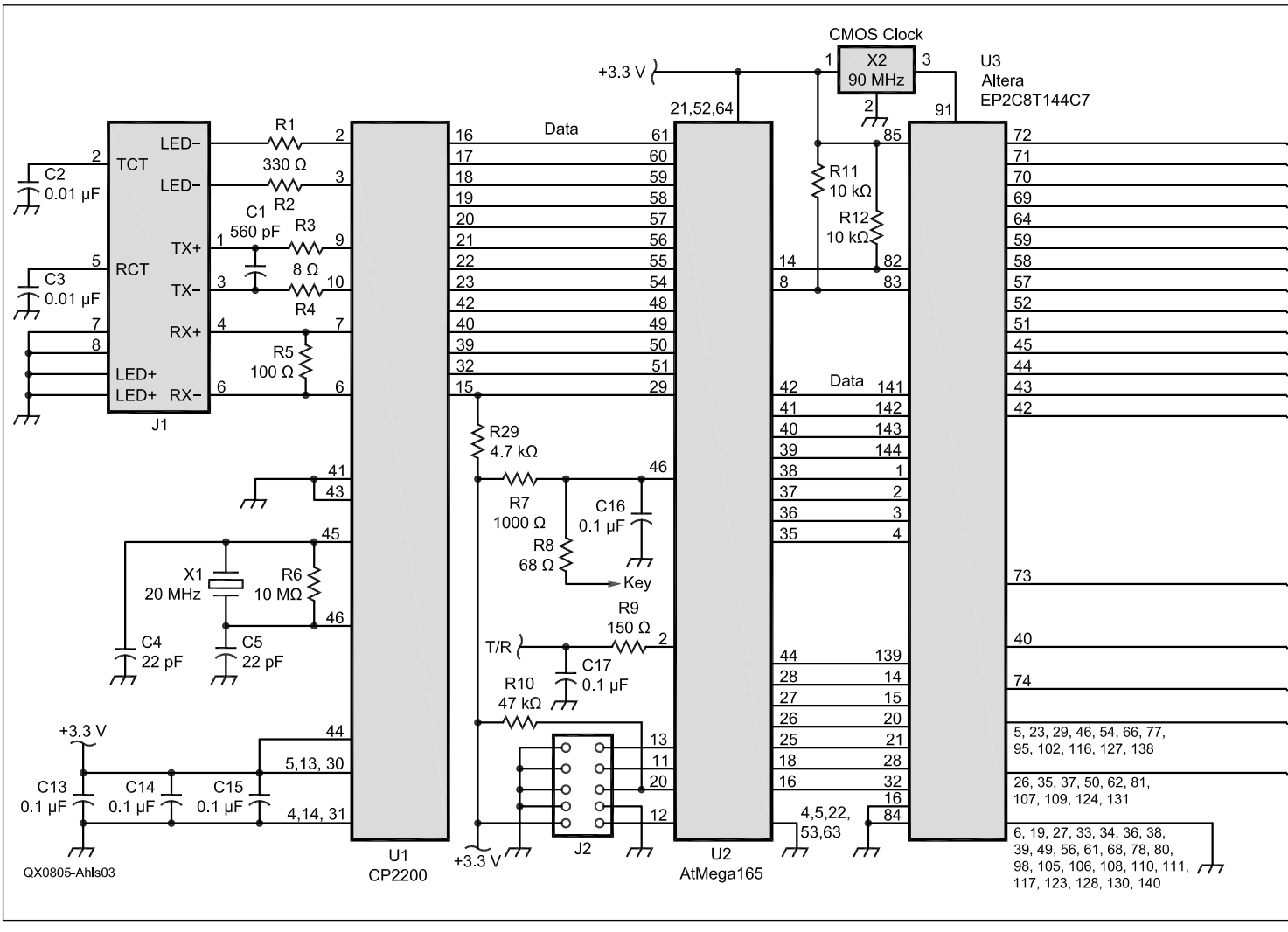


Figure 3 — This drawing shows the exciter schematic diagram.

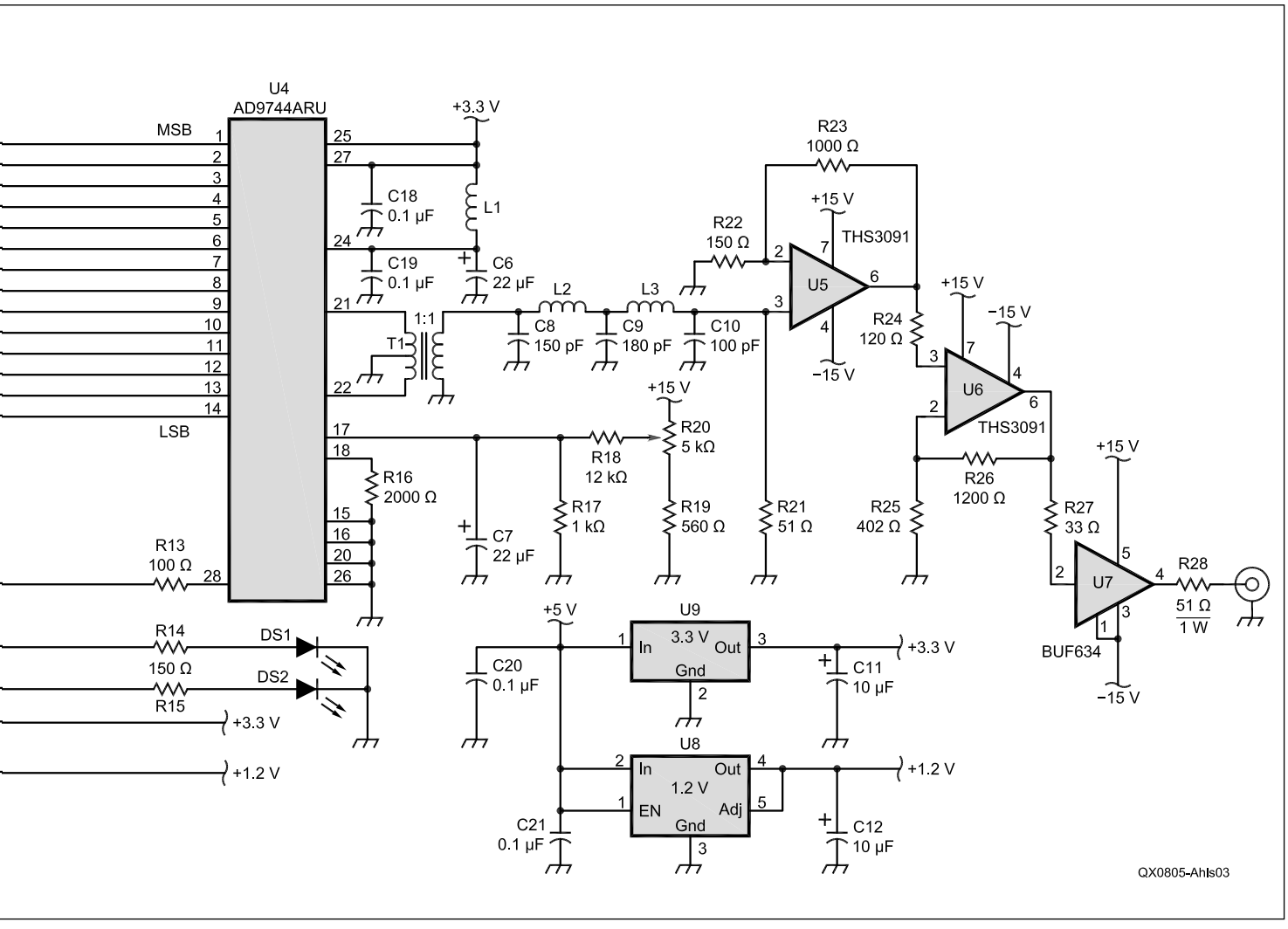
Parts List

All Capacitors are 50 V ceramic 1206 SMD unless otherwise indicated.

C1	560 pF
C2, C3	0.01 µF
C4, C5	22 pF
C6, C7	22 µF Tantalum 10 V SMD
C8	150 pF
C9	180 pF
C10	100 pF
C11, C12	10 µF Tantalum 6 V radial
C13-C21	0.1 µF 50 V ceramic 0805 SMD bypass. Not all bypass capacitors are shown.
DS1	LED, Green
DS2	LED, Red
J1	Mag Jack, Stuart SI-50170, DigiKey 380-1086-ND
J2	5 × 2, 0.1 inch pin header
L1	7 turns no. 32 enameled wire on ferrite bead
L2	359 nH, 10 turns no. 24 enameled wire on T37-6 core
L3	327 nH, 10 turns no. 24 enameled wire on T37-6 core

All Resistors are ¼ W, 5%, 1206 SMD unless otherwise indicated.

R1, R2	330 Ω
R3, R4	8 Ω
R5, R13	100 Ω
R6	10 MΩ
R7, R17, R23	1000 Ω axial
R8	68 Ω axial
R9, R14, R15	150 Ω axial
R10	47 kΩ
R11, R12	10 kΩ
R16	2000 Ω
R18	12 kΩ
R19	560 Ω axial
R20	5 k Ω pot, DigiKey CT2204-ND
R21	51 Ω
R22	150 Ω
R24	120 Ω axial
R25	402 Ω
R26	1200 Ω axial
R27	33 Ω
R28	51 Ω, 1 W axial
R29	4700 Ω
T1	6 bifilar turns no. 32 enameled wire on BN-43-2402 core
U1	CP2200
U2	AtMega165, DigiKey AtMega165-16AV-ND
U3	Altera EP2C8T144C7, DigiKey 544-1457-ND
U4	Analog Devices AD9744ARU, DigiKey AD9744AR-ND
U5, U6	THS3091DDA, DigiKey 296-15789-5-ND
U7	BUF634, DigiKey BUF634T-ND
U8	MIC29302WT adjustable voltage regulator, DigiKey 576-1124-ND
U9	MIC29300-3.3WT 3.3 V voltage regulator, DigiKey 576-1119-ND
X1	20 MHz crystal, DigiKey 300-8446-ND
X2	CMOS Clock, 90 MHz, Fox F4105



will appear at the output, and any clock jitter will appear as phase noise. You could build your own crystal clock, and if you do I suggest using the differential clock inputs on the FPGA. If you use a CMOS clock oscillator, as I do, avoid those meant for general use, and find one specifically designed for communications use — one with a specified jitter. For DAC use, the clock is a big deal.

The I/Q audio samples at 48 kHz are read from the Ethernet chip by the microcontroller, and then copied to the FPGA. The job of the FPGA is to change the sample rate to 90 MHz ("interpolate") and tune the signal to the desired output frequency in a digital mixer. An alternative design would use an ASIC for this, one known as a "digital up converter" (DUC). There are some problems with a DUC, however. Some use a ball-grid package, and I haven't figured out how to solder those yet. The Analog Devices AD6622 has a serial interface, and it is hard to move the data through the microcontroller fast enough. Besides, FPGAs are fun. See Note 6.

The interpolation (sample rate increase) step is simply a matter of adding zero samples to the signal. We have a 48 kHz rate that must be multiplied to 90 MHz, an increase of exactly 1875 times. So we just take one sample, add 1874 zero samples, and repeat. Actually it is better to do this in two stages, first multiplying by 25 then 75. But there is a catch. There will be repeats, or "aliases" of the original signal every 48 kHz, and these aliases must be filtered out by an anti-alias filter. The well-known way to do this is to use a cascaded integrator-comb (CIC) filter.[8] The CIC filter is especially fast and simple, uses no multiplications, and it interpolates and filters all at once. Note that we are using a narrow 25 times interpolation stage followed by a wider 75 times stage. This is because a CIC filter can only work with a signal that is a small fraction of the initial sample rate. In our case that is an SSB signal in 0 to 3 kHz divided by 48 kHz. Very wide (30%) bandwidths will not be filtered effectively. Also note that interpolation is an integer multiplication, and you wind up with a multiple of the original sample rate of 48 kHz. If you want to raise the clock frequency to a higher standard value, the next available clock rates are 120 MHz (times 2500) and 150 MHz (times 3125).

After interpolation we have a 90 MHz sample rate, but the data is still audio. The last job of the FPGA is to mix the baseband SSB signal to the output frequency in a digital mixer. There is no magic to a digital mixer. It just relies on the rule that you multiply two exponentials by adding their exponents. For example:

$10^2 \times 10^5 = 10^7$

Next, recall that if you put a sine or cosine wave into a Fast Fourier Transform (FFT) you get two spikes, one at plus frequency and one at minus frequency. But if you use a pure wave, the complex exponential

$e^{i\omega_0 t}$

you get only one spike. That is the reason to use complex signals; your mixer only produces one output, not the sum and difference

a regular mixer does. A digital mixer is just a multiplier. In our case, the first exponential is the I/Q SSB signal:

$e^{i\omega t}$

the second is a pure wave

$e^{i\omega_0 t}$

and we multiply these together to get the product

$$e^{i\omega t} \times e^{i\omega_0 t} = e^{i(\omega+\omega_0)t}$$

We see that the product is the original signal plus the tuning frequency, ω_0, just what we want from a mixer. The only problem is how to generate the tuning signal — a complex exponential — at, for example, 7.25 MHz, that will tune our zero hertz SSB signal to the 40 m band. This can be generated by the CORDIC algorithm.[9] This algorithm calculates a complex exponential by successive rotations of a vector, to produce a known phase angle. The phase angle is increased at each clock pulse by a constant amount, the "phase increment," and that increment determines the output frequency. The phase increment is sent from the computer to the microcontroller, and then to the FPGA.

After the digital mixer, the FPGA has a 7.25 MHz (for example) signal sampled at 90 MHz. It sends this signal to a 14 bit digital-to-analog converter (DAC), an Analog Devices AD9744. From now on the signal is analog. The next step is an analog low pass filter to remove high frequency images. This is only a five pole low pass filter, but additional filtering is provided later. The signal is then amplified by a THS3091 current feedback operational amplifier (op-amp). Originally this was the final output stage, but this chip overheated when driving a 50 Ω load. I wanted as high an output as I could get from the op-amps. The op-amps have very low IMD products, and the more output I could get from op-amps, the less distortion I would have from subsequent amplifier stages. So I added a second THS3091 and a BUF634 output stage. This combination can drive 50 Ω at about 1 W, but since I have filters following the exciter, I added a 50 Ω output series resistor. The output is 300 mW, up to about 25 MHz, and decreasing to 175 mW at 30 MHz. This decrease in output should not occur, but I have not had time to track it down.

I measured the IMD performance on my SDR-IQ, and got –62 dB at 5.3 MHz, –50 dB at 21.2 MHz, and –41 dB at 29 MHz.[10] These measurements are in dB below one tone, not PEP. The SDR-IQ does not have an IMD specification, so I am not sure where the IMD is generated. The IMD is not a strong function of output level until the output clips. The IMD performance is very good indeed.

Operation on CW

The above description is applicable to SSB. For CW, the hardware is identical, but the FPGA runs the CW program instead of the SSB program. Note that the key connects directly to the microcontroller, so generating CW does not use a computer. The FPGA uses the same CORDIC algorithm, but the input is no longer audio samples, it is just a number. A constant CORDIC input of 310000 would produce a sine wave at full amplitude, but we need to shape the CW envelope to reduce key clicks. When the key goes down, a counter slowly counts up to 310000 and stays there. When the key is released, it counts down to zero. The counter value is the input to the CORDIC algorithm, and the result is a ramp up and down of the CW envelope with a time of seven milliseconds. The T/R relays are also controlled by

Figure 4 — This photo shows the back panel of the exciter, with the various input/output connectors.

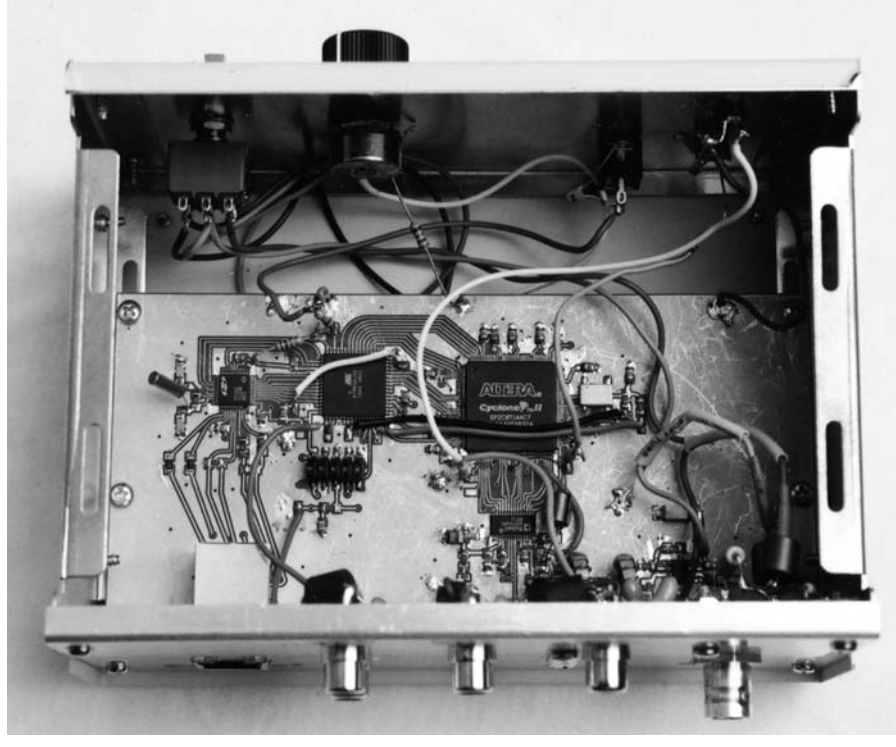


Figure 5 — Here is a look inside the project box. Note the construction style, which is a mix of circuit traces and "ugly" construction.

the microcontroller. On key-down, the T/R relays are closed and the FPGA is keyed 12 milliseconds later so the relays have time to switch. On key-up, the relays are opened after a 12 millisecond delay to allow time for the CW waveform to go to zero.

Notes on Construction

I generally build all my projects using the "ugly" construction method. The ground leads of the parts are soldered directly to an un-etched circuit board, and the remaining connections are made directly above. The un-etched board provides a good ground plane. I like this method because it is easy to experiment with the circuit, and to replace sections of the circuit that do not work. But when there are surface mounted parts involved, the board must be etched to accommodate them. We still need a good ground plane, so only a minimum of the board can be etched. I etch the pads for the surface mount components, the power supply bypass chip capacitors, most direct connections between integrated circuits, and some of the power traces. There is a limit to how many traces can be routed on the board because there must be a very good solid ground plane in these RF and digital circuits. Even routing just power traces can break up the ground plane too much, so I make many connections with wires. It helps to use double-sided board and solder the top and bottom surfaces together with wires passed through small holes. The bottom side remains un-etched. As space permits, I attach unused IC pins to pads so wires can be added later if required. The result is still "ugly" construction but with surface mounted parts incorporated.

The board for this project was laid out using *Eagle* under the assumption that I would make the board myself.[11] The board turned out with too many bridged traces. The 0.5 mm pin pitch parts are at the limit of what I can manage with a homemade board. Perhaps I can make it work by making the traces narrower, as the pre-sensitized circuit boards I am using have trouble with narrow spaces between traces. In the end, I decided to order a commercial two-sided prototype circuit board. These are quite workable but come without solder mask or silkscreen. Figure 5 is a photo of the circuit board inside the project box.

Digital Spurs

No transmitter based on DSP is complete without a search for spurious emissions, or "spurs." All mixers generate unwanted outputs at frequencies removed from the desired output. In the case of DSP circuits, a desired sine wave output will be accompanied by small unwanted signals that bear no obvious relationship to the carrier. Part 97.307 of the FCC rules specifies that the maximum spur for transmitters below 30 MHz must be at least 43 dB below the desired output, and that the spurs must be reduced "to the greatest extent practicable." Taking a look at the data sheet for the AD9744, we see that it has spurs of –74 dBc at an output frequency of 25 MHz and a sample rate of 65 MHz. Spurs generally rise with the output frequency and decrease with the sample rate.

The FPGA digital mixer can also produce spurs due to the inaccuracy of integer arithmetic. In this design we are using wide widths for the calculations; 32 bits for phase and 20 bits for amplitude. If spurs are found to result from the FPGA it can be programmed for even wider data widths.

Digital spurs can be located far removed from the output frequency. For example, the AD9953 DDS VFO I am using for my receiver shows –60 to –70 dBc spurs at 20, 160 and 180 MHz when operating at 80 MHz. Some data sheets will specify close-in spur performance that is significantly better than total bandwidth performance. We are using a narrow bandwidth filter for each band on transmit to suppress these wide spurs.

I searched for spurs from the exciter using my receiver, but the largest spurs I could find clearly came from the receiver and not the exciter. So I recently purchased an SDR-IQ receiver and spectrum analyzer from RfSpace to search more carefully for spurs. (See Note 10.) The specified spur-free range is 80 dB below full scale worst case, and 100 dB typical. I set my two-tone test signal level to 20 dB below full scale and searched several megahertz around the signal frequency. The largest spurs I could find from the exciter were 77 dB below one tone on the 10 m band. Since this is 97 dB below full scale, I cannot be sure the spurs are due to the exciter and not to the SDR-IQ. The SDR-IQ shows only 190 kHz of the band at once, so it takes a while to set the exciter to several frequencies in each band and search many megahertz around each frequency. Even then, I didn't try every possible operating frequency. Still, the purity of the output was gratifying. It was difficult to find any spurs at all, even small ones.

The Software

The software for this project is available on my Web site, and is licensed under the general public license (GPL) as an open source project.[12,13] Complete project files, not just source files, are provided. The FPGA software is in the Altera directory, and the microcontroller software is in the AVR directory. This software should not require changes. The computer software is in the quisk directory, but this includes the complete receiver software too. The QUISK software runs under the *Linux* operating system, but only the quisk/microphone.c file is relevant to the exciter, and it is generic *C* code. It should run on *Windows* by just changing the sound card access.

The software for this project was written in *Python*, *C*, *Verilog* and *AVR* assembler language. I especially enjoy *AVR* assembler language. It is a textbook example of a RISC processor instruction set, and is very different from the high level languages I use in my day job. This was my first *Verilog* project, so I hope to get suggestions for improvement.

Future Work

This is version one of the exciter, and there are some things I would do differently the next time. Copying audio data through the microcontroller is a bottleneck. The current design works, and does have the needed throughput, but with little room to spare. If a faster data rate is required in the future, the microcontroller could not keep up. And it would never be able to operate at the full 10 megabit rate of Ethernet. The Ethernet controller CP2200 used here has an 8 bit interface that is perfect for the microcontroller. I planned to use the RXAUTORD interface in the CP2200 to read successive bytes, but I could not make that work. Instead I am setting an address for every byte read, and this has slowed down the throughput. Next time I would try connecting the Ethernet controller to both the microcontroller and the FPGA. The microcontroller could get the FPGA program and handle routine UDP packets as in the current design, but the FPGA would read its audio data directly from the Ethernet controller. This should provide close to the maximum 10 megabit data rate. It would probably be easier to do this with a different Ethernet chip such as the ENC28J60.

The drop in output at 30 MHz should not happen. I am sure this could be fixed. I would also try to use one THS3091 instead of two. Using two was just the result of adding an extra buffer after the board was done. It would also be interesting to raise the clock rate to 120 or 150 MHz instead of 90, although 90 MHz is clearly sufficient for 30 MHz output.

I need to continue to search for spurs. Perhaps I will write a computer program for the SRD-IQ to search over its frequency range and automatically find spurs. Maybe I should port QUISK to *Windows*, but first I need some time to just operate my station!

The Rest of My Station

The exciter output goes to a BNC connector and then to a separate filter box, ampli-

fiers, the transmit/receive (T/R) switch and the antenna. The filter box is in a separate enclosure and has a band-pass filter for each band, to provide spur reduction on transmit and protection from strong out of band signals on receive. After that the signal is amplified and sent to a set of low pass filters, also one per band. The signal then goes through a final 35 MHz low pass filter and then to the antenna. The final power output is about 100 W. Transmit/receive (T/R) switching is provided by relays driven by the microcontroller, and the microcontroller provides suitable sequencing. My filter box currently has filters for the 60, 40, 30, 20 and 17 m bands with one remaining position. This meets my current requirements, as I lack antennas for 160 and 80 m, and my receiver is limited to 20 MHz and below. Of course, the SSB exciter will work on all HF bands.

Conclusions

Operating this exciter on the air has been gratifying. Audio reports have been good, and if I can hear a station I can usually talk to them, too. CW operation is especially nice with smooth full break-in operation.

It seems to me that the digital techniques used in a software receiver and a software transmitter are so different that there is no point in trying to share parts between them. In a receiver the problem is dynamic range and avoiding clipping. In a transmitter the problem is to maintain high signal levels to maximize power output and numerical accuracy. My old CW exciter that shared the VFO with the receiver never did have a very good keying envelope, and the switch in VFO frequency between transmit and receive made full break-in harder to achieve. This current design is much better.

I hope this project inspires others to build their own equipment. You are welcome to duplicate this project, or, better yet, improve on it. I know some people dread working with surface mounted parts, but this is a solvable problem with proper magnification and a decent soldering iron. And there is no alternative if you want to use modern ICs. These modern ICs pack a punch, and they eliminate the need for endless lists of discrete parts. Just look at this board. There are only five integrated circuits, and most of the rest of the parts are power supply bypass capacitors. To me, this is easier to construct than the hundreds of discrete parts that constitute the alternative.

I would like to say a special word of thanks to Leif Åsbrink, SM5BSZ. His Linrad pages are a treasure trove of practical information and hard-won insight. (See Note 1.) Near the end of this project, when I was stuck on how to do SSB speech processing, I revisited his Web site. And there it was: his recently added insights on just that topic. Thanks Leif!

James Ahlstrom, N2ADR, was first licensed as KN3MXU in 1960. He received a BS in physics from Villanova University in 1967 and a PhD in physics from Cornell University in 1972. He then moved to New York to work in the financial business. He is currently a one-third owner of Interet Corporation, Millburn, New Jersey. Interet publishes software to analyze leveraged equipment leases. His license lapsed while raising his family, and he was re-licensed in 2006. He currently holds an Amateur Extra class license. Besides Amateur Radio, he enjoys bird watching, skiing, music and working out at the gym.

Notes

[1]**www.nitehawk.com/sm5bsz/**

[2]Gerald Youngblood, AC5OG, "A Software-Defined Radio for the Masses," *QEX* Jul/Aug 2002, pp 13-21, Sept/Oct 2002, pp 10-18, Nov/Dec 2002, pp 27-36, Mar/Apr 2003, pp 20-31.

[3]**wwwhome.cs.utwente.nl/~ptdeboer/ham/sdr**. [Note that this URL is correct as printed. There is no period between www and home. — Ed.]

[4]**www.arrl.org/tis/info/sdr.html**

[5]Wes Hayward, Rick Campbell and Bob Larkin, *Experimental Methods in RF Design*, ARRL, 2003, ISBN: 0-87259-879-9; ARRL Publication Order No. 8799. ARRL publications are available from your local ARRL dealer, or from the ARRL Bookstore. Telephone toll-free in the US 888-277-5289, or call 860-594-0355, fax 860-594-0303; **www.arrl.org/shop; pubsales@arrl.org**.

[6]**www.fpga4fun.com**

[7]U. Meyer-Baese, *Digital Signal Processing with Field Programmable Gate Arrays*, Second Edition, Springer-Verlag, 2004.

[8]Richard G. Lyons, *Understanding Digital Signal Processing*, Second Edition, Prentice Hall, 1996.

[9]Ray Andraka, A Survey of CORDIC Algorithms for FPGA Based Computers, **www.andraka.com/files/crdcsrvy.pdf**.

[10]**www.rfspace.com**.

[11]**www.cadsoftusa.com**.

[12]**www.james.ahlstrom.name/quisk**.

[13]The software files for this project are also available for download on the ARRL Web site for our readers' convenience. Go to **www.arrl.org/qexfiles** and look for the file **5x08_Ahlstrom.zip**. The authors Web site may have updated listings available for download. QEX

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A Software Controlled Radio Preselector

A Tunable Bandpass Filter Bank for the HF Bands (1.8 MHz to 30 MHz).

The SCR-Preselector prototype is packaged in a Hammond Instruments case.

Features:

- PC controlled through a graphical user interface (GUI).
- USB v2.0 compliant, for data communication with PC. Plug and Play feature.
- Tested under *Windows XP* and *Windows Vista32* Operating Systems (OS).
- Can perform its functions as a standalone unit.
- Compatible with software defined radios (SDR).
- Removes the strong signals radiated back to the antenna from quadrature mixers.
- Improves your average receiver or scanner to lead with strong signals, on the most noisy and crowded bands.
- Connected to an exciter as a tunable band pass filter, it reduces harmonics generated in the exciter.
- Complete receiver front-end for your projects.
- Joined to a VFO, the preselector can perform a tracking tuning function.

The SCR-Preselector — A First Line of Defense Against Interference and Static

The SCR-Preselector, pictured in the lead photo, is connected in series between the antenna and the receiver. Tuning to desired signal keeps the preselector bandwidth centered at the operating frequency, adding selectivity and protection to your receiver. The SCR-Preselector rejects or reduces out of band unwanted interfering signals, improves signal to noise ratio and protects against interference from strong signals like AM/FM broadcast stations. It can also be helpful in preventing interference during multi-multi contest operations.

The high linearity of the preselector is preserved thanks to a passive design that uses large toroidal cores and reliable mechanical relays for switching functions, instead of nonlinear semiconductors that cause distortion and exhibit low tolerance against strong signals and static.

Direct sampling SDRs are protected against false images since the SCR-Preselector incorporates a low pass filter (LPF) with an enhanced stop band of more than 60 dB. This filter has the ability to provide a very sharp transition from pass band to stop band at a cut-off frequency of 30 MHz, attenuating signals in the VHF region that could mix with the sampling frequency of its analog to digital data converter.[1]

The SCR-Preselector incorporates gas discharge tubes to provide safety against static and voltage transients. Further, the unused antenna input is short-circuited to ground.

Brief History

In September 2006 I attended a conference at the Whitton Amateur Radio Group, at which Jeffrey Pawlan, WA6KBL, had the kindness to give us during his European tour.[2] The talk was all about Software Defined Radio, and the *WinRAD* computer program, how it came about, how it works and where will be going in the future.

Motivated by his speech I became truly interested in SDR. I began playing around with quadrature sampling detectors, also called Tayloe detectors. This is a nice piece of radio technology. Soon I noticed that despite its excellent features, it still needs a good front-end circuit to condition signals before they reach the mixer. I focused my interest on this problem, and with the help of my old friend Xavier Junqué de Fortuny, a software engineer, we started the job. First of all, because Xavier lives in Barcelona, Spain, and I live in London, England, we established a broadband link through the Internet, with audio/video capabilities. One year later, the SCR-Preselector was born.

[1]Notes appear on page 18.

Overview

The core of the SCR-Preselector is the tunable band pass filter bank, which is complemented with the necessary switching, protection, filters, amplifier and control circuitry as shown the block diagram in Figure 1 and the assembled prototype of Figure 2. The incoming signals pass through the antenna selector relay, and then go to the bypass relay. From there, the signals either bypass the preselector or enter a step attenuator that offers a selection of 0 dB, 6 dB, 12 dB or 18 dB. Those attenuation values match the standard calibration of S meters.

Next, the input signals enter a broadcast band (BCB) high pass filter. This is a so-called "brick-wall filter," which attenuates spurious signals from strong AM broadcast stations as much as 120 dB. Such signals are well known enemies of shortwave receivers. I have stretched the effects of this filter into the medium wavelength band. It has a very sharp slope, as Figure 3 shows. The filter has minimum attenuation of all signals at 1.8 MHz and higher frequencies, including the CW portion of the 160 m band.

At this point, the input signals reach the tunable band pass filter bank, which is arranged in five overlapping bands that are user selectable. Each filter is a classic serial tuned LC circuit, and offers narrow bandwidth with little attenuation. A set of eight switchable capacitors of 1 pF, 2 pF, 4 pF, 8 pF, 16 pF, 32 pF, 64 pF and 128 pF emulates the variable capacitor needed to tune the series resonant circuit. The control program

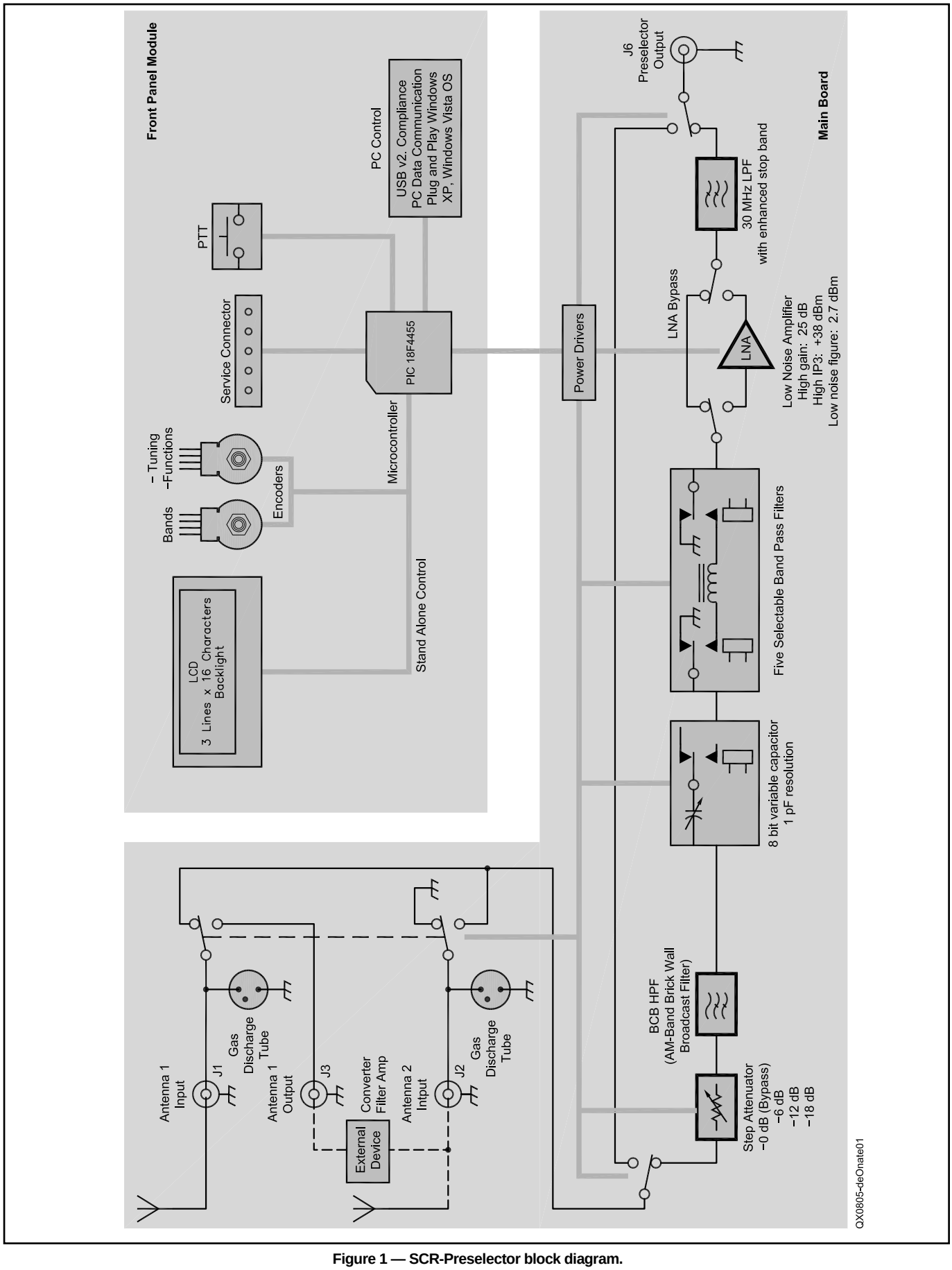


Figure 1 — SCR-Preselector block diagram.

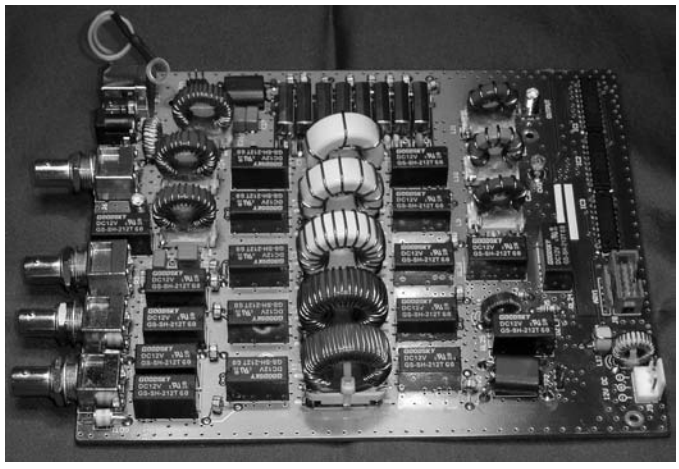


Figure 2 — This photo shows the main circuit board for the preselector.

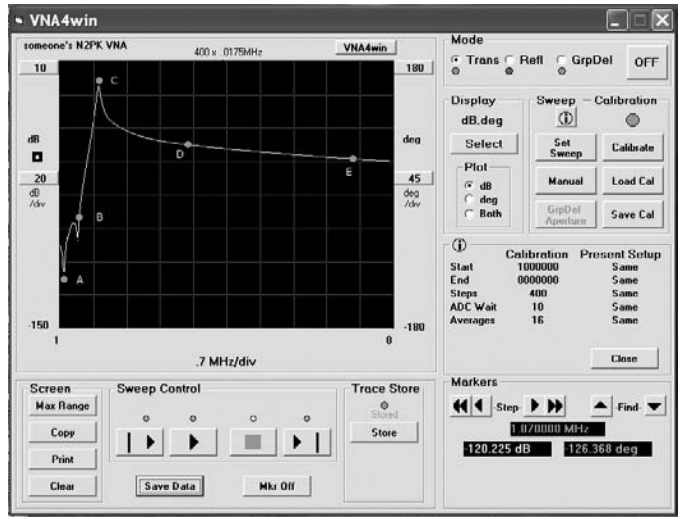


Figure 3 — The SCR-Preselector was tested with an N2PK Vector Network Analyzer. Point A: –120.2 dB at 1.07 MHz; Point B: –81.12 dB at 1.4 MHz; Point C: -3.5 dB at 1.8M Hz; Point D: –39.5 dB at 3.6 MHz; Point E: –48.1 dB at 7.05 MHz.

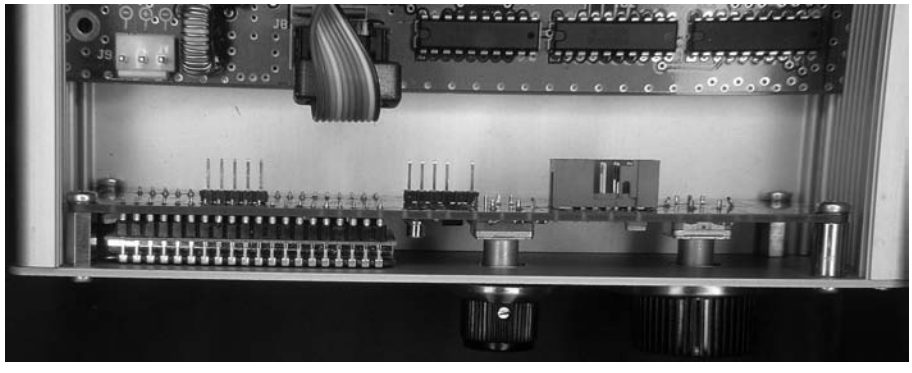


Figure 4 — A photo of the front panel circuit board module, assembled on the front panel of the Hammond Instrument case.

Figure 5 — Here is a screen shot of the SCR-Preselector Graphic User Interface display on my computer.

performs this task by adding or subtracting capacitor values in binary fashion, in direct relationship with the tuning knob operated by the user. Increments or decrements are done in steps of 1, 2, 5 or 10 units. One of five toroidal inductors is selected by the front-panel switch to form the filters. The selectable bands are:

- A) 1.8 MHz to 4 MHz
- B) 3 MHz to 6 MHz
- C) 4 MHz to 10 MHz
- D) 9 MHz to 18 MHz
- E) 16 MHz to 30 MHz.

Filtered signals are amplified or bypassed in the following stage, a low noise amplifier (LNA). I chose a Gali74 MMIC device, with an average gain of 25 dB, a noise figure (NF) of 2.7 dB and high dynamic range.[3] Because it is a high gain, wideband amplifier that operates to more than 1 GHz, we need to "hold its horses." The gain of this amplifier can be regulated through the input attenuator. An LPF connected at the output, limits the bandwidth to 30 MHz.

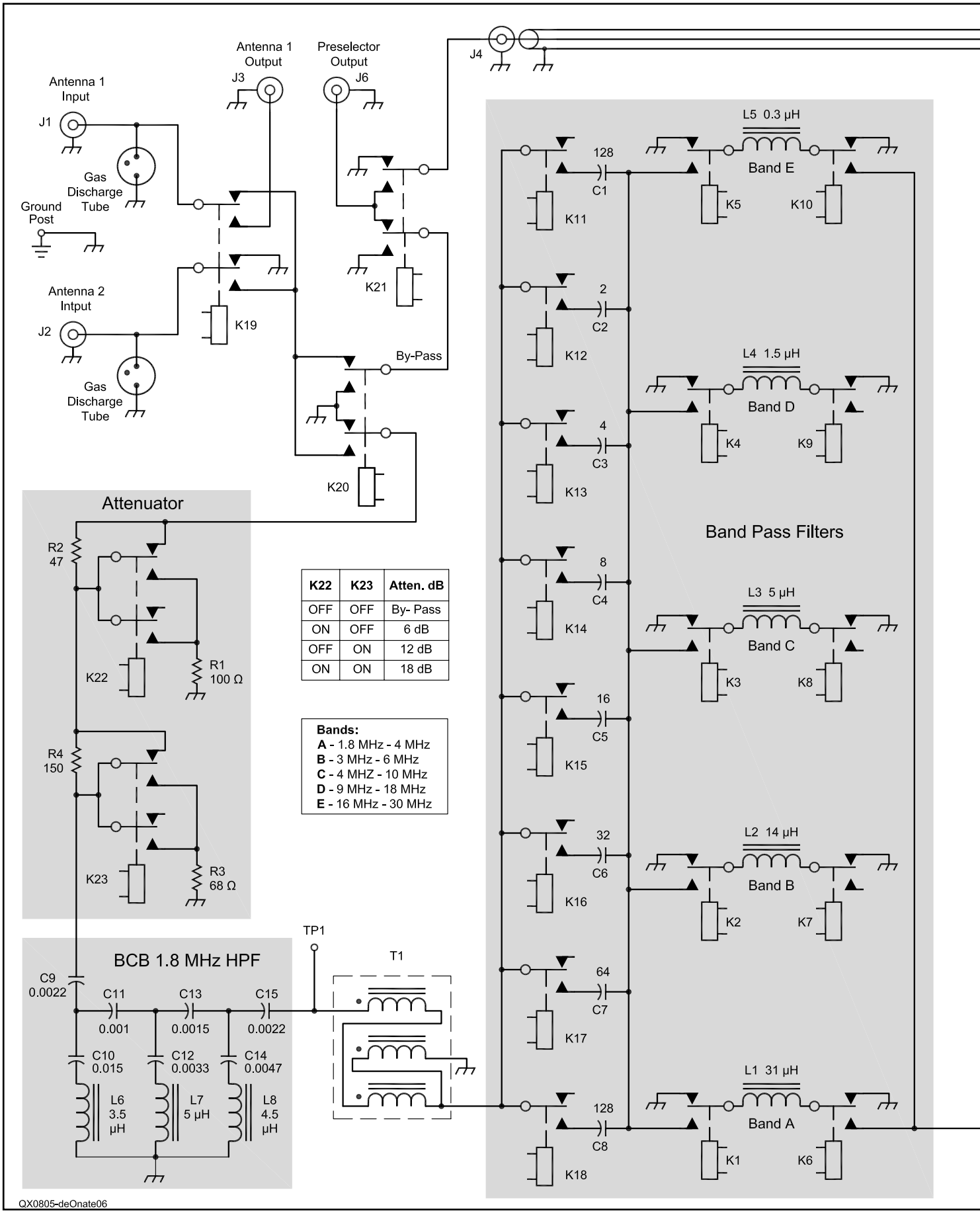
To make the SCR-Preselector compatible with computerized receivers we needed it to operate not only as a stand-alone unit, but also to perform its functions under computer control. For all that, a PIC microcontroller 18F4455 was selected, which includes an integrated USB peripheral, 35 I/O ports and in circuit programming (ICSP), among other features. It is assembled on a front panel circuit board module apart from the main circuit, along with a liquid crystal display (LCD) and two incremental rotary encoders for band switching, tuning and other functions. See Figure 4. Also, it offers the possibility to command the SCR-Preselector by other external means.

The software program on the PC runs under *Windows XP* or *Windows Vista32*. The user, through the GUI, commands the SCR-Preselector in the same way as it does in stand-alone mode. See Figure 5. Switching between USB or standalone modes is done when the USB cable is plugged in or unplugged. This adds a "Plug and Play" feature to the project. The program can work at the same time with any SDR software running on the PC, allowing to the user to control both simultaneously.

Circuit Description Main board

The SCR-Preselector main board schematic is shown in Figure 6. K19 is the antenna selector relay. The SCR-Preselector is designed to operate with antennas (and feed lines) that have a 50 Ω impedance. An optional external device, such as a converter, amplifier or filter can be inserted between J3 and J2, with antenna 2 selected.

Relays K20 and K21 drive signals to J6, the preselector output in bypass mode, or to the attenuator section. Switching to either K22, K23, or both configures the desired attenuation, or bypasses signals. Next, the circuit built around C9 to C15 and L6, L7,



K22	K23	Atten. dB
OFF	OFF	By- Pass
ON	OFF	6 dB
OFF	ON	12 dB
ON	ON	18 dB

Bands:
A - 1.8 MHz - 4 MHz
B - 3 MHz - 6 MHz
C - 4 MHZ - 10 MHz
D - 9 MHz - 18 MHz
E - 16 MHz - 30 MHz

QX0805-deOnate06

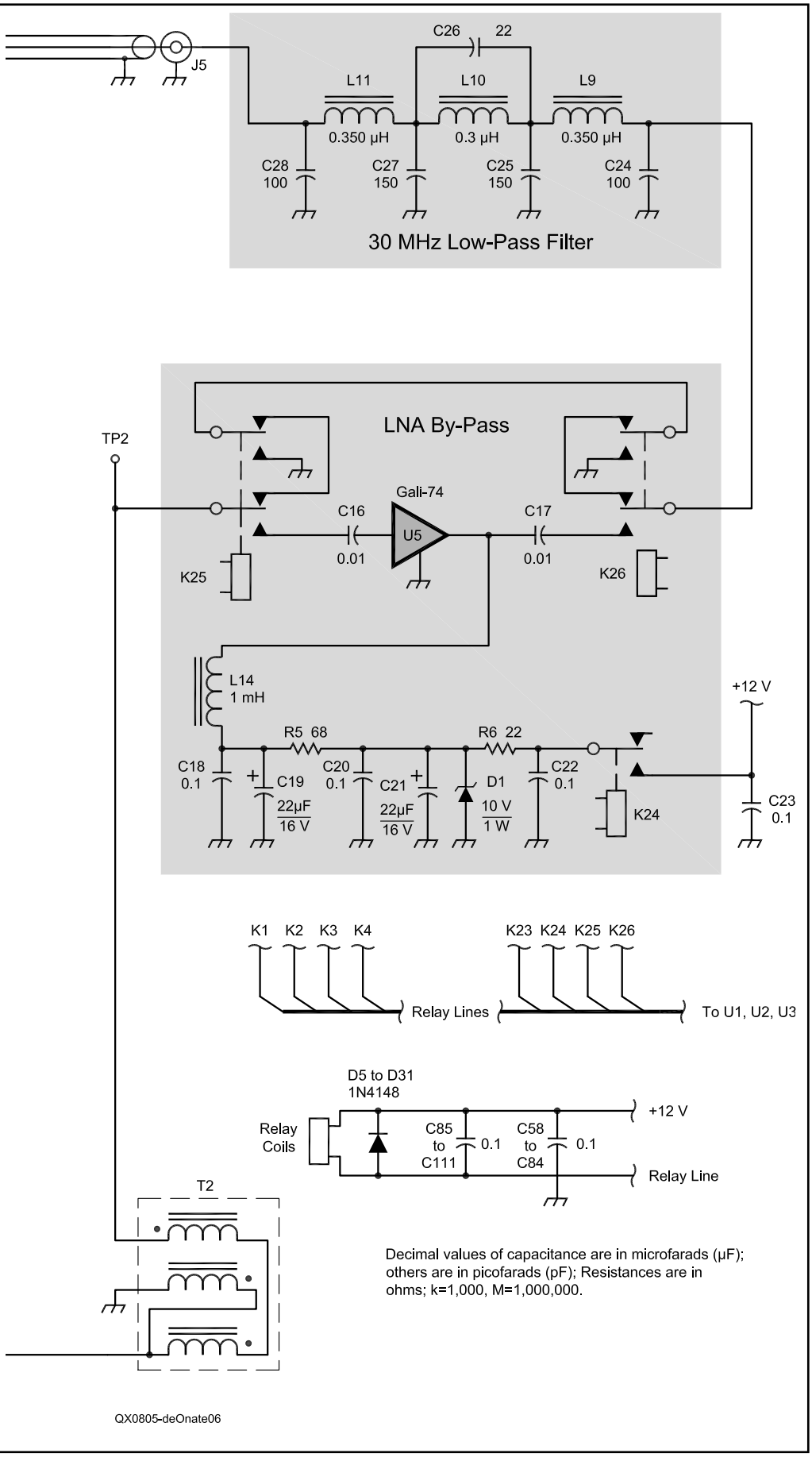


Figure 6 — The schematic diagram of the SCR-Preselector main circuit board.

L8 shapes a sharp BCB HPF of ten elements. T80-2 powdered iron toroidal cores are used to achieve large Q values. Other characteristics are the low pass band insertion loss — less than 1 db — and the flat pass band response.

The characteristic impedance of the circuit, 50 Ω, is converted to a typical low level for the series band pass filter by means of T1, a wide bandwidth UNUN transformer arranged to improve the filter high-frequency response.[5]

A set of eight capacitors, C1 to C8, and relays K11 to K18, form the "switching capacitor" section or "variable capacitor emulator" that is connected to relays K1 to K5. Together with K6 to K10 and L1 to L5, the switched capacitors shape the five overlapped band pass filters. Only one set of relays and one inductor are connected at a time, such as K1-L1-K6.

Notice that the band inductors that are not selected are connected to ground to avoid unwanted resonances. Large cores — T106 powdered iron — are used to avoid saturation. Saturated cores produce intermodulation distortion (IMD) with large signals. Some designers use the saying, "*The more iron in circuit, the merrier*." On the other hand, high Q values of more than 300 at the resonant frequency are reached, as measured with an HP 4342A Q-meter.

The resonant circuits with different values were designed with the filter design program, *Elsie*, written by Jim Tonne, WB6BLD.[6] This is an excellent piece of software. I was able to evaluate the filters in real time using *WinDipoles*.[7] I followed this methodology for the entire project.

All this work revealed good selectivity, but some attenuation — an average of 3 dB on bands of interest. Sensitivity and selectivity are not friends. That is not a difficulty, because who wants sensitivity in noisy and crowded bands? On the other hand a good preamplifier complemented with a step attenuator offers a good option for keeping gain and noise at optimum point to feed the mixer. That is the mission of the next stage, amplification, if needed.

The amplifier stage is built around U5, a low noise amplifier with high IP3 of 38 dBm, polarized to 4.8 V dc and decoupled. K24 provides operating voltage when the amplifier is selected. Signals are routed to or bypassed around the amplifier by relays K25 and K26.

After the amplifier, the signal goes towards C24 to C28 and L9 to L11, which form a sharp eight element low pass filter

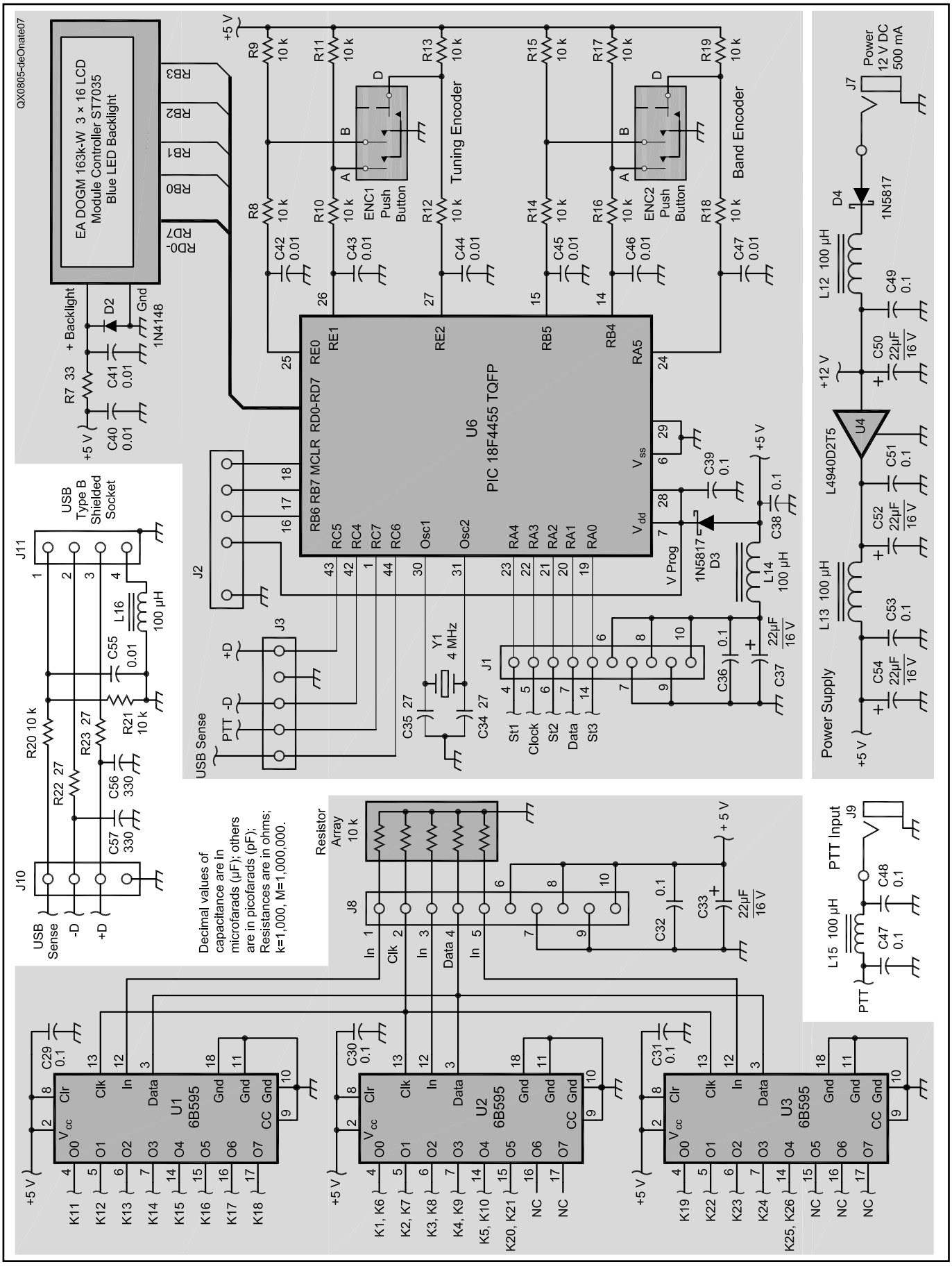


Figure 7 — This schematic diagram shows the SCR-Preselector power drivers and front panel module.

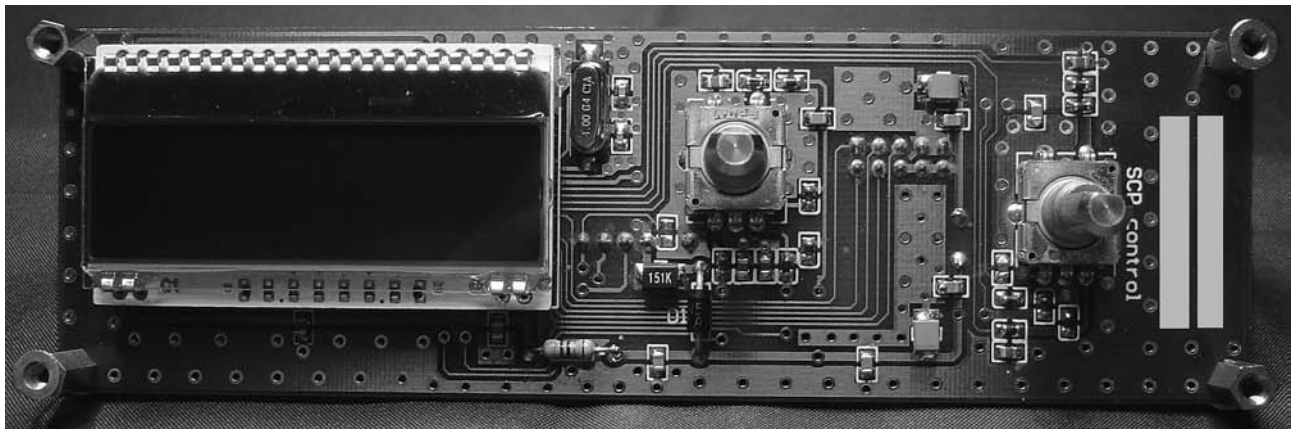


Figure 8 — The front panel module circuit board is shown in this photo. The PIC microcontroller is located below the LCD. The band encoder and tuning encoder switches are visible near the center and near the right edge of the photo.

with a cut-off frequency of 30 MHz. This filter has a Chebyshev topology, with a touch of Cauer response to improve its stop-band rejection but maintaining an acceptable pass-band return loss, greater than 20 dB. The LPF output at J5 connects through an internal coaxial link, with J4 and is then routed to J6, the preselector output, via K21. If bypass mode is activated, U5 is switched off and J4 is shorted to ground for protection purpose.

In Figure 7, the eight bit serial power driver shift registers, U1, U2 and U3 interface the relays on the main board with the microcontroller. Data, clock and strobe control signals are connected to the front panel control module via J8. These signals are pulled down with Resistor Array 1. Data signals are clocked to them and each one is latched independently by means of its strobe line. Power drivers can be commanded from any external compatible logic control, because of their simple codification.

J7 is the external power supply connector. It is followed by reverse-polarity protection and decoupling. A 5 V regulator, U4, feeds the logic control through J8.

Front Panel Control Module

The circuit board for the control module of the SCR-Preselector is located behind the front panel. The Schematic diagram is included in Figure 7. The user operates in Standalone Mode by means of two rotary mechanical encoders with push-on switches, ENC1 and ENC2. You can see those controls in the center and on the right side of Figure 8. Both have 20 pulses per revolution and a series of polarized RC filters on each pin to eliminate the noise generated by the bounce of its switches. This application does not require the fine precision that a VFO tuning control would require, so optical encoders were not used.

The 3 line × 16 character LCD module is driven in parallel mode. The polarization protection circuit, R7 and D2 feeds the operating voltage to the backlight LED.

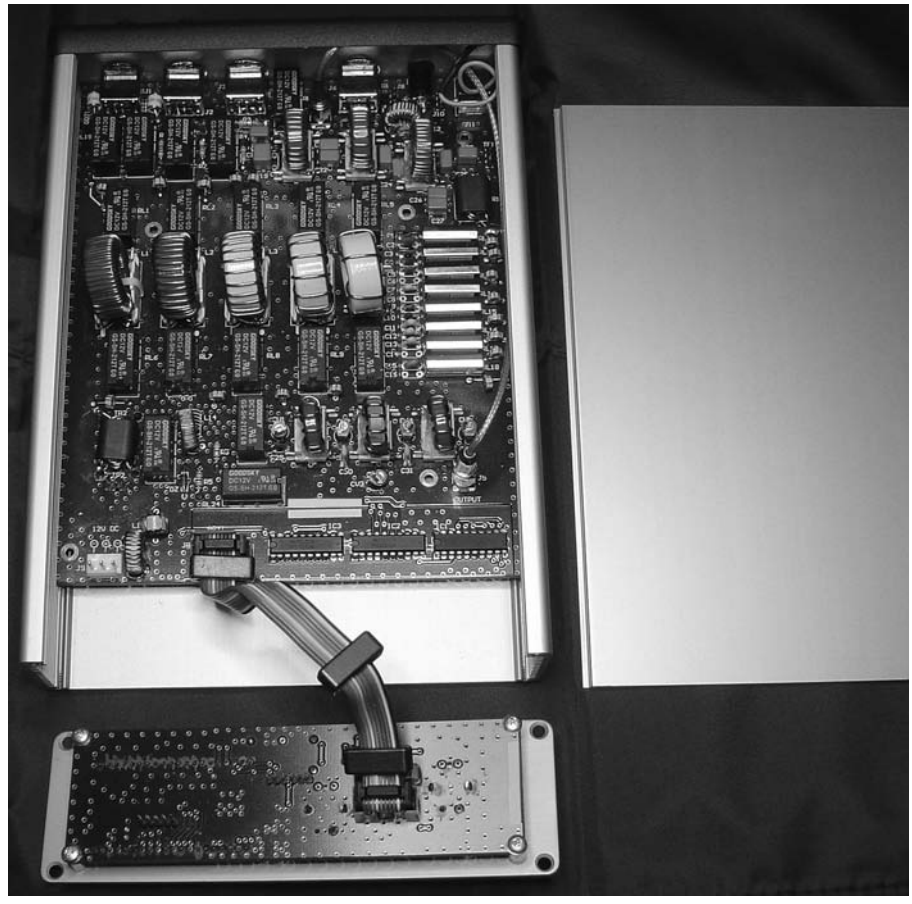


Figure 9 — A photo of the completed SCR-Preselector, with the front panel and cover removed.

Because of its TQFP package, the PIC microcontroller must be programmed in circuit. For this, an ICSP service connector is included, as J2. Another connector, J3, routes external signals, USB sense, PTT activated and USB data differential lines. A 4MHz quartz crystal is used for the main oscillator. The internal PLL multiplier converts this to the 96 MHz USB clock and 48 MHz CPU clock frequencies. No external reset or supervision circuits are needed because they are embedded in the microcontroller. J1 routes the signals to control the power drivers to J8 on the main circuit board. The 5 V dc supply from U4 is fed to pins 6 to 10 of J1, to power the module. This supply is strongly decoupled with capacitors and L14,

to eliminate the noise generated from the PIC microcontroller.

Construction

No project can be considered complete without dressing a good case around it. So I chose a Hammond Instrument enclosure, model1455T2201. These enclosures are very good for projects, because they have removable front/back panels, and a sliding top cover. See Figure 9. The internal slots make it very easy to slide a 0.062 inch (1.6 mm), standard thickness circuit board into the slots, and no screws are required. If another enclosure is selected, the main board arranges several through holes to mount spacers. The board is fixed on the rear panel by means of the hardware supplied with the BNC right angle sockets.

Firmware, Software

The firmware (object code) on the PIC microcontroller was written in Assembler and *C* languages, under *MPLAB* and *C18* compiler.[8] The software program and driver on the computer side were developed under *Visual Studio.NET* from Microsoft. The program is an executable file that runs under *Windows XP* or *Vista32*. Figure 10 shows the computer screen with the Rocky 3.4 SDR software, the Realtek soundcard audio control software and the SCR-Preselector software all running. The SCR-Preselector software doesn't need to be installed; only the USB driver does. The software does need the Framework installed, however. This is a software component that comes with *Windows* update. The software was tested on several computers, and the final version ran without bugs.

The program offers to the operator the following features on the computer and standalone operating modes:

Selection of one of the five bands; bypass mode; four attenuator positions; Preamplifier ON/OFF; Antenna selection switch; tuning steps ×1, ×2, ×5 and ×10; tuning knob and five memories for each band. Each memory keeps all present configurations. When the program starts, it attempts to connect to the SCR-Preselector. If it is not connected, an error message appears for three times, followed by the GUI being configured in default status — Bypass. Selecting any band, the program leaves this state. Tuning is accomplished either by rotating the wheel mouse or through left-right arrow keys. The memory feature is activated by clicking on the MEM button. There are five red "LEDs" on the display, marked 1 through 5, that flash; when you press any of them, all present configurations are stored in that memory location. The selected "LED" number remains on. Up to five presets per band can be memorized. To erase a memory, simply click two times on the red LED selected will clear that position.

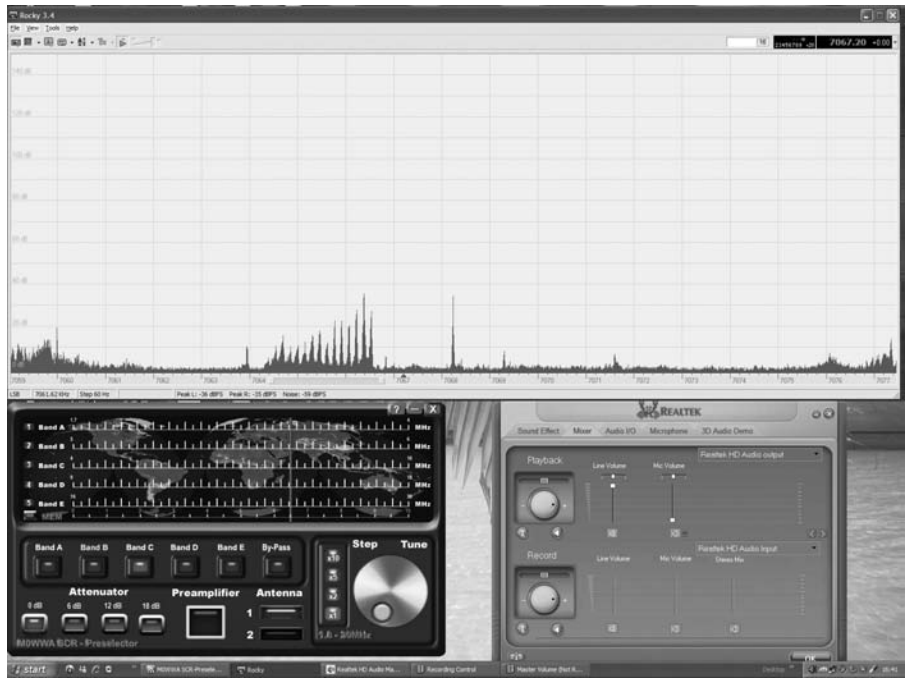


Figure 10 — This screen shot shows the SCR-Preselector control software working together with the Rocky 3.4 Softrock receiver control program and the Realtek sound card control software.

Explaining all of the software and hardware options involved on this project in detail would take too many pages, we offer you further information regarding this project on our little corner on Internet, at: **www.m0wwa.co.uk/**.

Notes

[1]Leif Åsbrink, SM5BSZ, "IMD in Digital Receivers," *QEX*, Nov/Dec 2006, pp 18-22.

[2]Jeffrey Pawlan, WA6KBL, **www.pawlan.com/wa6kbl.html**..

[3]Minicircuits, Gali-74 Datasheet, **www.minicircuits.com/products/amplifiers_monolithic.html**.

[4]Microchip, PIC18F2455/2550/4455/4550 Data sheet, **ww1.microchip.com/downloads/en/DeviceDoc/39632D.pdf**.

[5]Jerry Sevick, W2FMI, *Transmission Line Transformers*, Chapter 6, "Unbalanced to Unbalanced Transformer Designs," SciTech Publishing, Raleigh, NC, 4th Edition, 2006. *Transmission Line Transformers* is available from your local ARRL dealer, or from the ARRL Bookstore. Telephone toll-free in the US 888-277-5289, or call 860-594-0355, fax 860-594-0303; **www.arrl.org/shop**; **pubsales@arrl.org**.

[6]Jim Tonne, WB6BLD, **tonnesoftware.com/index.html**.

[7]Heros Technology Ltd., *WinDipoles*, **www.herostechnology.co.uk/herostech/pages/software.html**.

[8]Microchip, Development tools, **www.microchip.com/stellent/idcplg?IdcService=SS_GET_PAGE&nodeId=64**.

QEX

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An Advanced Direct-Digital VFO

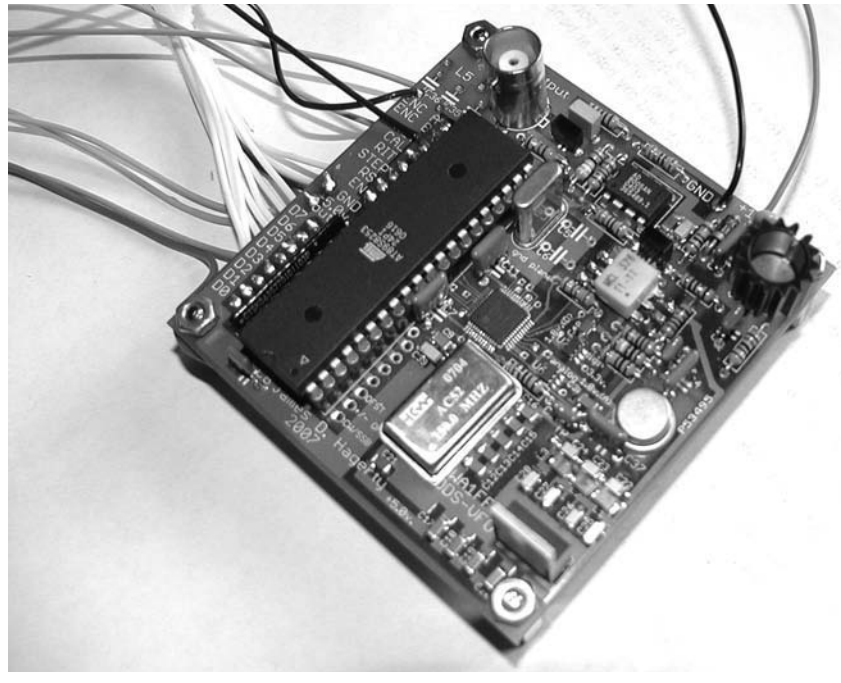
The author used an Analog Devices AD9951 DDS IC in a new VFO design.

A number of radio amateurs, including the author, have built direct digital VFOs with the Analog Devices AD9835 and the AD9851.[1] Although powerful software features have been available for these projects, there was a significant limitation in the hardware: the 10-bit D/A converter at the output limits the spurious-free dynamic range (SFDR) to about 60 dB. This is a critical parameter if such a device is used as a local oscillator, because even very low-level spurs can mix with weak adjacent signals, severely compromising dynamic range.

This article describes a hardware design that features the Analog Devices AD9951.

A 14-bit D/A converter at the output, and a much higher rated clock speed than the 98xx family allows a frequency-dependent SFDR in excess of 70 dB, and approaching 80 dB with a 400 MHz internal clock frequency. It puts the latest technology on a four layer, 3 inch circuit board, and can be used as a stand-alone VFO or as part of a multi-loop frequency synthesizer. There are two stages of RF filtering included in the design: the first between the 9951 DDS and the output buffer amplifier, and the second after the buffer, at the board output. A significant capability for software expansion exists, as only about 2 KB of program memory (out of an available 12 KB) is presently used. As in previous designs, tuning is accomplished with a shaft encoder. An inexpensive LCD provides a frequency readout.

Present software features include a calibration routine to null out clock frequency error, RIT (receive incremental tuning) spanning ± 10 kHz, an improved method for changing the tuning step size, and flash EEPROM storage of all RAM data. This last feature allows the most recent calibrated carrier to come back up after power down. Additional new software features are under development. The oscillator is tunable over the entire HF band. Higher output frequencies are possible if the clock frequency is increased. The complete design, software, and board were developed using tools costing the equivalent of an entry-level transceiver.



The AD9951 DDS IC was chosen as the successor to older DDS IC families because of its greatly improved spectral purity, its suitability as a local oscillator and its powerful architecture. For example, one of the many new features of this chip is a programmable rise-time parameter to minimize side lobes, such as those causing key clicks. All of these features come at a price of significantly greater complexity. The chip is contained in a 48-pin surface-mount package about the size of a small fingernail. A special surface-mount template was made for this part using the printed-circuit layout package, *Eagle*. Tom Riley, a friend and an expert with *Eagle*, helped me with this. Fortunately, it fit perfectly the first time.

Three supply voltages are required for the 9951: 1.8 V analog, 1.8 V digital, and 3.3 V for the interface pin. The chip runs on a 1.8 V core, a startling difference from the "old" 5 V logic many are used to. The 9951 can be directly interfaced with 5 V logic once the 3.3 V is supplied on pin 43. Analog Devices engineers have told me that the much greater chip circuit density mandates these lower supply voltages. The technology is impressive: at present I am clocking this chip with its 1.8 V core at 150 MHz. Several programmable internal clock multiplier factors are available to increase this up to the rated value of 400 MHz.

Circuit Design Architecture

Figure 1 shows the complete circuit of the direct-digital VFO. The overall intent of this project was to put the most advanced hardware on a compact board immediately and concentrate on elaborate software features later. Still, there were several features that I wanted, and these were given high priority.

[1]Notes appear on page 24.

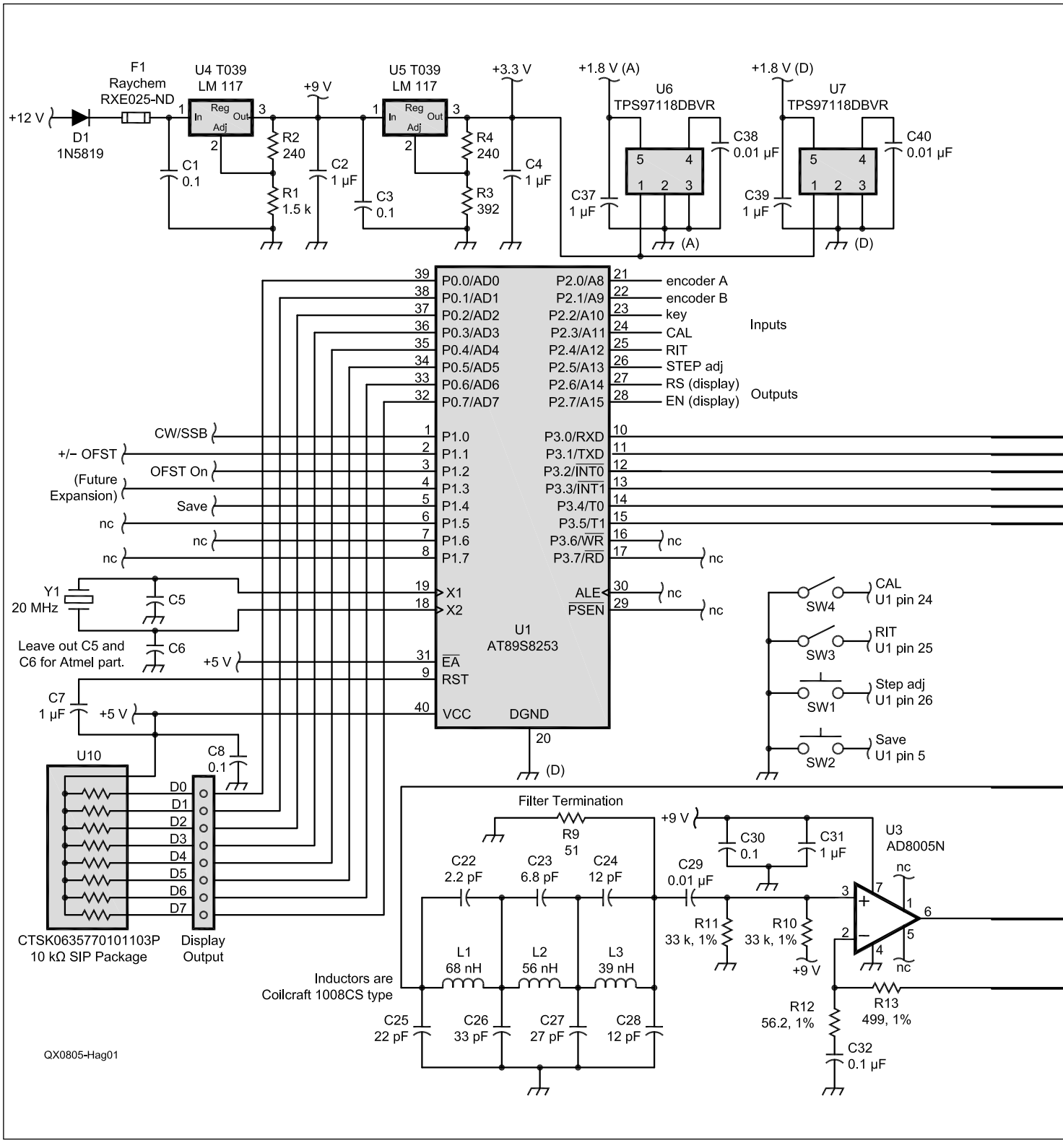
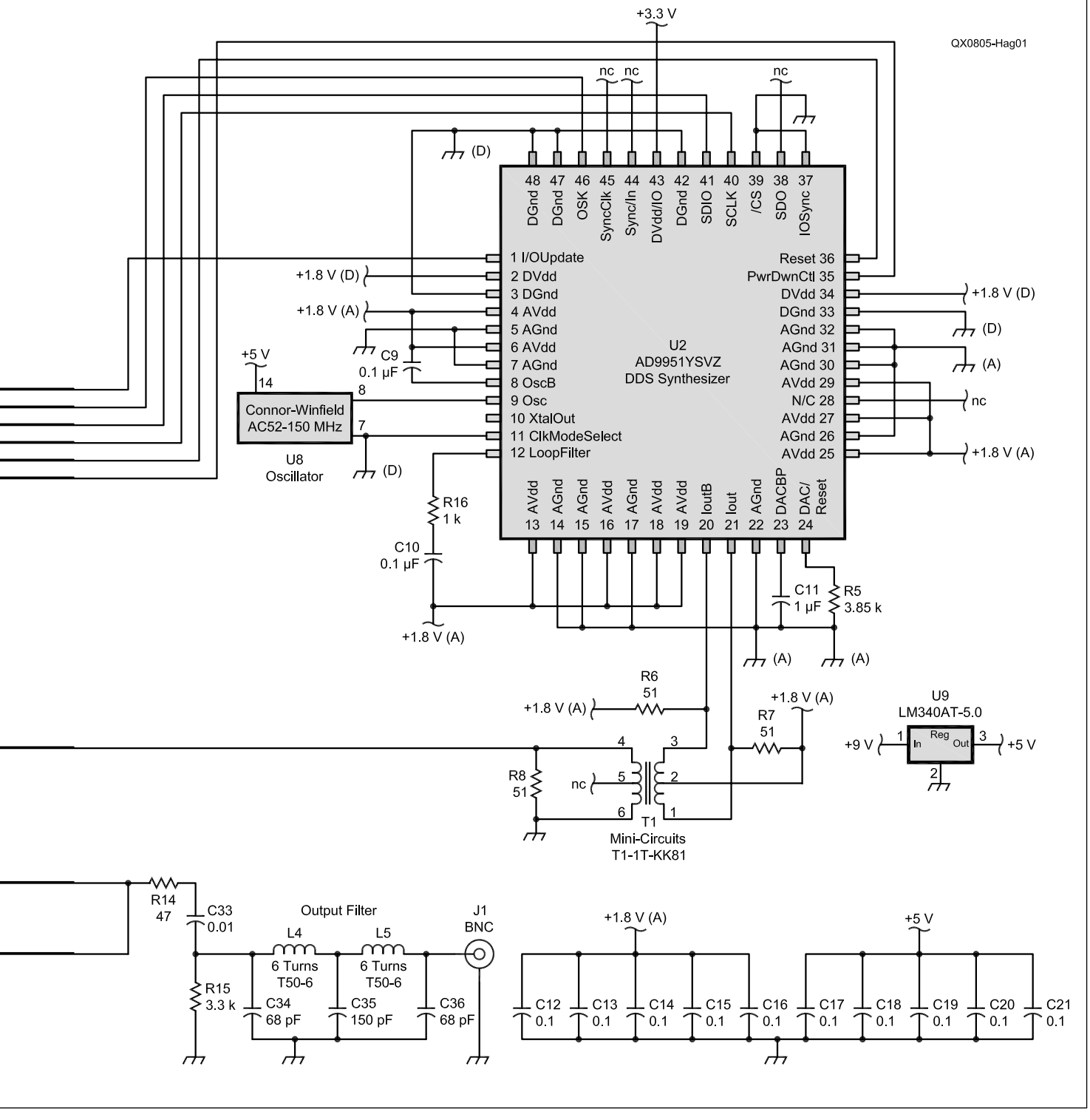


Figure 1 — The schematic diagram for the direct digital VFO uses an AD9951 DDS IC, and an AT89S8253 microprocessor.


QX0805-Hag01
+3.3 V
nc nc
nc
(D)
48 47 46 45 44 43 42 41 40 39 38 37
DGnd DGnd OSK SyncClk Sync/In DVdd/IO DGnd SDIO SCLK /CS SDO IOSync
1 I/OUpdate
2 DVdd
3 DGnd
4 AVdd
5 AGnd
6 AVdd
7 AGnd
8 OscB
9 Osc
10 XtalOut
11 ClkModeSelect
12 LoopFilter
Reset 36
PwrDwnCtl 35
DVdd 34
DGnd 33
AGnd 32
AGnd 31
AGnd 30
AVdd 29
N/C 28
AVdd 27
AGnd 26
AVdd 25
U2
AD9951YSVZ
DDS Synthesizer
+1.8 V (D)
+1.8 V (A)
+5 V
14
C9
0.1 µF
8
7
Connor-Winfield
AC52-150 MHz
U8
Oscillator
(D)
R16
1 k
C10
0.1 µF
+1.8 V (A)
AVdd AGnd AGnd AVdd AGnd AVdd AVdd IoutB Iout AGnd DACBP DAC/ Reset
13 14 15 16 17 18 19 20 21 22 23 24
C11
1 µF
R5
3.85 k
(A)
(A)
R6
51
+1.8 V (A)
+1.8 V (A)
R7
51
U9
LM340AT-5.0
+9 V
Reg
In
Out
+5 V
R8
51
nc
T1
Mini-Circuits
T1-1T-KK81
R14
47
C33
0.01
Output Filter
L4
6 Turns
T50-6
L5
6 Turns
T50-6
J1
BNC
R15
3.3 k
C34
68 pF
C35
150 pF
C36
68 pF
+1.8 V (A)
+5 V
C12 C13 C14 C15 C16 C17 C18 C19 C20 C21
0.1

The multiple supply voltages required by the 9951 provided new challenges for the board layout. Analog Devices recommends a 4-layer board for this part. The top layer is the surface-mount layer, followed by a ground plane layer, power plane, and a final ground plane at the bottom. In addition to the two 1.8 V supplies and the 3.3 V interfacing voltage, a 9-V regulator was added to power the output buffer stage. This was a single-supply RF op amp (AD8005) similar to that in the 2002 article. The 1.8 V supplies, which were only necessary for the AD9951, were provided by small surface-mount, fixed-voltage regulators made by Texas Instruments.

The 3.3 and 9 V regulators were implemented with the well-known, adjustable National LM117 metal-can devices. The metal-can packaging was chosen to provide ease of heat sinking. Finally, a 5 V regulator was added to power the microprocessor, LCD display, and the shaft encoder, as my search for 3.3 V displays and shaft encoders had turned up very little.

The microprocessor used here is a recent offering by Atmel that incorporates the common 8051 instruction set. I had experience with this language and developed the assembly language software first by using an assembler from American Automation (no longer supported) and then a more recent one by Metalink. The chief attraction of the Atmel part was the 2 KB of flash EEPROM, giving the designer great expansion capability to store frequencies, implement memory stacks, and so on. The part was programmed with a Needham Electronics EMP-21. This is a new, USB-driven product. The Atmel part has a rated clock speed of 24 MHz. Faster 8051 parts such as those by Philips are available with up to 33 MHz clock ratings but without the flash EEPROM.

In the early stages of the design, I debated the use of separate clock oscillators for the microprocessor and DDS. The Atmel part is designed to operate without capacitive loading on the crystals, making it extremely attractive for a compact board. The 9951 has a feature allowing it to be driven by a significantly lower frequency clock (at U8) with the internal phase-locked loop multiplying up the actual internal clock frequency. For flexibility I chose to clock the microprocessor and DDS with separate oscillators. The spectral plots of the results have been reassuring, and stability measurements indicate only the small drift of the clock oscillator specifications, such as 50 ppm or 100 ppm. Clocking the DDS with, say, a TCXO (temperature-compensated crystal oscillator) will give even greater stability. Analog Devices states that the quality of the DDS output in terms of phase noise is directly related to the quality of the DDS clock oscillator. The one presently used is a Connor-Winfield AC52 and it clocks the DDS directly (DDS internal clock multiplier disabled) at 150 MHz. It was obtained as a development sample. The microprocessor is driven by a 20 MHz crystal.

For the best spectral purity possible there are two stages of filtering included on the circuit board. The first, a 160-MHz low-pass filter just after the transformer-coupled output from the 9951, was taken directly from the 9951 evaluation board. Analog Devices uses the transformer T1 on its evaluation board (EVB), and recommends it for the best performance. Although this small transformer (made by Mini-Circuits) is meant for surface-mount construction, I was able to solder it carefully to the board without too much trouble. The first low-pass filter uses surface-mount inductors made by Coilcraft. These were obtained as samples. The capacitor values were readily available. As I prototyped the board, I found it helpful to standardize all surface-mount parts to the "1206" size, which is large enough for practical handling but still offers a wide range of component values.

The second stage of filtering is at the very output, and is a classic two-stage low pass filter. Values were taken for a cutoff of slightly greater than 30 MHz. Other design values are in the article, "A Progressive Receiver," by Wes Hayward and John Lawson.[2]

Layout and Construction

After choosing the AD9951 for the new board, I purchased the software layout program *Eagle* (standard version), and used that to put together a layout. Although much is made of using large ground planes, I have always felt that they are not a substitute for a good layout. Much time was spent in orienting the parts to give the shortest possible lead lengths and the most direct ground return paths. Then the ground and power planes were put into the layout. Care must be taken not to "stitch" ground and power planes together with through holes when changes are made. *Eagle* automatically generates good-quality Gerber files and can be used to design a complete product. The cost of this software package was about $200.00. A library of surface-mount parts is included, as well as a component editor. As mentioned before, the AD9951 template, as well as that for the transformer, were custom made for this application.

Samples were obtained for the AD9951. There is a small square of metal on the bottom side of the 9951 package, which must be soldered to ground for best low-noise operation. This is incorporated into the assembly process. A local surface-mount assembly technician was enlisted for a small fee to hand-solder the surface-mount parts onto the prototype board. While the AD9951 and TI 79118 regulators had multiple, closely spaced leads and required the use of a professional assembler, I believe that the rest of the surface-mount parts (many of which are simply filter capacitors) could be easily soldered by hand. Tom Riley — a friend mentioned earlier — does much of this assembly using

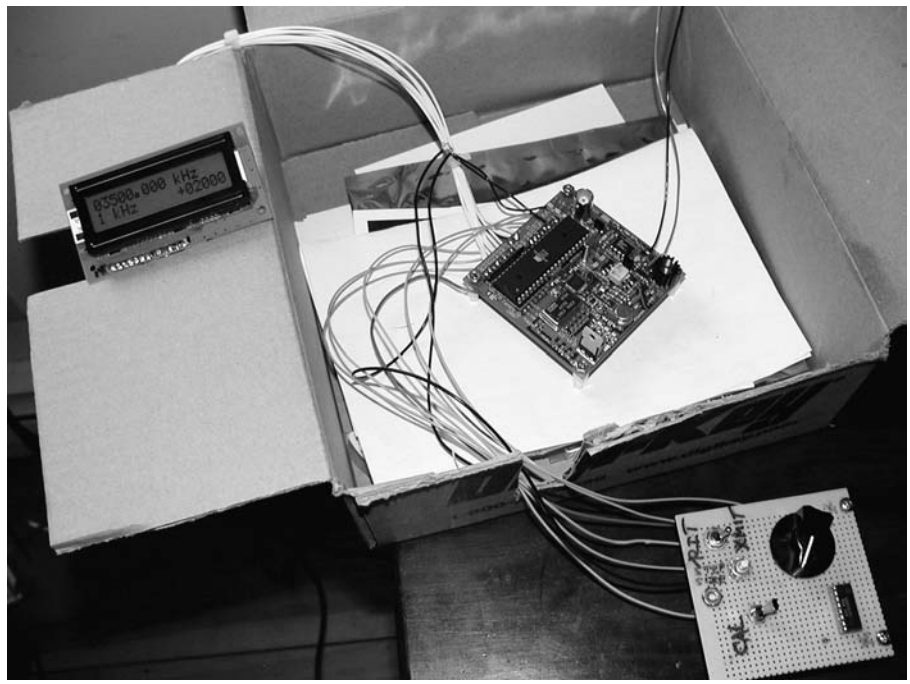


Photo B — This "Box Board" prototype shows the main DDS circuit board, LCD circuit board and the input controls wired on a piece of perf board.

tweezers and silver epoxy with good results. The larger, 1206-sized surface-mount parts make this even more possible. Through-hole parts were used whenever possible, but the 160 MHz filter was implemented with surface mount construction in order to duplicate the Analog Devices evaluation board as much as possible. Circuit boards and partial kits for the DDS VFO are available. Check the author's Web site at **www.WA1FFL.com** for the latest updates, kit options and information, and application notes for the VFO.

Prototyping has changed radically in the past twenty years, with designers often being forced to go right to a circuit board layout in order to get surface-mount components working. It has become a fact of life. Many components in the RF world are only available now in surface-mount packages. A noteworthy article by Walt Kester of Analog Devices discusses the difference in RF characteristics between a through-hole-packaged RF op amp (the AD8001) and its surface-mount equivalent.[3] Surface-mount filter capacitors are generally preferred as they have smaller lead inductance.

Testing and Results

After the board was constructed, measurements were made before connecting the display and shaft encoder. The supply voltages came up correctly the first time. Despite some minor cosmetic issues, all electrical connections were as desired. Attention was then diverted back to software development, in particular, getting the microprocessor to generate the correct control signals to download the AD9951 with the correct frequency. This was done with simple subroutines after extensively studying the 9951 control registers bit-by-bit in the data sheet. After some brief debugging, a clean 21 MHz carrier was generated at the board output. The 21 MHz output was significantly better in quality than the 10 MHz waveform on the previous VFO design. Because of the very low supply voltages on the AD9951, one must expect a much lower output voltage at the chip — on the order of 100 to 200 mV.

The spectral plots in the 9951 data sheet begin at –4 dBm, a level of only 140 mV across 50 Ω. With the output buffer in place, the board's unterminated output was about 1 V peak across most of the HF band. A 50 Ω termination on the output filter is expected for correct performance. To boost the output level even more, an external buffer amplifier may be used to supplement the VFO output stage. One that is highly recommended was described by Doug DeMaw, W1FB, in a QST article.[4] It includes another stage of output filtering and uses a 2N5179 transistor. It was originally designed by Wes Hayward, W7ZOI.

Work proceeded on the display and shaft encoder wiring, which came up immediately. A new model of shaft encoder, the Grayhill 61K64, was used. The 61K25, which has a much slower tuning rate, was preferred and obtained as a sample, but was difficult to find in stock. Another model by CUI with an even slower tuning rate (20 pulses per revolution) is being evaluated as well. It has smooth detent operation and is well-made and affordable. The VFO software was modified to allow the shaft encoder to operate as a tuning step size selection device, while a momentary push button switch is held down. While holding down the push button, the shaft encoder is rotated until the desired tun-

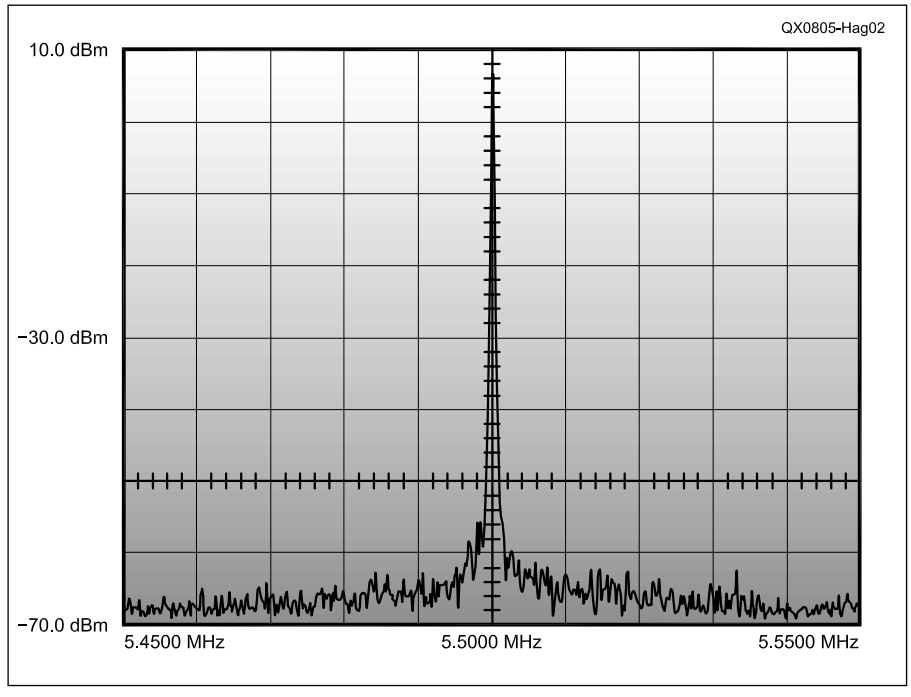


Figure 2 — This spectral output display shows the VFO operating at 5.5000 MHz. The top of the display represents 10 dBm. The input signal has been attenuated by 40 dB.

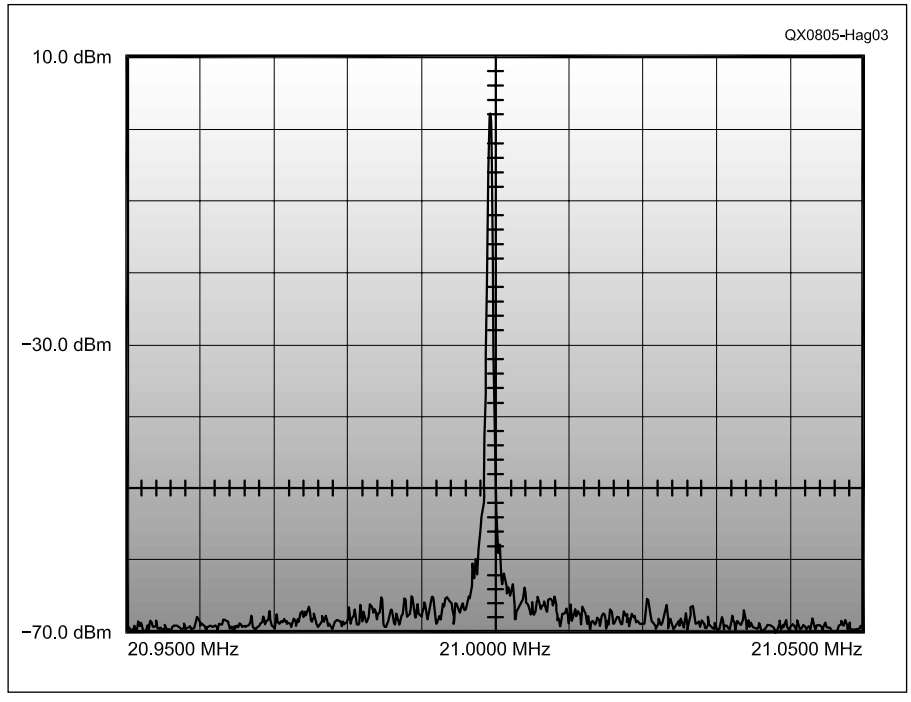


Figure 3 — This spectral output display shows the VFO operating at 21.0000 MHz. The top of the display represents 10 dBm. The input signal has been attenuated by 40 dB.

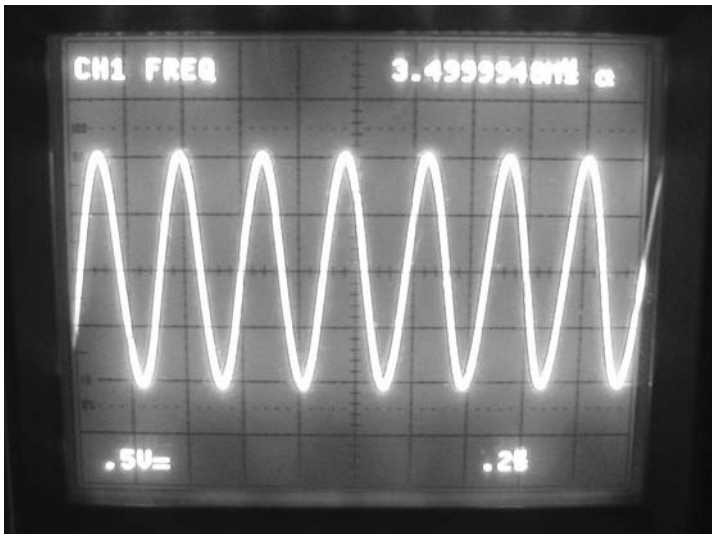


Photo C — This clean sine wave output is with the DDS VFO operating at 3.499994 MHz.

ing step is selected. Step sizes of 1 Hz up to 1 MHz are available with this design. A version of this feature using a rotary switch was also successfully implemented but put aside due to the cost and size of the switch.

The display is a standard 16 × 2 LCD with equivalent versions made by Optrex, Varitronix, and other companies. To minimize power consumption, a back-light is not used.

A software calibration feature was implemented to null out clock frequency error. Throwing the CAL switch freezes the display and allows the operator to add or subtract 1 Hz. steps until the carrier is "spot on." Then, the calibrated carrier is saved in flash EEPROM by pressing the SAVE switch. This feature thus acts like a trimmer capacitor that is implemented in software.

Another feature that was desired was receive incremental tuning (RIT) and this was programmed to appear in the lower-right corner of the display. An offset of plus or minus 10 kHz is available. The RIT display reads directly in Hz. The RIT is tuned in 10 Hz steps until the desired offset is achieved. Throwing the RIT switch back to the off position restores the carrier to its former value. Another option would be to program a separate VFO display on the bottom ("B side"). I concluded that this would be easier to program than the separate RIT because of its inherent symmetry, and have added this option to my wish list.

Most importantly, spectrum measurements were made on several example waveforms.

See Figures 2 and 3. Because of the popularity of 5.0-5.5 MHz as a local oscillator tuning range, it was desired to focus somewhat on this region. Measurements at 5.5 MHz showed a spurious-free dynamic range of about 72 dB. This could be increased with a higher clock rate (up to 400 MHz.) More measurements will be made accordingly. At 21 MHz, the SFDR was about 70 dB.

The next step will be to program in a clock multiplier of 4× for an internal DDS clock frequency of 400 MHz and perform the same measurements. This implies the use of a 100 MHz clock oscillator on the board. Other clocking methods will produce different results. The spectral plots in general, which were the very first made on this board, mirrored the narrow-band results given in the data sheet very well. More experimentation and evaluation are anticipated.

In general, the purest waveform and highest SFDR will be obtained while running the VFO at the highest possible clock frequency. The output frequencies will appear cleaner. The tightest filtering possible should be used, consistent with tolerable roll-off at the highest output frequency.

Total current drain of the board using the Connor-Winfield 150 MHz oscillator, and with the display connected, was 150 mA. Using a clock oscillator by International Crystal that operated at 100 MHz, the current drain dropped to about 80 mA, but the much lower clock frequency resulted in noticeable waveform distortion at lower frequencies, as expected. Higher frequency clock oscillators using YIG devices are available but I have not evaluated them. There are many possibilities left for experimentation.

The use of the microprocessor flash EEPROM has given even more possibilities for expansion. I recently added 16 memory storage locations for frequency configurations, with expandability to 32 memories. In addition, plus or minus keying offset is now available for CW (700 Hz) and SSB (1.5 kHz).

I eagerly await the development of DDS ICs that give full 16-bit performance at the output D/A stage, for 90 dB SFDR. New design techniques and IC technology will only improve performance.[5]

Acknowledgements

I want to acknowledge the assistance of Tom Riley, who provided the surface-mount template for the AD9951. He was also helpful in advising me about surface-mount prototyping techniques. Jeremy O'Neal saved me much time by alerting me to the zero-padding requirements of the *Eagle* drill file coordinates. Paul Mileski generously gave of his time in helping me set up spectral plots. Wes Hayward, W7ZOI, gave me valuable feedback after the previous VFO article and I appreciate his rigorous approach and his comments about the necessity for spectrally-pure local oscillators and their relationship to dynamic range. Dan Duang of Atmel and David Brandon of Analog Devices gave valuable advice on device applications. Much gratitude goes to Mitchell Lee of Linear Technology Corp for his helpful suggestions.

Notes

[1]James D. Hagerty, WA1FFL, "A Compact, Direct-Digital VFO," *QST*, Jan 2002, pp 35-38.

[2]Wes Hayward, W7ZOI, and John Lawson, K5IRK, "A High-Performance Communications Receiver," *The ARRL Handbook for the Radio Amateur*, ARRL, 1985 through 1994 editions, pp 30-8 to 30-15.

[3]Walt Kester, (Analog Devices), "Prototyping Techniques Help Verify Analog-Circuit Performance," *EDN*, Feb 15, 1996, pp 131-140.

[4]Doug DeMaw, W1FB, "Accessories For Your VFO," *QST*, Jan 1988, pp 31-34.

[5]Ken Gentile, and Roger Huntley, (Analog Devices), "Signal Cancellation Improves DDS SFDR," *Microwaves and RF*, Aug 2006, pp 120-128.

References for Additional Reading

Charles Kitchin, "Avoiding Op Amp Instability Problems in Single-Supply Applications," *Analog Dialog*ue (Analog Devices), Volume 35-2 (2001), pp 12-14.

"Exploring the Synthesizer in a Commercial MF/HF Transceiver," *The ARRL Handbook for the Radio Amateur*, 1999, pp 14.49-14.51. Describes the use of DDS in the ICOM IC-765 transceiver, as part of a multiloop synthesizer. Here, the DDS subsystem is operated at very low radio frequencies for the cleanest spectral performance possible.

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Linux under *Windows*?

Think you can't run Linux *applications on a* Windows *computer? Think again!*

I enjoy many aspects of Amateur Radio, but one of my favorites is combining two of my interests: computers and radios. Because of this, the various digital modes available hold a particular interest to me, and so I am always looking for new ways to take advantage of this technology.

In several recent *QST* "Eclectic Technology" columns, Steve Ford, WB8IMY, has discussed a new multimode HF digital software offering called *Fldigi*, by Dave Freese, W1HKJ. This program is particularly interesting because it offers many modes in one program, is free (which fits my budget perfectly!) and provides the same user interface and program for all of the supported modes. This keeps me from having to jump from one program to another to change modes and try to remember all of the various menus and commands. There was one small, little, problem, however — *Fldigi* is only available as a *Linux* program and I am running Microsoft *Windows* on my computers.

What is *Linux*?

Linux is an operating system, just like Microsoft *Windows*. It is available for free (or close to free), is based on the *Unix* operating system, and can be downloaded from the Internet. There are many different flavors of *Linux*, each with its own strengths and weaknesses. Currently, the push is to have a small package that offers all of the functionality that most users are looking for — such as Internet browsing, e-mail, and word processing applications. Amazingly, there are *Linux* flavors available that can do all of this, with nothing more than a CD (which is called a "Live CD") or USB Thumb Drive (sometimes referred to as a "Flash Drive") to hold the whole operating system. After looking at *Fldigi's* Web site, it looks like Dave has tested it on several different *Linux* versions, but I decided on either *Puppy Linux* or *Mandriva Linux*. I chose these two to try for several reasons — both offered the small *Linux* experience, with all of the bells and whistles, both offered a nice *Windows*-like interface (called *X-Windows*), and Dave had made available Live CD versions of these operating systems with *Fldigi* already installed. Since you can only have one operating system running at a time on your computer, you would have to either temporarily run *Linux* from that CD or USB-Thumb Drive, or convert the computer over to *Linux*. Or, do you?

Virtualization to the rescue

I wanted to run *Fldigi*, but I did not want to give up my current operating system, Microsoft *Windows Vista Ultimate*. I also did not want to have to boot the computer to *Linux* via a CD or a USB Thumb Drive just to run the program. I then lose use of all my other applications and my family can't use the computer at that point either.

In order to resolve this, I determined that virtualization was the route to go. Virtualization allows you to create a "separate PC" running under your current operating sys-

Figure 1 — Microsoft *Windows XP* running under Microsoft's *Virtual PC*.

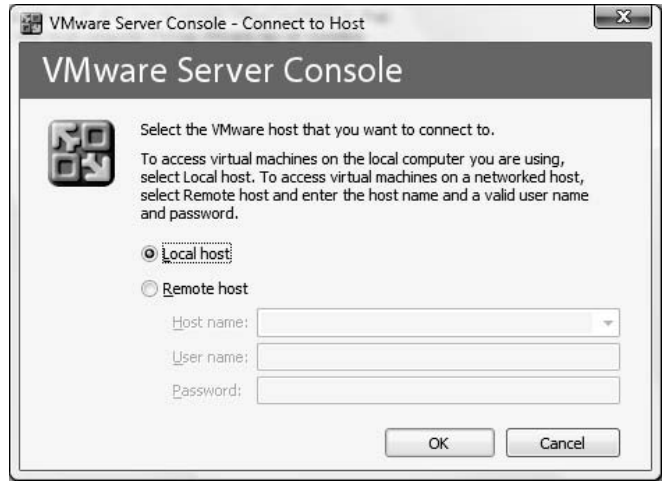

Figure 2 — *VMWare Server* Console.

tem. In other words, it creates a new machine within the machine. Fully isolated from the host operating system, it offers everything a normal PC has to offer — memory, CPU, hard drive, serial port, LAN, sound card… You name it! It literally looks and feels like you are running a new PC in a window.

There are two highly popular applications available today, which allow you to run a virtual computer and are offered free (see budget constraints above). This virtual computer could run any operating system you like, and any programs you like, while you are using your computer just like you normally do. Sounds like a great match, doesn't it? These applications are Microsoft's *Virtual PC*, available at **www.microsoft.com/windows/products/winfamily/virtualpc/default.mspx** and VMWare's *VMWare Server*, available at **www.vmware.com/products/server/**. Both of these can be downloaded and used on any recent Microsoft *Windows* versions, including *2000*, *XP* and *Vista*.

Microsoft *Virtual PC*

I first tried Microsoft's *Virtual PC* to see how it would work on my computer. I downloaded and installed it without a hitch. I decided to try a Windows *XP Professional* install first, just to see how it would work. It was easy to install the *XP* operating system following the Wizard prompts and it ran great! See Figure 1.

So, I decided to try installing both *Linux* operating systems with it. Well, after many, many tries, I could not get it to work properly. Basically, after the initial install of the operating system and when the X-Windows screen came up, the video was unusable. It appears that the *Virtual PC*'s virtual graphic card is not compatible with these two versions of *Linux*. But, not one to give up easily, I decided to try *VMWare Server*.

VMWare Server

VMWare has been producing virtualization solutions for some time, and is well respected in the computer industry. Just recently, they began offering the *Server* version of their solution free to the general public. Pretty amazing, isn't it? So, I downloaded and installed *Server* without a hitch. I decided to just jump right into installing *Linux*.

My goal was to permanently install one or both of these *Linux* options under *VMWare Server*. In other words, I wanted to install the operating system on the virtual hard drive that is provided under the virtual machine. By using this approach, I would not need to continue to use the Live CD or Thumb drive to run the operating system, could save data on the "hard drive," and could run it anytime I wanted to. So, off I went!

While both *Linux* offerings ran under *VMWare Server* without a hitch, I was only able to get *Mandriva Linux* to install onto the virtual hard drive. I am not exactly sure why the *Puppy Linux* was not able to see the hard drive correctly, but eventually, I decided that *Mandriva Linux* provided me with everything I wanted.

Using *VMWare Server*

Please note that the end goal of having *Fldigi* running on your virtual machine assumes that you have already configured your machine to interface with your radio for digital modes such as PSK31. If this is not the case, you may want to get that all set up and running before trying this. There are many articles on the ARRL Web site and the Internet on how to do this. Also, since you will be running a Virtual Machine under your current operating system, you will experience better performance if you have a fairly powerful PC. I am using a homebrewed computer, using an AMD Athlon 4400+ dual-core processor, with 2 GB of RAM and running Microsoft *Windows Vista Ultimate*. I put this machine together in January 2007, just for *Vista*. If you have been thinking about an upgrade, this may just push you to it.

After you have downloaded *VMWare Server*, you will need to install it. This can be done in a number of ways, but assuming that you downloaded the .ISO CD image, you would simply burn this to a CD and run the installation. Once installed, you are ready to go!

The install that we are about to walk through will allow you to install the *Mandriva Linux* operating system with *Fldigi* already installed. Please note that many of the selections we make below can be changed after the Virtual Machine has been established.

The first thing we need to do is download the "Live CD" version of *Madriva Linux* with *Fldigi*. You can find that at this URL: **www.mannindustries.net/pskmail/psklive_2007_2_1.iso**. Once you have downloaded this, we are ready to go. (You do not need to burn this to a CD — I have a little trick to share with you!)

Now, start *VMWare Server* and we will set up a virtual machine to hold *Mandriva Linux*.

When you first start *VMWare Server*, you are asked to select a Server Console. Just use the default, "Local host," and click "OK," as shown in Figure 2.

Next, you will want to select "New Virtual Machine" from the options. Figure 3 shows this screen. At the first dialog, select "Next." At the second dialog, select "Custom" for the "Appropriate Configuration" and click "Next," as shown in Figure 4.

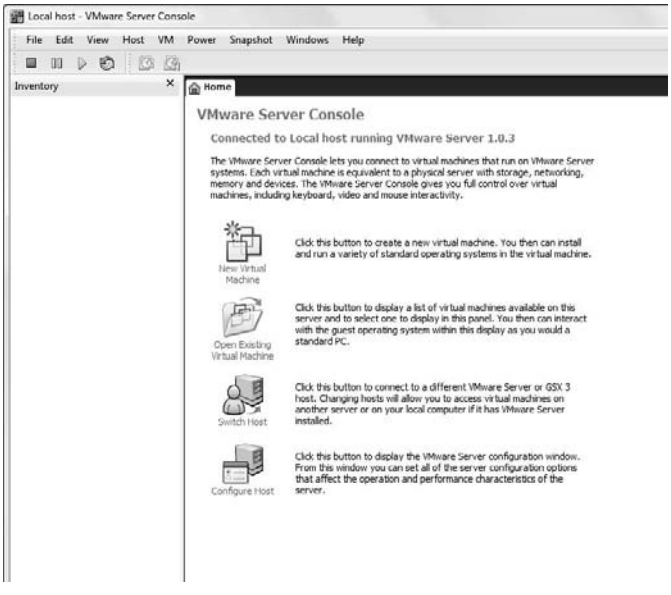

Figure 3 — *VMWare Server* **Options.**

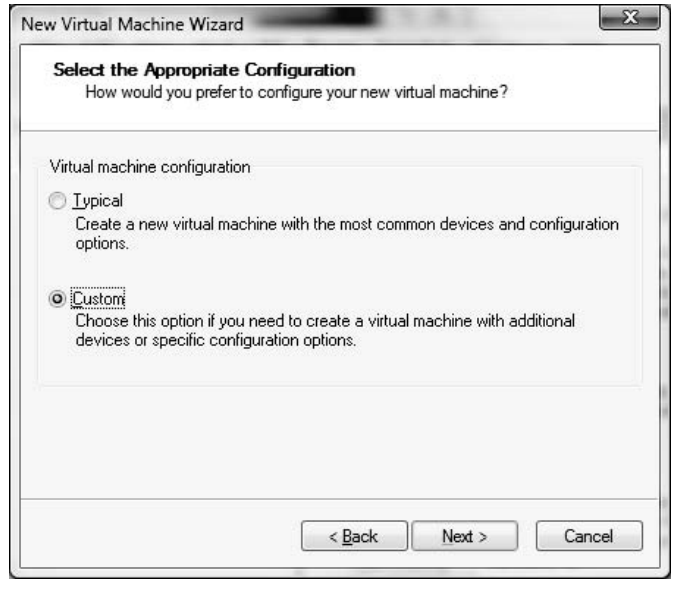

Figure 4 — *VMWare Server* **Appropriate Configuration.**

On the third dialog, select "*Linux*" as the Guest operating System, and then select *Mandriva Linux* from the Version drop down box and then click "Next." See Figure 5.

You will be prompted for a name to identify this Virtual Machine. Use any name you wish, or use the default. The same can be done for the location (using the Browse button to locate other folders in which to store the Virtual Machine). See Figure 6. Then, click "Next."

In the next dialog, simply accept the defaults and click "Next." (This dialog may not appear, depending on your operating system.) Figure 7 shows a screen shot. At the dialog screen shown in Figure 8, do the same (accept the defaults and click "Next").

The dialog screen of Figure 9 will only be presented if you are running a computer with either two (or more) physical processors, hyper-threaded processors, or multi-core processors. I have found that selecting "One" processor is the best choice for performance. Click "Next."

When you see the dialog screen shown in Figure 10, make the memory setting at least 512 if not 1024 MB of memory. (This is assuming you have enough RAM to support it. Just like with "normal" machines, the more memory you give it, the better it will perform.) Then, click "Next."

At the Figure 11 dialog screen, use the defaults and select "Next," assuming you have high speed Internet access. If you have dial-up, select the "NAT" option.

For the next dialog, simply select the defaults and click "Next," as shown in Figure 12.

Figure 13 shows the dialog screen for selecting a target disk. Simply select the defaults and click "Next."

Figure 14 is the screen for selecting the type of virtual disk to create. I recommend that you select the defaults, and then click "Next." I also suggest that you choose the defaults for disk capacity, as shown in Figure 15. Now, modify the name of the virtual drive if you wish, or just select the default and click "Finish." See Figure 16.

After this, the program will create the virtual hard drive. This will take a while, so hang in there — we are really close now! You can watch the progress bar, as shown in Figure 17, or you can take a break and get another cup of coffee. Once this is completed, we will need to modify the Virtual Machine before we can use it.

From the main *VMWare Server* screen, you

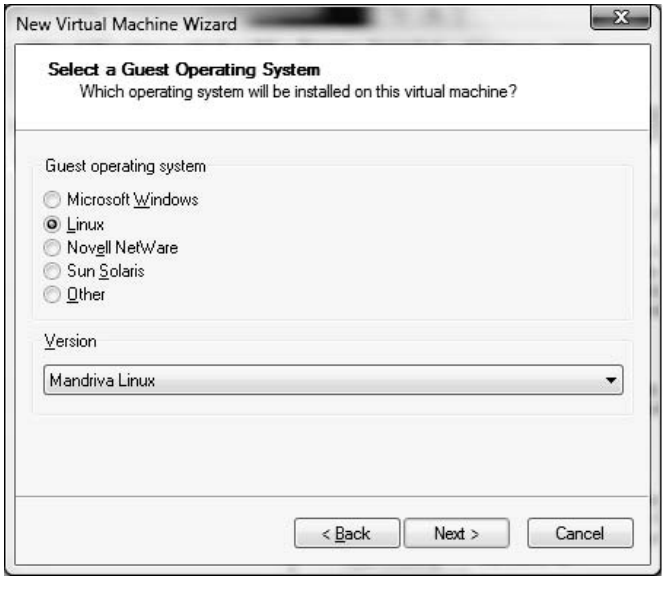

Figure 5 — Selecting *Mandriva Linux*.

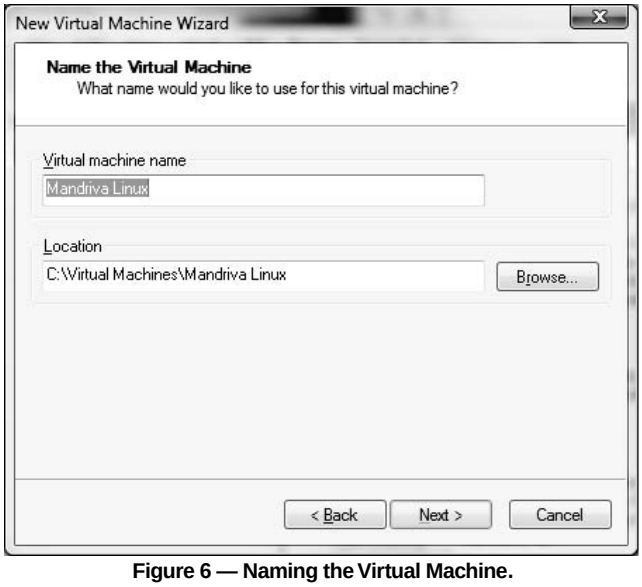

Figure 6 — Naming the Virtual Machine.

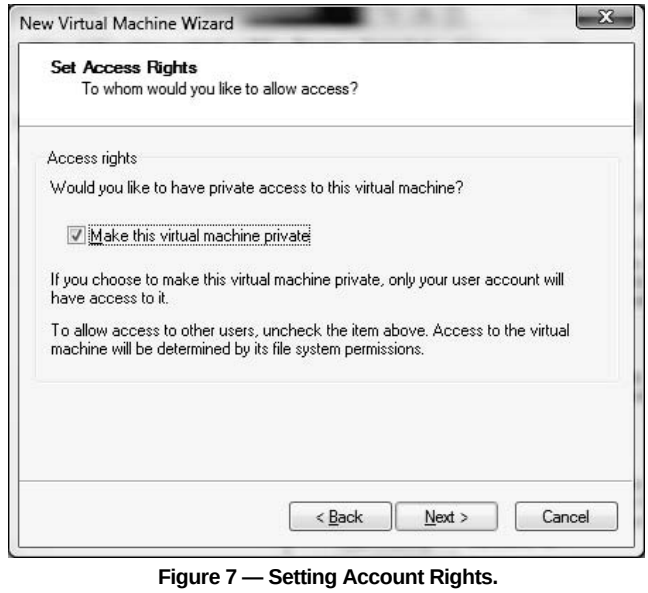

Figure 7 — Setting Account Rights.

Figure 8 — Startup / shutdown options.

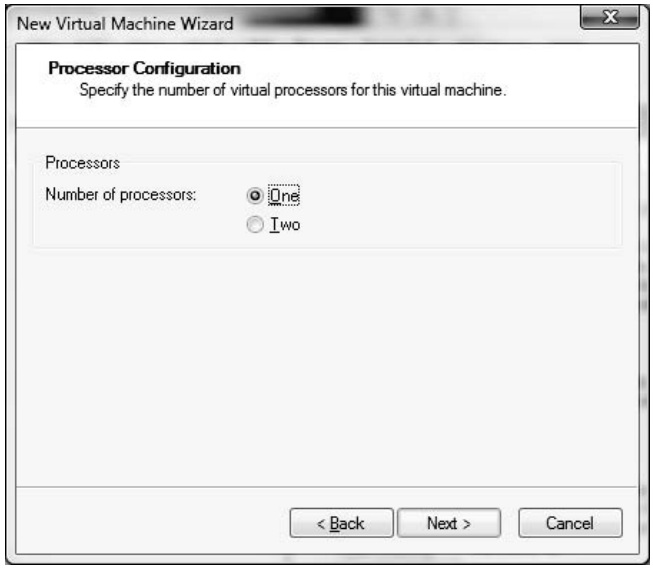

Figure 9 — Processor Configuration.

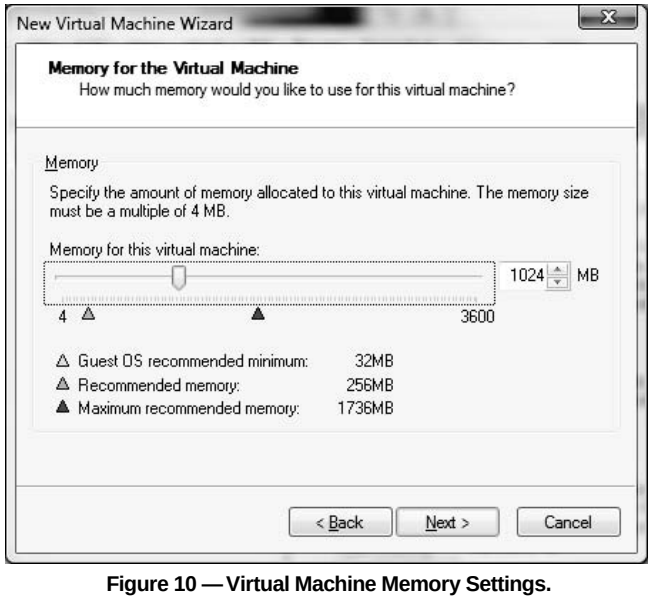

Figure 10 — Virtual Machine Memory Settings.

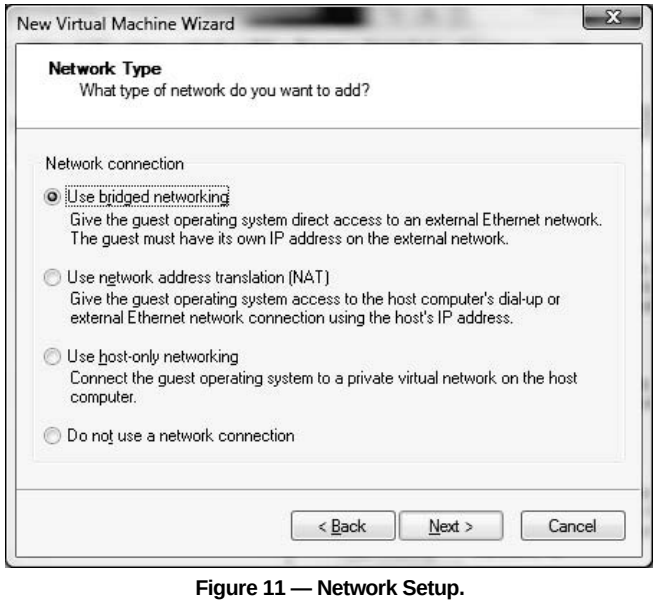

Figure 11 — Network Setup.

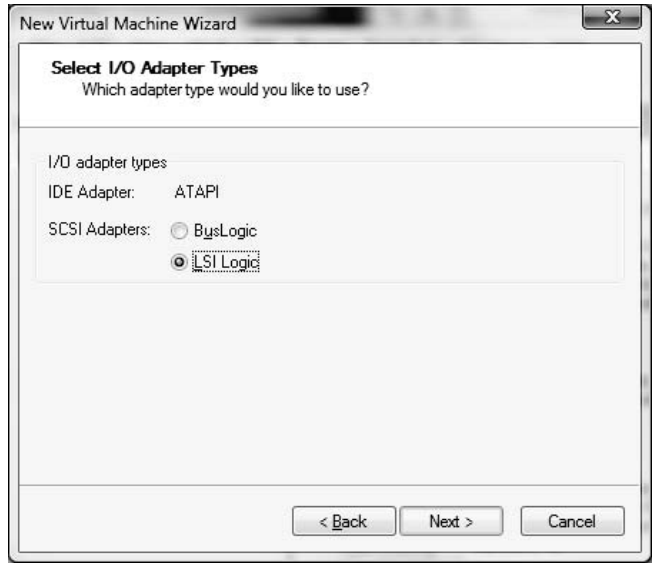

Figure 12 — I/O Adapter Setup.

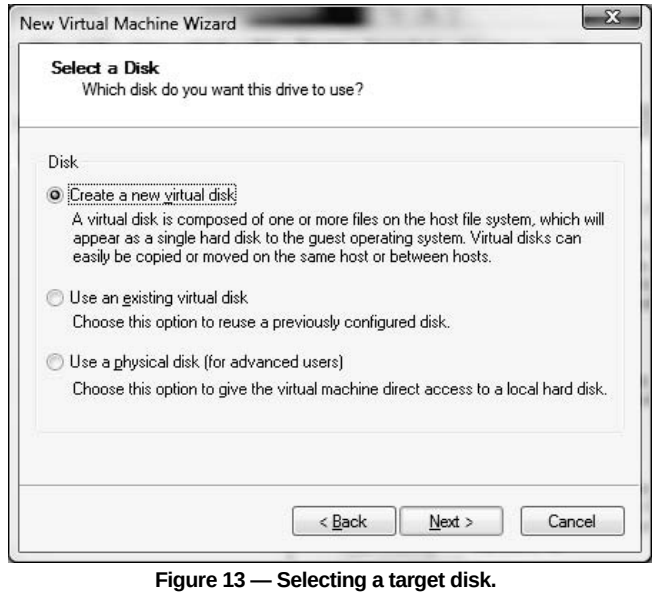

Figure 13 — Selecting a target disk.

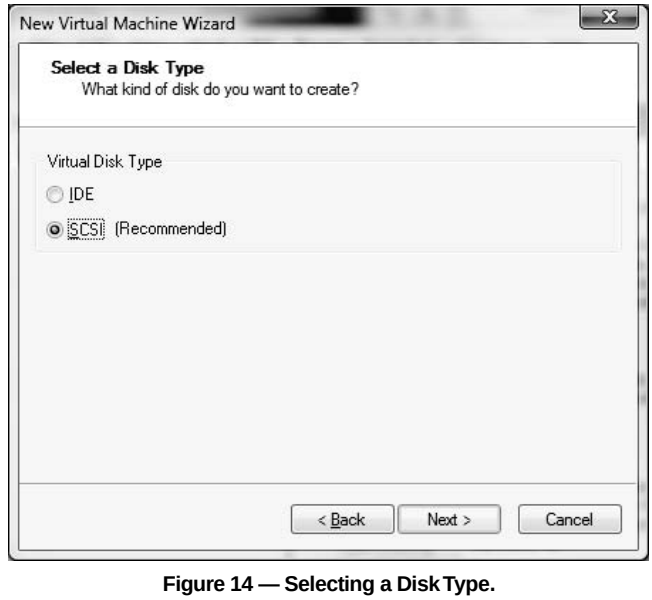

Figure 14 — Selecting a Disk Type.

will see details about your newly created Virtual Machine. We need to change the default for the CD ROM and other Amateur Radio specific needs — such as a serial port and the sound card to use with the digital modes.

First, the CD ROM: Double click on the CD-ROM (IDE 1:0) from the screen shown in Figure 18. The screen will now look like Figure 19.

Select the "Use ISO image:" radio button and then click the "Browse" button. You will need to select the psklive_2007_2_1.iso file you downloaded earlier (this is typically downloaded into your user folder and then "Downloads." If you cannot find it, don't fear — just use the *Windows* search feature to find it. Right click on the Start button and select search. Type in the above name (or just

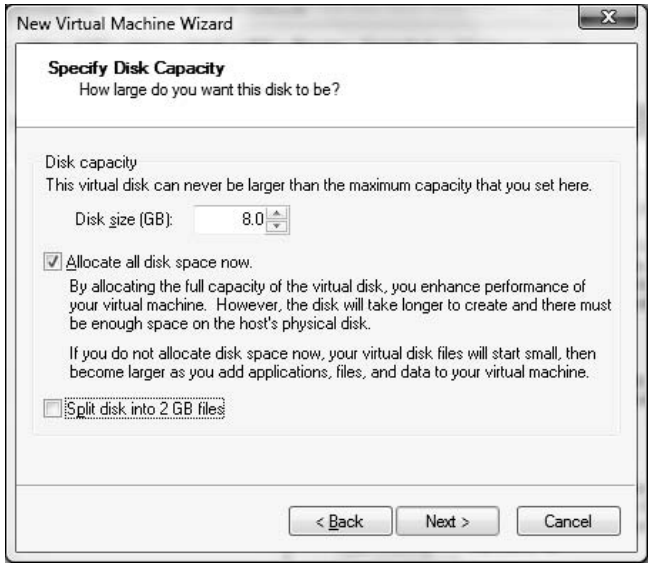

Figure 15 — Specify Disk Capacity.

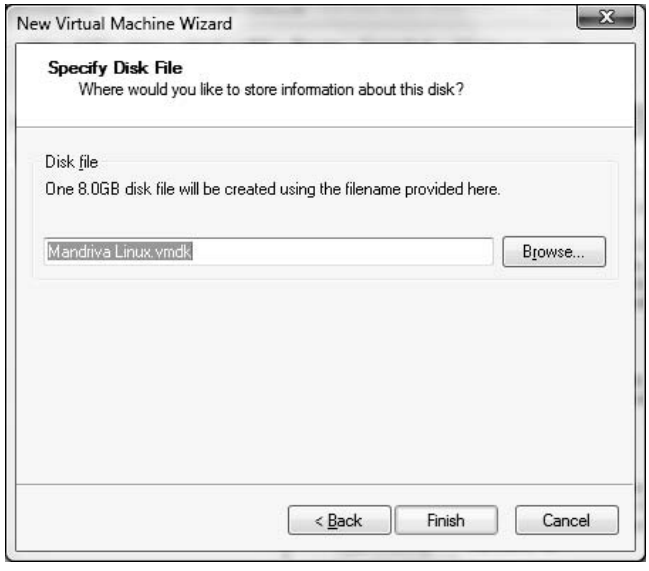

Figure 16 — Specifying a disk file.

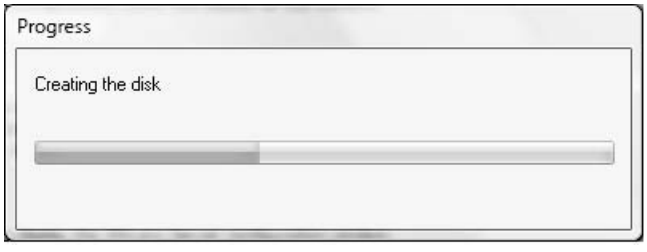

Figure 17 — The progress Bar... Hang in there!!

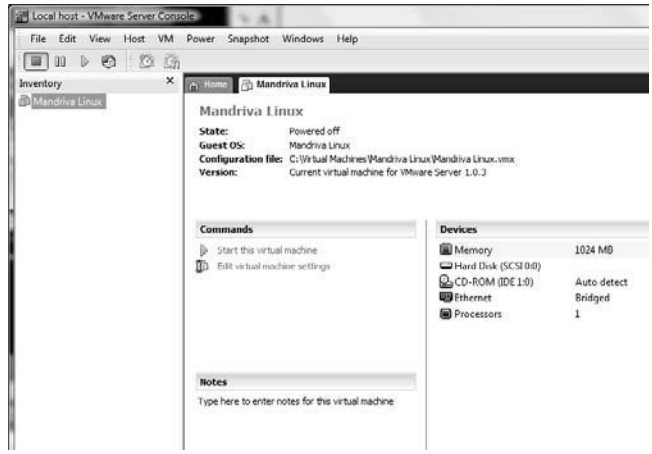

Figure 18 — Changing the DVD options.

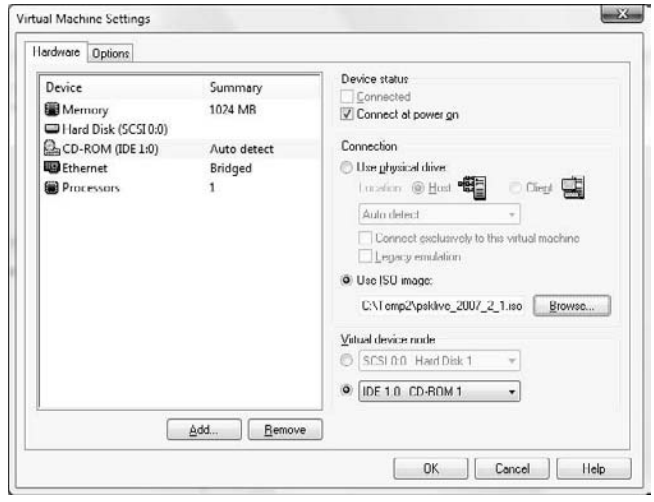

Figure 19 — Selecting the CD-ROM/DVD settings.

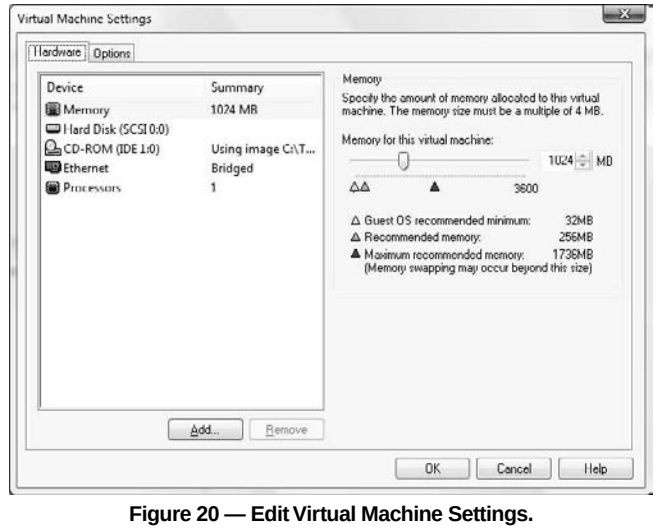

Figure 20 — Edit Virtual Machine Settings.

*.iso to make it even easier). Be sure to search all of your hard drives — from the drop down option, and click "OK." Now, just let it search until it finds the file. Then, click "OK."

Here is the little trick I told you about earlier. Basically, with *VMWare Server* and *Virtual PC*, you can load a CD or DVD image without having to create an actual disk. This is a really nice feature, because that way, you can try all kinds of different operating systems, or even software, without having to burn the disk.

Okay, next we need to add the serial port and sound card, as shown in Figure 20. Now, click on "Edit virtual machine settings" and at the next dialog screen, click the "Add" button. A wizard will start up and walk you through the process. See Figure 21.

Select "Serial Port" and click "Next." Accept the defaults on the next two screens and click "Finish." This will place COM1 (serial port 1) in your Virtual Machine. Now, click "Add" again and this time select "Sound Adapter." Click "Next" and on the next screen, click "Specify sound adapter" and select the sound card you wish to use. Then, click "Finish." Follow the same process if you wish to add other ports, such as the parallel port, for other features, such as radio control or printing. Now, we have the Virtual Machine all ready to go. Click "Start this virtual machine." It will look just like a new machine is starting and will begin loading the contents in the "CD" (our *Mandriva Linux* "Live CD"). Figure 22 shows the new screen.

When the machine stops at "Boot:" press Enter (or wait and it will start it for you). This will begin loading the *Linux* operating system. (Also, note the icons at the bottom right of the *VMWare Server* screen. These icons show you what devices are available to you and the activity of the CD or hard drive. You may need to use the *VMWare Server* scroll bars to see this information, depending on your host's screen resolution.)

Once it has loaded, you should see the *Mandriva Linux* window ready for you to use, as shown in Figure 23.

Now, you can certainly begin to use and play with this Virtual Machine. Remember, however, that you will not be able to save any of your changes. So, when you are ready, let's load the operating system to the Virtual Machine's hard drive. Click on the star icon on the lower left. (You may have to click twice to get your mouse to click the star. This is because the Virtual Machine has to "capture" your mouse and keyboard so they work in the Virtual Machine. If you want to go back to the Host Machine — your normal machine — simply click the ALT and CTRL buttons together.)

Now, select the MCN Live menu option, and

Figure 21 — Hardware Type Selection.

Figure 23 — *Mandriva Linux* **Up and Running!**

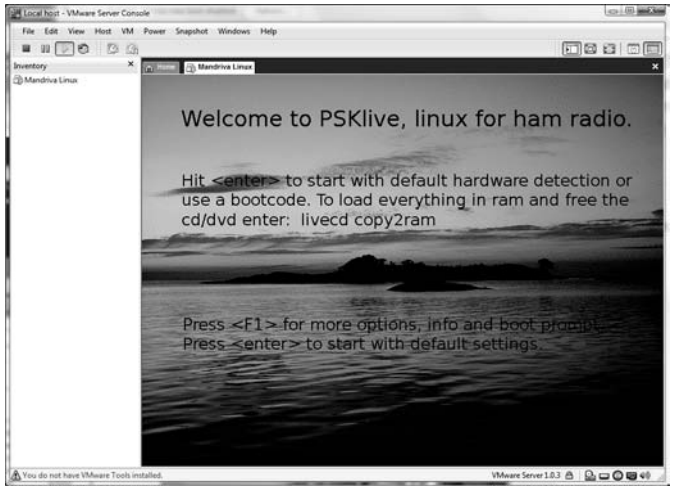

Figure 22 — *VMWare Server* **Starting a Virtual Machine.**

Figure 24 — Configuring *Mandriva Linux***.**

then click on the "Install to HD (not suited for *Vista* dual boot)" option. You will be prompted for a password. The default password is "root," so just type that in and click "OK."

This will start another wizard to complete the installation. On the first dialog, click "Next." Then, on the next dialog, use the defaults and click "Next" again. It will then format your Virtual Hard Drive. (Don't worry — this isn't your main hard drive!) Then, it will begin the copy process. Watch the icons on the bottom right — you will see the "CD ROM" and "Hard Drive" icons going to town. After it is done copying the files, on the next dialog, use the defaults and click "Next." On the following screen, click "Finish" and on the final screen, click "Finish" again. Guess what? You have now installed *Mandriva Linux* to the Virtual Machine!

Now we are ready to reboot the Virtual Machine, so we can run it from its hard drive. Press the ALT and CTRL buttons together to release the mouse and keyboard. Right under the "File" menu for *VMWare Server*, you will see a series of control buttons like you might find on a tape or CD player. See Figure 24.

The control button on the far left, the little red Stop button, will shut down the Guest machine. Please click that and, once it has been shut down, you will be returned to the *VMWare Server* screen. Now, we will need to modify the CD-ROM setting one more time so the computer will no longer load the ISO image (otherwise, we will just be starting the Live CD again and we want to run from the hard drive). So, double click on the "CD-ROM (IDE 1:0) again and change the Connection to be "Use Physical drive" and then, on the drop down menu, select the drive letter associated with your CD-ROM drive. Typically, this is drive D. Figure 25 shows the configuration screen. Then, click "OK."

Once that is done, click "Start this virtual machine" again. *Mandriva Linux* will now boot from the "hard drive." Pretty cool, huh?

Running *Fldigi*

Once your Virtual Machine is fully up and running, you have a full *Linux* operating system running in the Virtual Machine. Of course, you could play with Internet Browsing, Open Office, and all of that, but let's jump right into the more important piece — the *Fldigi* Amateur Radio program! There are two ways to start it — from the desktop or from the star start menu. (You will find that the normal *Windows* keyboard commands, like ALT-TAB, will work the same under *Linux*. Also, note that all mouse clicks only require one click. I learned this by having two *Fldigis* running the first time.) But, whichever way you prefer, start up *Fldigi*. When it starts, you won't see it doing a lot, as it has not yet been configured.

Click on "Configure," then "Defaults," and then "Interface" (this is probably the hardest part). See Figure 26.

Select the radio button "TTY" (it will turn

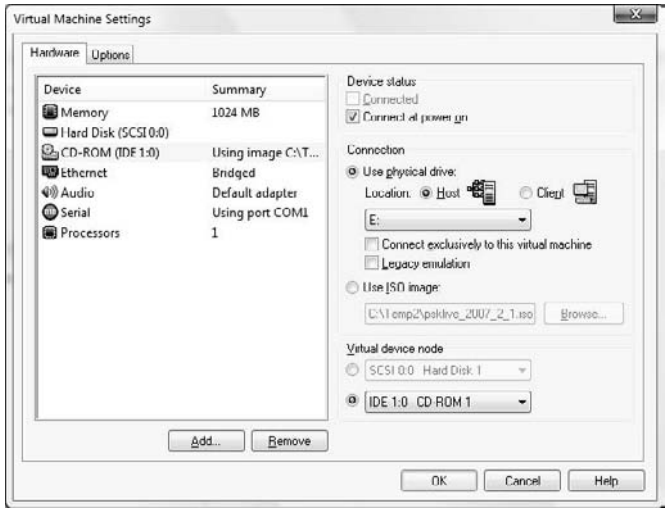

Figure 25 — Configuring the CD-ROM / DVD.

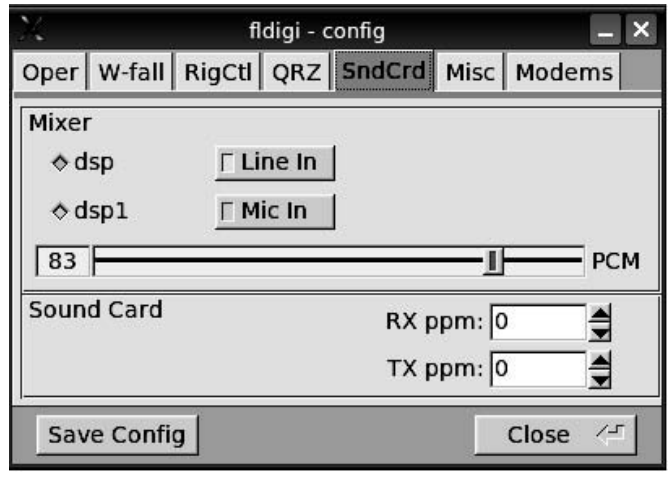

Figure 27 — Configuring the Sound Card.

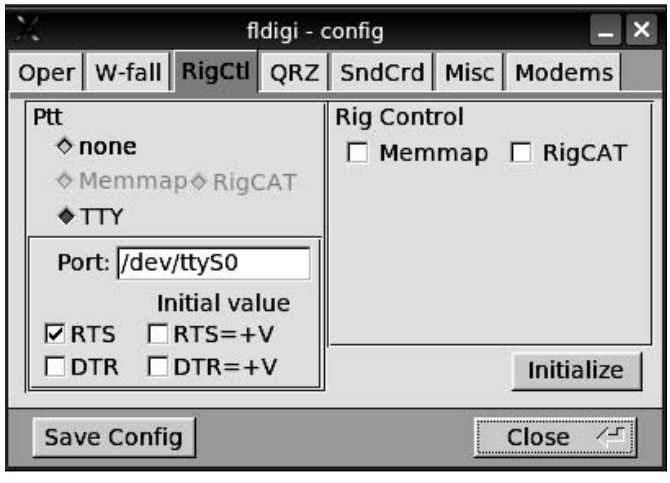

Figure 26 — *Fldigi* Configuration.

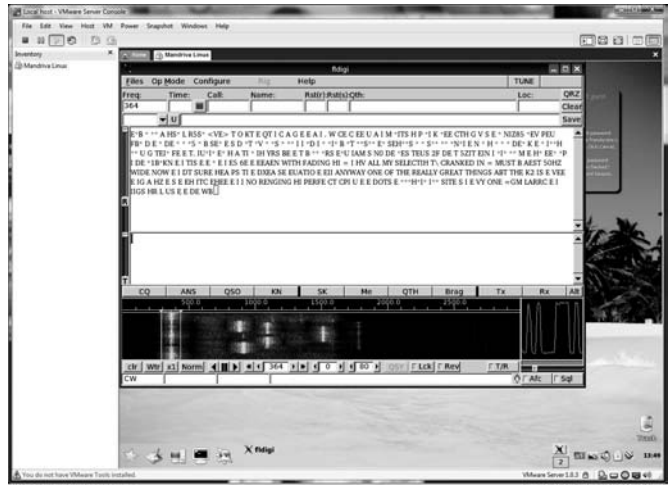

Figure 28 — *Fldigi* — it RUNS!

red), then type /dev/ttyS0 (that is a capital S and the number zero), click "Initialize" — your radio will probably go into transmit for a second — and then click "Close." Now, you may already be seeing something in the waterfall display. If that is the case, there should not be a need to configure the sound card. If you need to select Mic In or Line In, you can do that by configuring the sound card. From the main menu, click on "Configure," then "Defaults," and then "Sound Card." Select the input source that you would like to use. Figure 27 shows the sound card configuration screen. (Please note that you can also adjust the volume by clicking on the little speaker icon on the lower right of the screen — just like in *Windows*. Interestingly, the interface is very much like *Vista*.)

Once you have selected your correct input, click on "Save Config" and click "Close." When all of that is completed, click on "Configure" again from the main window and select "Save Config." There, the basics are done. Now, you can enjoy the features of *Fldigi*! See Figure 28 for the final success. (By the way, it really does have a nice CW feature.)

Conclusion

Well, it looks like I can have my cake and eat it too! With a very budget friendly solution, I can now run *Linux* while I am also running my normal *Windows* operating system. With *Fldigi*, I am able to use my computer for all kinds of different modes, without giving up anything that I may have on my "normal" computer. I am very happy with the end result and encourage you to try it as well. The uses of this are quite vast and I hope that you explore more ways to take advantage of this type of setup. We walked through setting up a *Mandriva* version of *Linux*, but there are many, many other options available. For example, I have been running *Windows Vista* for quite some time, and am very happy with it. But, if you haven't felt that you could jump right into it, why not try it out under *Windows XP*? Just use either of these virtualization solutions (*Virtual PC* will probably work just fine for this) and try it out. Also, remember that you can have many different virtual machines set up. So, you can be running *Vista* as your main operating system, then have *Mandriva* and *Fldigi* running for your Amateur Radio applications, but then have *Windows XP* up for that one piece of software that doesn't run under *Vista*. The combinations and possibilities are almost endless! Well, except for the limitation of the computer's RAM, CPU, and your imagination!

Robert Kluck, N4IJS, holds an Amateur Extra class license, is a ARRL Life Member, and has been licensed since 1982. He has been working with computers for many years, both professionally and personally, including development work under several operating systems, including Windows *and* Unix (Linux). *He enjoys many aspects of Amateur Radio, is active in his local club, and is a certified NOAA Weather Spotter, participates in WARN, and is also a VE. His wife, KI4NRG, and father, WN4W, are also licensed hams. Robert has 4 children, aged from 15 years to seven months old.*

QEX

In the Next Issue of QEX

Al Christman, K3LC, discusses various "Ground System Configurations for Phased Vertical Arrays." The article examines ground systems for two-element cardioid-pattern arrays as well as the widely used four-square array. Al's computer analysis indicates that, for a given total length of wire, some configurations perform much better than others.

Cornell Drentea, KW7CD

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The *Star-10* Transceiver — Part 3

In Part 3 of this series we conclude with the remaining circuits used in this high-performance transceiver, along with the final test results, which support the specifications presented in Part 1.

KW7CD Photo

This photo shows a back view of the *Star-10* transceiver prototype during final assembly. The sensory electronics are shown on the left, the power linear amplifier assembly (with fans on the heat sink) is in the center, and the master reference unit (MRU) is on the right.

Mission

The *Star-10* transceiver has been a unique research experience into understanding what can be done from the laws-of-physics point of view in receiver and transceiver dynamic range performance. This research has been performed over a period of five years, with parts, technologies and packaging means available to me at the time. The transceiver has been implemented with some unique parts that may no longer be available. The *Star-10* development has been a purely scientific endeavor intended primarily to understand what could be done to achieve ultimate receiver performance. Although the results have been outstanding, slightly better results may be possible using newer technologies and parts. The *Star-10* project was not intended as a product. Its duplication is probably not economically feasible.

Errata

We regret that several errors have crept into the first two parts of this series. In Part 1, the power supply specification incorrectly listed the TX max dc power as 800 VA. The correct specification is 450 VA. Also in Part 1, the caption with the lead photo of the *Star-10* transceiver indicated that the electrical and mechanical design features a modular approach using eighteen double sided, plated through printed circuit boards housed in machined, *irradiated* aluminum assemblies. That text should have said that the circuit boards are housed in machined, *irridated* aluminum assemblies. Irridation is a chemical process by which the aluminum is etched to give it a frosty, textured surface that is fingerprint resistant.

In Part 2, an incorrect photo swap occurred after the issue went to the printer. The lead photo for Part 2 was intended to be a view inside the radio with the top cover removed. Instead, that photo shows a view inside the radio with the bottom cover removed. The caption does not describe what you see in the photo. (The correct photo — and caption — appear in the version of the article posted to the *QEX* Web site at **www.arrl.org/qex/2008/03/Drentea.pdf**. The correct photo is also reproduced here as Photo A. Visible from the left are the FSYNTH assembly (left side panel), the IF75BC assembly (top left), the automatically switched half-octave receiver band-pass and transmitter high power, low-pass filter bank assembly, and the DFCB command and control assembly and keypad mounted on the back of the front panel. Front panel, side panels, top and bottom are removable, allowing access to the assemblies.

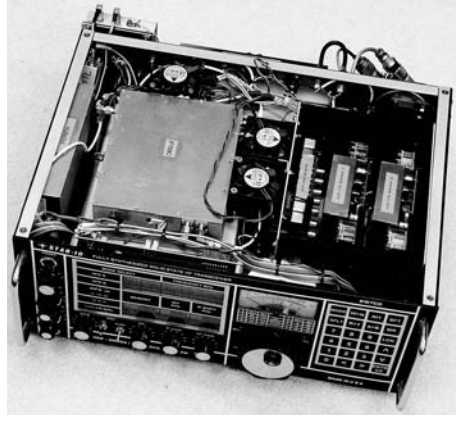


Photo A

On page 33 of Part 2, near the top of the center column the text says "The synthesizer in Star-10 goes a step further by generating the LO frequencies at ten times the required frequency range, or 770 MHz to 1050 MHz for improved phase noise performance after a division by 10, which facilitates a 6 dB improvement at the divided down 77 MHz to 105 MHz." The improvement in phase noise performance is 20 dB, not 6 dB—*Ed.*

Introduction

In Part 1 of this series, I presented a system design criteria for a modern double conversion transceiver, namely the *Star-10*. [Part 1 appeared in the Nov/Dec 2007 issue of *QEX*. That issue is currently out of print, but the *Star-10* article was the sample article from that issue. It is available on the *QEX* Web site at: **www.arrl.org/qex/2007/11/drent.pdf**. — *Ed.*] A complete discussion of how the transceiver works was also presented along with an introduction to the technologies used in the transceiver development. Also, in Part 1, I presented a set of predicted and actual performance specification numbers for the developed transceiver. A block diagram of the entire system was introduced in Figure 2 and ample composite dynamic range and system spurious analysis were presented in Figures 3 A, B, C and 4 A and B. In Part 2 of this series, I discussed in detail, the design and development of several major assemblies for the *Star-10* transceiver, particularly the IF75BC, BILAT AMP, FL75, FSYNTH, MRU, Half Octave Filter Banks, IF9BC,

DFCB and the IF9RX. [Part 2 of this series was published in the Mar/Apr 2008 issue of *QEX*. That part of the article is also available on the *QEX* Web site at: **www.arrl.org/qex/2008/03/Drentea.pdf** — *Ed.*] I will next discuss the remaining assemblies, along with final thoughts regarding their development, key performance results and lessons learned from the entire project experience.

Product Detector Audio Frequency Assembly (PDAF)

Referring to Figure 2 from Part 1, the PDAF assembly provides final receiver conversion to audio frequencies of the detected signals after they have been filtered and conditioned (AGCed) for final detection in all modes of operation. A properly shifted BFO signal is provided from FSYNTH depending on the mode being used and commanded through the DFCB assembly. The PDAF assembly contains a high-level product detector using a class II mixer, a BFO buffer amplifier (another CA2832) providing injection to both the product detector and the transmitter mixer in IF9TX. An audio amplifier follows the product detector. In addition to audio amplification, it provides audio mixing functions in order to integrate audio feedback signals from the microprocessor as well as the CW side tone signals. A schematic diagram of the PDAF assembly is shown in Figure 27. The actual PDAF assembly implementation is shown in Figure 28.

Looking at Figure 27, the BFO signal coming from FSYNTH enters the PDAF assembly at J1. It is immediately amplified by the class A amplifier, U1, another CA2832 unit. This amplified BFO signal is further split by A1, which is a Mini-Circuits PSC2-1 part. Half the signal is passed on to J3, which distributes it to the transmitter mixer on IF9TX. The other half goes through a pad made of R4, R5 and R6 and is input to MIX 1, a high-level class II, SRA-1H mixer that serves as the product detector. This mixer was purposely selected for this function, as it is suitable for baseband frequency response output, compatible with audio frequencies, and has a reported IP3 of +28 dBm.

The conditioned 9 MHz IF receiver signal coming from IF9RX is input to the product detector mixer at J2. The mixed down audio product is matched and filtered via L1, C4, R7, R8, C5, L2 and C6, and is further processed by Q1 and U2 to be finally presented to U3, a TDA2003 audio block and output at J4-B. The L2, C5 and C6 audio low-pass filter is intended to suppress noise beyond 3 kHz. Tones from the CW side tone generator along with various feedback tones coming from the DFCB command and control

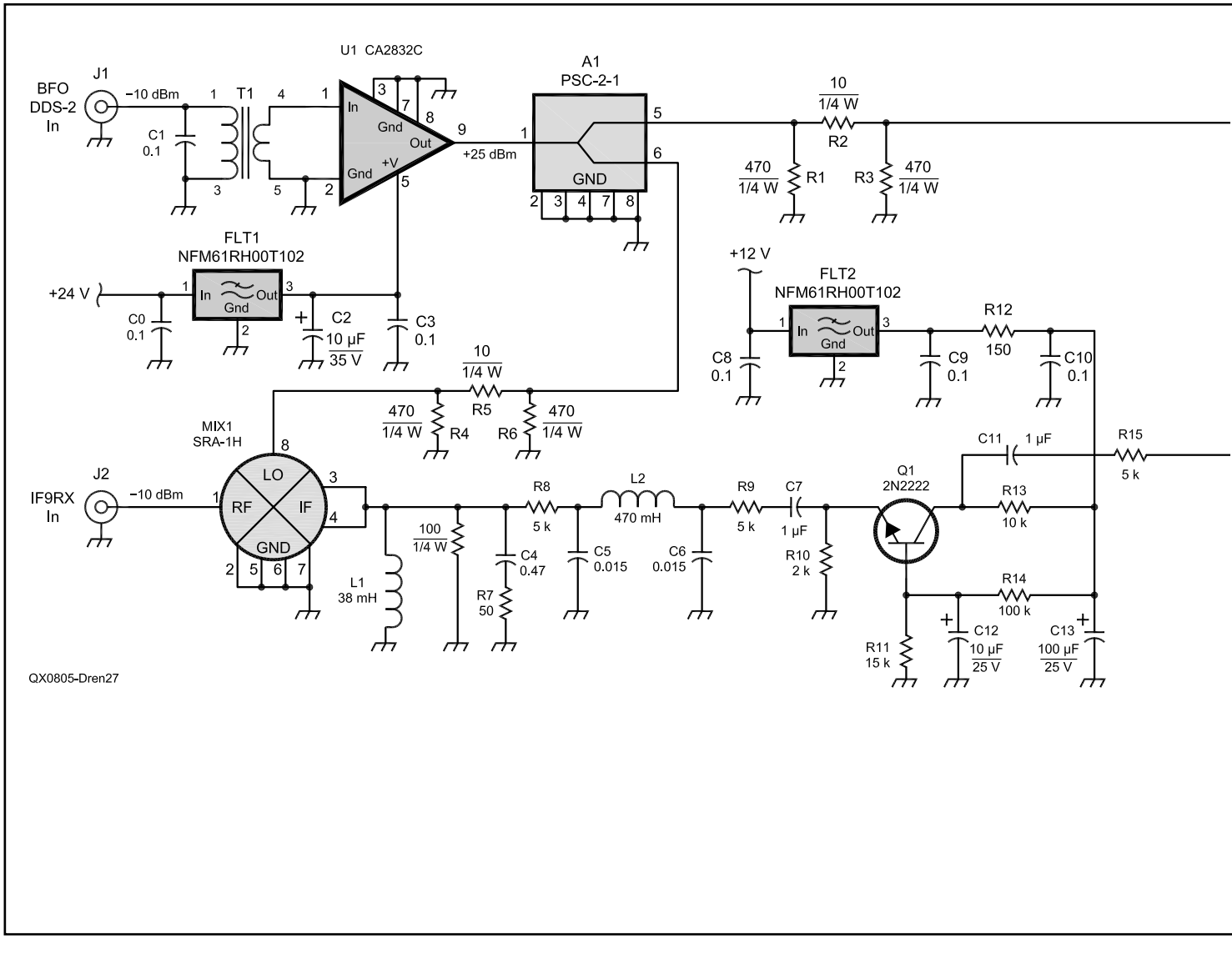


Figure 27 — Schematic diagram of the product detector audio frequency (PDAF) assembly.

assembly are audio-mixed and injected in this circuit via the J4-A connector as shown. In addition, volume control wires from the front panel audio control are input via this connector along with the MUTE signal from the T/R assembly, which silences the receiver via Q2 when transmitting.

Digital Signal Processing

Digital signal processing (DSP) can be implemented with the *Star-10* at baseband audio frequencies as shown in Figure 2 of Part 1. This can add further refinement to the transceiver's performance.

For DSP, I used the Silicon Pixels 16-bit DMA — Chroma SOUND, Audio DSP software, V 0.19 (**barberdsp.com/**). This requires the addition of a PC with a full duplex 16 bit sound card with the software installed.

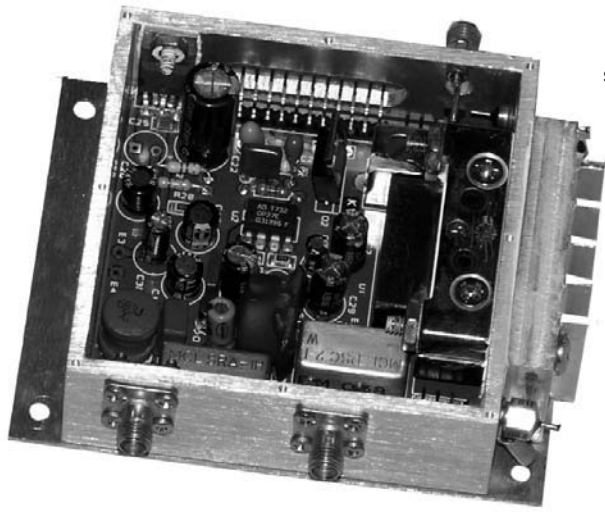
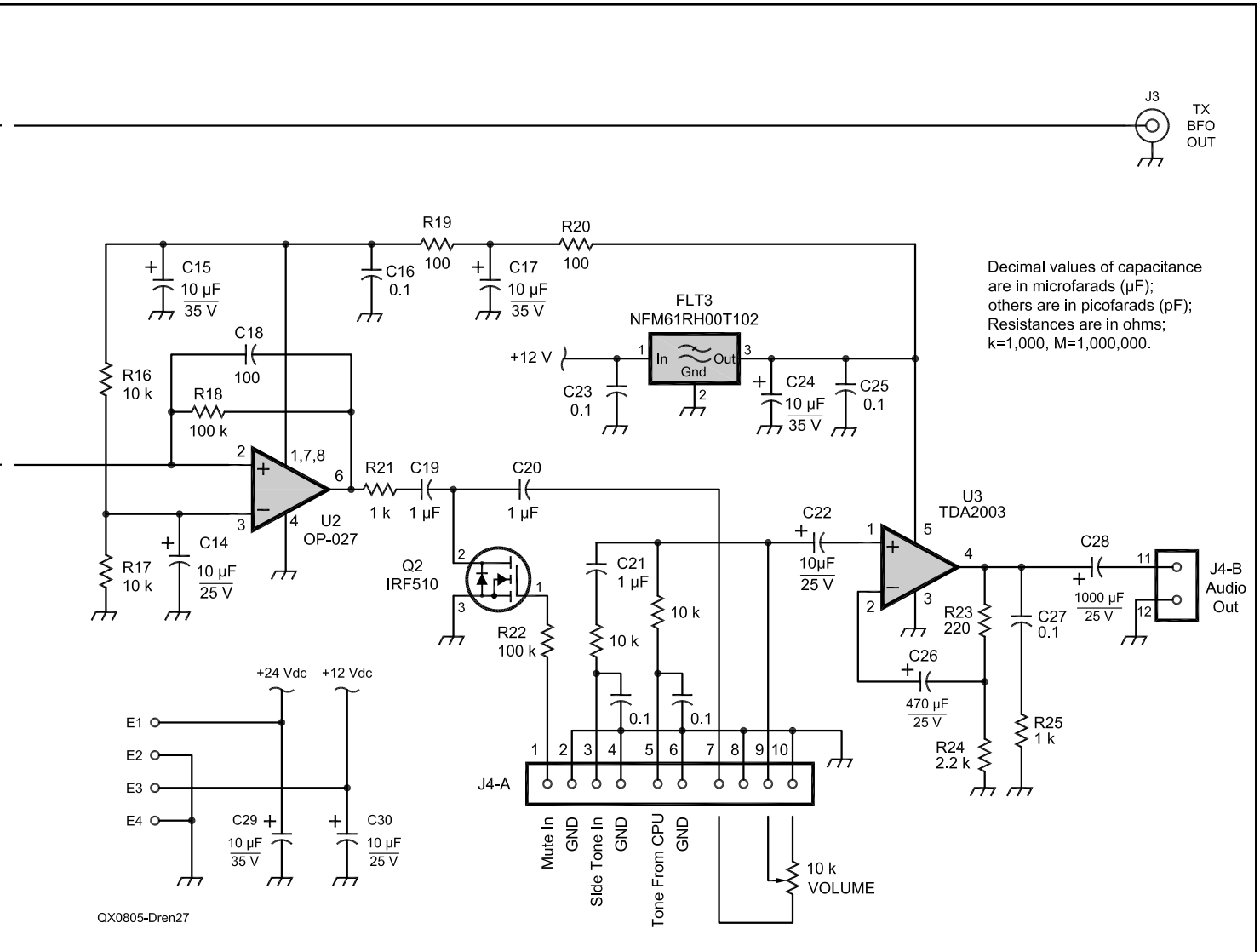


Figure 28 — This photo shows the implementation of the PDAF assembly. Visible at the right is the class A amplifier (another CA2832), which buffers the BFO signals for both, the receiver product detector mixer, as well as the transmitter mixer. The product detector is a high level class II mixer (SRA-1H), which is visible at the bottom right. The audio amplifier chip (TDA2003) is visible at the top left side of the assembly. Various other circuits are also visible.



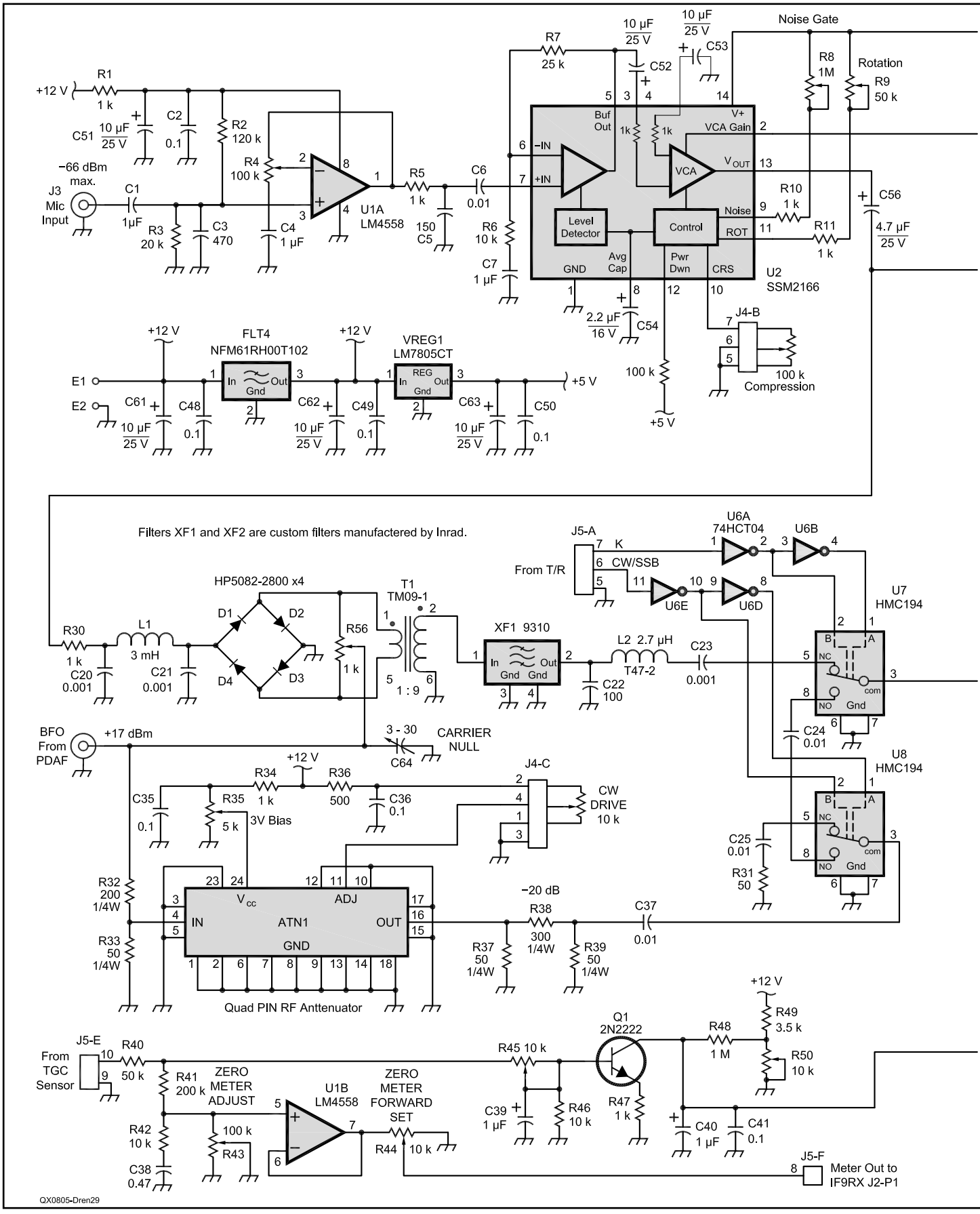
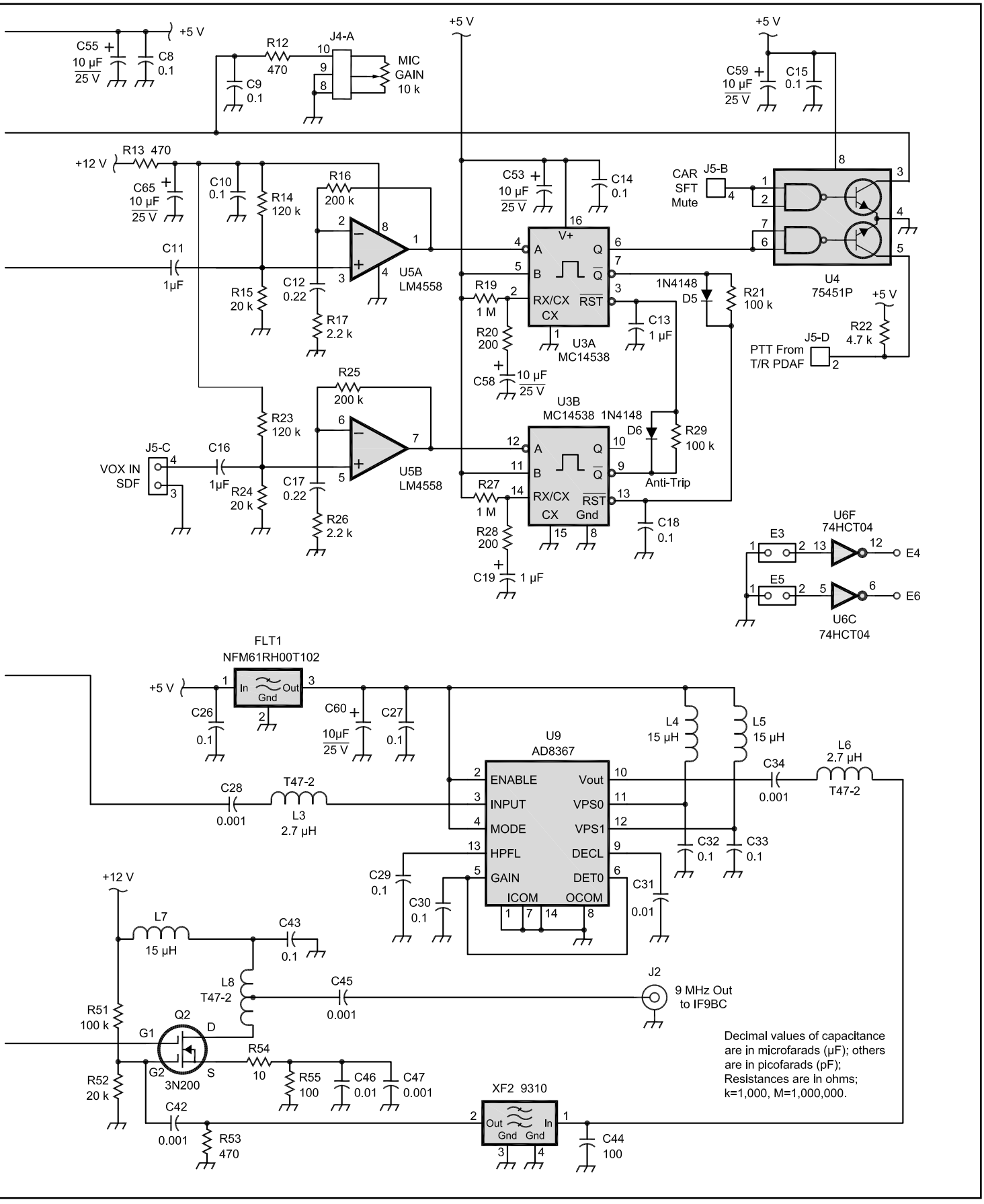


Figure 29 — Schematic diagram of the IF9TX assembly. IF9TX performs all key transmitting functions as commanded by DFCB and using the BFO signals from the FRU — FSYNTH.


+5 V
C55 10 µF 25 V
C8 0.1
R12 470
C9 0.1
J4-A
MIC GAIN 10 k
C59 10 µF 25 V
C15 0.1
+12 V
R13 470
C65 10 µF 25 V
C10 0.1
R14 120 k
R16 200 k
C11 1µF
R15 20 k
C12 0.22
R17 2.2 k
U5A LM4558
C53 10 µF 25 V
C14 0.1
U3A MC14538
R19 1 M
R20 200
C58 10 µF 25 V
C13 1 µF
CAR SFT Mute
J5-B
U4 75451P
1N4148 D5
R21 100 k
J5-D PTT From T/R PDAF
R22 4.7 k
R23 120 k
R25 200 k
R24 20 k
C17 0.22
R26 2.2 k
U5B LM4558
J5-C VOX IN SDF
C16 1µF
U3B MC14538
1N4148 D6
R29 100 k
Anti-Trip
R27 1 M
R28 200
C19 1 µF
C18 0.1
U6F 74HCT04
U6C 74HCT04
E3
E4
E5
E6
FLT1 NFM61RH00T102
In
Out
Gnd
C26 0.1
C60 10µF 25 V
C27 0.1
U9 AD8367
ENABLE
INPUT
MODE
HPFL
GAIN
Vout
VPS0
VPS1
DECL
DET0
ICOM
OCOM
L4 15 µH
L5 15 µH
L6 2.7 µH
C34 0.001
T47-2
C28 0.001
T47-2
L3 2.7 µH
C32 0.1
C33 0.1
C29 0.1
C30 0.1
C31 0.01
L7 15 µH
C43 0.1
L8 T47-2
C45 0.001
J2
9 MHz Out to IF9BC
R51 100 k
Q2 3N200
G1
G2
D
S
R54 10
R55 100
C46 0.01
C47 0.001
R52 20 k
C42 0.001
R53 470
XF2 9310
C44 100
Decimal values of capacitance are in microfarads (µF); others are in picofarads (pF); Resistances are in ohms; k=1,000, M=1,000,000.

This excellent software is intended for *Windows 95/98/NT/2000/XP* and can provide a lot of additional functionality for the transceiver. Among the functions are: Noise reduction of SSB signals, automatic notch filtering for removing tones, band pass, low pass, high pass, and band stop (manual notch) filters. Filters can be user-defined, using the built-in graphical filter designer. Additional functions can be selected. Among them are pre-defined filters. One can just drag a filter from the design window to an empty button, and a new filter bandwidth can be designed into the menu. In addition, an AGC function can be selected. Since there is no such thing as a perfect AGC circuit, this can temper possible shortcomings in the previous analog AGC circuits of the transceiver under varying conditions.

The Chroma SOUND software addition further improves the already outstanding performance of the *Star-10*, which benefits from good image rejection due to the transceiver's high first up-convert IF, and a well behaved RF/IF signal processor, using up to 32 poles of cascaded quartz filters.

Figure 30 — Actual implementation of the IF9TX assembly. Visible at the top are the two cascaded 9 MHz, 2.4 kHz wide, Quartz crystal filters, which are similar to those, used in IF9RX. Another BIPA-like circuit (bottom left) is used as the CW drive control.

9 MHz Transmitter IF (IF9TX)

I will next discuss the design of the transmitter IF (IF9TX). Referring to Figure 2 from Part 1, the transmitter IF, IF9TX, performs all key transmitting functions as commanded by DFCB, using the BFO signals from the FRU — FSYNTH as buffered through PDAF. A microphone amplifier combined with a compression function and a VOX/ANTI-VOX function; condition the voice signals coming from the microphone. These signals are then input to a high level class II mixer, which in this case is made from individual components (unlike all other mixers in the system) in order to be able to control its balance. Carrier re-insertion and drive control are achieved in CW via the solid-state Hittite RF switches and another BIPA-like circuit used at 9 MHz in this application.

Transmitter gain control (TGC) is achieved automatically via a control loop fed from the TGC sensory assembly located at the back of the transceiver. This double RF sensor also provides RF power readings to the S-meter/RF Power meter via the T/R switching meter circuits located on the IF9RX assembly. There are two, eight pole — 9 MHz, 2.4 kHz wide — quartz SSB transmit filters cascaded in IF9TX, for a total of 16 poles of transmitted SSB selectivity. These filters are similar to the 2.4 KHz wide SSB filters used in the IF9RX assembly. The 16 poles were intended to keep the transmitted SSB signals within specific voice and intelligibility communications standards and not spread the information into adjacent channels. The resulting SSB signals sound crisp on the air with an audio response of 300 Hz to 2700 Hz. The schematic diagram of IF9TX is shown in Figure 29 and the actual implementation of the IF9TX assembly is shown in Figure 30.

Looking at Figure 29, the microphone audio input enters the conditioning circuits at J3. The signals are amplified by U1A and are further compressed and conditioned via U2, an Analog Devices SSM 2166 chip.[1] This professional grade audio conditioner gives outstanding performance and control over the speech waveforms with very low noise and total harmonic distortion (typically 0.25%). It offers variable compression (set at 2:1 in maximum mode) and automatic noise gating to improve the intelligibility of the microphone signals by recognizing and compensating for various signal level conditions. This circuit also uses a "downward expansion" technique (noise gate), which allows smoothing out speech transitions between words while canceling out background noise for improved signal-to-noise performance. For DX work, this "wonder chip" provides gain that is dynamically adjusted by a control loop to maintain a given set of compression characteristics. This allows using more compression when necessary, to increase average power. A high degree of flexibility was built into this chip by providing programmable VCA (voltage controlled amplifier) features, rotation point and noise gate adjustments.

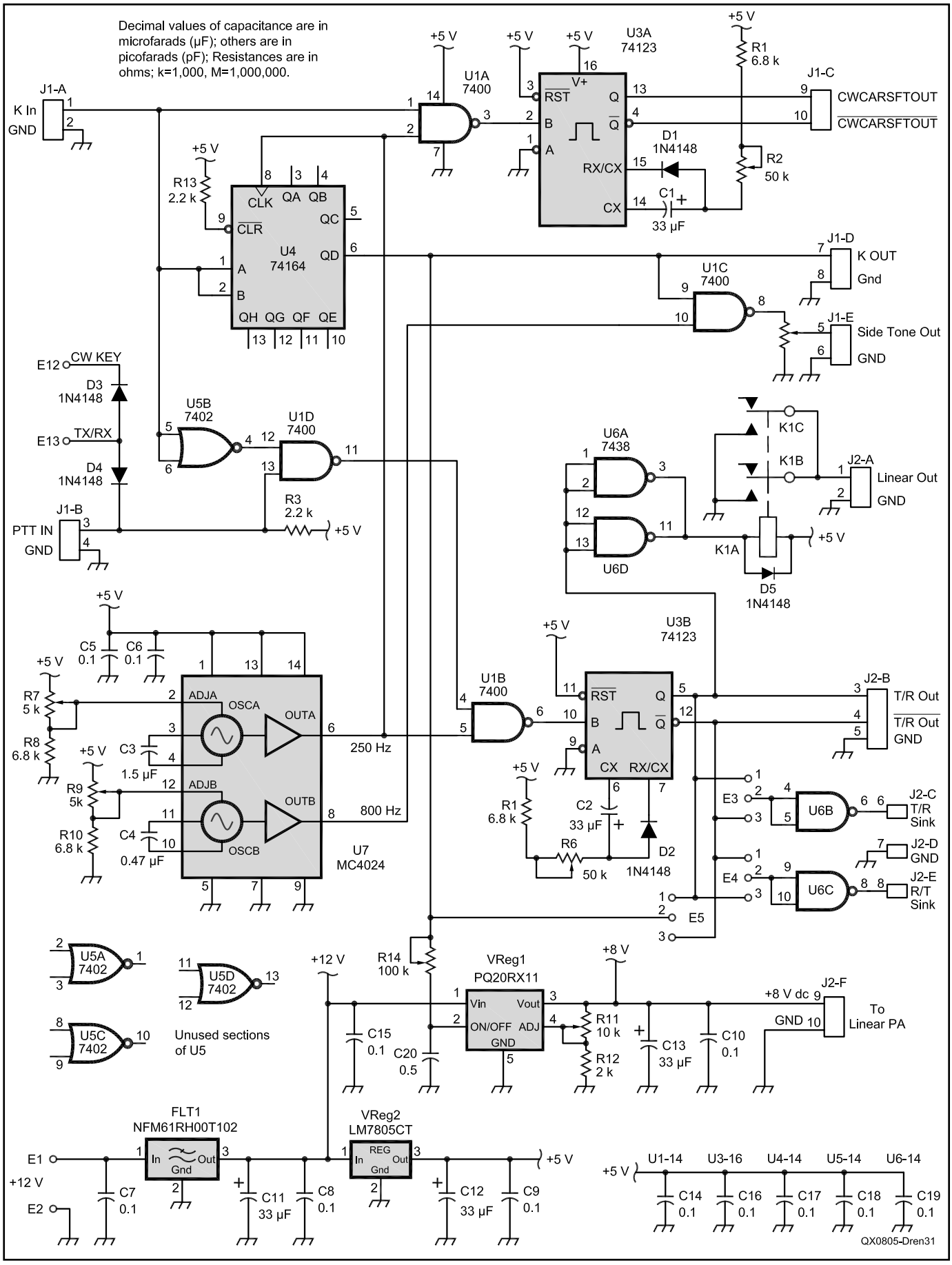
[1]Notes appear on page 49.

Looking at Figure 29, microphone gain is achieved from the front panel via J4-A. Compression level is also controlled from the front panel via J4-B. The actual controls are implemented via two concentric 10 kΩ potentiometers located on the left side on the front panel. The VOX/ANTI-VOX circuits are implemented via U5A and U3A andU3 B.

The conditioned microphone signal leaving the SSM 2166 variable compressor/noise gating device is input to a high level mixer via R30 and a low pass filter formed by L1, C20 and C21. The mixer is constructed of four matched HP 5082-2800 Schottky diodes.

Mixer balance is achieved via the combination of R56 and C64, which also serves as the BFO injection point for the various BFO frequencies (dependent on mode) selected from PDAF and coming from the FSYNTH via the PDAF assembly. It is at this point that the CW carrier is reinserted via the adjustable Quad PIN attenuator (Pi) ATN1 which is an exact replica of the BIPA circuit previously discussed in Part 2 of this series. CW drive

Figure 31 — Circuit diagram of the T/R control assembly. Various delays and commands are generated via one-shot logic circuits. A shift register (74164) is used to slightly delay the Morse code signals in order to allow the FRU — FSYNTH — to settle and lock-up between characters or character elements when switching between RX and TX and operating split. A dual clock (MC 4024) is used in conjunction with the shift register to generate the delayed Morse code characters as well as a keyed side tone signals.


Decimal values of capacitance are in microfarads (µF); others are in picofarads (pF); Resistances are in ohms; k=1,000, M=1,000,000.
J1-A
K In
GND
U1A
7400
U3A
74123
R1
6.8 k
J1-C
CWCARSFTOUT
CWCARSFTOUT
D1
1N4148
R2
50 k
C1
33 µF
R13
2.2 k
U4
74164
CLK
CLR
QA
QB
QC
QD
QH
QG
QF
QE
J1-D
K OUT
Gnd
U1C
7400
J1-E
Side Tone Out
GND
E12
CW KEY
D3
1N4148
E13
TX/RX
D4
1N4148
J1-B
PTT IN
GND
U5B
7402
U1D
7400
R3
2.2 k
U6A
7438
U6D
K1C
K1B
K1A
J2-A
Linear Out
GND
D5
1N4148
C5
0.1
C6
0.1
R7
5 k
R8
6.8 k
R9
5k
R10
6.8 k
C3
1.5 µF
C4
0.47 µF
ADJA
ADJB
OSCA
OSCB
OUTA
OUTB
250 Hz
800 Hz
U7
MC4024
U1B
7400
U3B
74123
J2-B
T/R Out
T/R Out
GND
R1
6.8 k
C2
33 µF
R6
50 k
D2
1N4148
E3
E4
E5
U6B
U6C
J2-C
T/R
Sink
J2-D
GND
J2-E
R/T
Sink
U5A
7402
U5C
7402
U5D
7402
Unused sections
of U5
+12 V
R14
100 k
VReg1
PQ20RX11
Vin
Vout
ON/OFF
ADJ
GND
+8 V
R11
10 k
R12
2 k
C13
33 µF
C10
0.1
C15
0.1
C20
0.5
+8 V dc
J2-F
To
Linear PA
FLT1
NFM61RH00T102
In
Out
Gnd
VReg2
LM7805CT
REG
C7
0.1
C11
33 µF
C8
0.1
C12
33 µF
C9
0.1
E1
E2
U1-14
U3-16
U4-14
U5-14
U6-14
C14
0.1
C16
0.1
C17
0.1
C18
0.1
C19
0.1
QX0805-Dren31

control is achieved from the front panel via J4-C as shown. Switching between SSB/AFSK and CW operation is achieved from the T/R assembly (and from PDAF) via J5-A and through the double RF solid-state switch arrangement at U7 and U8.

In either of the single sideband modes (upper or lower), the BFO is shifted accordingly and the 9 MHz SSB transmitter path coming from the mixer follows via T1, a TMO9-1 Mini-Circuits part and enters the first quartz filter XF1 (2.4 kHz) to go through the U7 solid state RF switch to be further amplified by U9 through the second quartz filter XF2 (2.4 kHz) and is finally output to IF9BC at J2. The transmitter gain control (TGC) (otherwise known as ALC) signals coming from the RF sensor assembly located on the transceiver's back (see leading picture) enter the IF9TX assembly at J5-E. The feedback signal is processed through Q1 (2N2222) and Q2 (a 3N200), which put the brakes on the IF/RF output coming out of XF2 at J2, always limiting the RF output of the transmitter to 100 W average.

When the transmitter is operating in the CW mode, the U7 and U8 solid state switches (Hittite HMC194) change the RF path from the SSB mode to insert the BFO signal directly into this path as controlled from the ATN1 CW drive and to be conducted through the U9 and XF2 path, through the TGC control circuits and to be output at the same J2.

Additional muting circuits are implemented via the T/R Switching Director assembly shown in Figure 2 of Part 1. DC power for the IF9TX is supplied as on any of the other *Star-10* assemblies, through on board tubular filters and regulators, as shown.

The IF9TX assembly is as unique as the IF9RX assembly. It accomplishes several transmit functions as commanded from the command and control assembly, DFCB assembly, the FSYNTH and the PDAF assemblies.

Transmit / Receive (T/R) Controller

The T/R control assembly in the *Star-10* is implemented using an all-digital approach. It operates in conjunction with the DFCB assembly, the IF9TX assembly, and the T/R Switching Director assembly. It accomplishes all T/R functions as shown in Figure 2 of Part 1.

The T/R assembly receives commands from the push-to-talk circuits, the VOX circuits and the CW key commands. Some of its functionality is also routed through the microprocessor in the command and control DFCB assembly. The T/R assembly outputs several control signals including the carrier shift commands in CW, the T/R control signals for closing the on-board high power linear amplifier switch-over relay circuit, the MUTE commands for IF9RX, PDAF and the Switching Director assemblies. In addition, it produces an 8 V dc bias control voltage to the power linear amplifier.

The T/R assembly is equipped with a dual square wave oscillator circuit (MC 4024), half of which provides keyed side tone audio signals to the audio mixer amplifier circuits in PDAF, the other half serves as a clock for a Morse code character shift register intended to delay slightly the code to the keying circuits on the IF9TX in order to allow the FRU — FSYNTH — to steer and lock-up between received and a transmitted frequencies when operating split and/or even between code characters when switching back and forth between the two split frequencies. The T/R control assembly is shown in Figure 31.

Looking at Figure 31, the PTT and/or Key functions are ORed together via the J1-A, E12, E13 and J1-B inputs. The signals are combined through the debouncing functions on DFCB as we previously discussed. A series of events are created upon key down or PTT, depending on the mode selected from DFCB.

In CW, the keyed signals are slightly delayed by a few milliseconds through the shift register at U4 (a 74164 shift register) and output through J1-D to be presented further to the IF9TX keying circuits. This delay is necessary to allow the synthesizer to settle down before shifting out the first CW character elements when working split between two different RX and TX frequencies. The delay is created in U4 as clocked by the 250 Hz oscillator A, at U7 (MC 4024). This short delay does not affect the operator perception of the transmitted CW keying. The 800 Hz side tone oscillator is implemented similarly at oscillator B of U7 (MC 4024). It is gated together with the delayed keyed Morse code and is output to the PDAF audio mixing circuits at J1-E.

Carrier shift commands are started through the logic circuit U3A, one half of a 74123 one shot. This one-shot circuit delays the release time of the shift commands briefly. The carrier shift command is output at J1-C. T/R commands are output through J2-A. These commands are intended for the external power linear amplifier switch over relay keying. Additional T/R control signals are output at J2-B and J2-C. The keyed regulated 8 V dc bias for the transceiver RF linear amplifier circuits is output via J2-F. This completes the T/R assembly description.

Power Linear Amplifier (PA)

The power linear amplifier for the *Star-10* is an adaptation of an off-the-shelf 100 W plus RF power brick available commercially. An initial amplifier was designed and developed following the Motorola application notes. This approach was abandoned later in favor of the current design because of parts availability. The power amplifier assembly is shown in Figure 32 A. The assembly has been mounted on a massive heath sink including the two fans visible in the back of the assembly as shown in Figure 32 B and C.

Looking at Figure 2 from Part 1, the transmitted signals are converted to the HF range by the H-mode mixer on IF75BC. The signals are further low pass filtered and amplified by the on-board class A amplifier (another CA2832 monolithic amplifier). This output is further presented to the power linear amplifier as shown.

The design of the RF power amplifier block is typical of 13.7 V power amplifier design. The first stage in this amplifier is operated in class A. Frequency response is compensated with feedback via a capacitor in parallel with the first transistor emitter resistor. Then the signal is amplified further by a low power push-pull amplifier. The output of this low power amplifier is coupled to the high power final push-pull amplifier stage. Additional feedback circuits are used throughout to keep gain relatively flat over the entire HF range. Cooling control is achieved by sensing temperature changes via an on-board thermistor, and using comparators, which activate the two fans when temperature exceeds 100°F. Higher fan speeds can also be achieved automatically. The output of the power linear amplifier is then passed to the half octave low-pass filter banks as previously discussed. From there, the RF signals go through the sensory electronics (see Figure 32C left), which in turn, feed the TGC circuits on IF9TX as previously discussed.

Other Assemblies (IF9NB)

Among the other assemblies in the *Star-10* are the Switching Director assembly, which provides additional muting circuits for the IF9BC, and the wide band IF amplifier and noise blanker assembly — IF9NB — as previously discussed in Part 1. This assembly provides wide spectrum analysis functions at 9 MHz, noise blanker detector functions to be fed to the BIPA circuit in IF9BC, and an oscilloscope function via a fixed conversion to 455 kHz.

Looking at Figure 2 from Part 1, the IF9NB assembly uses the 500 kHz wide IF signals from IF9BC. It amplifies them and triggers the one shot blanking circuits, which in turn blank the receiver through BIPA in IF9BC. The schematic diagram for IF9NB is shown in Figure 33.

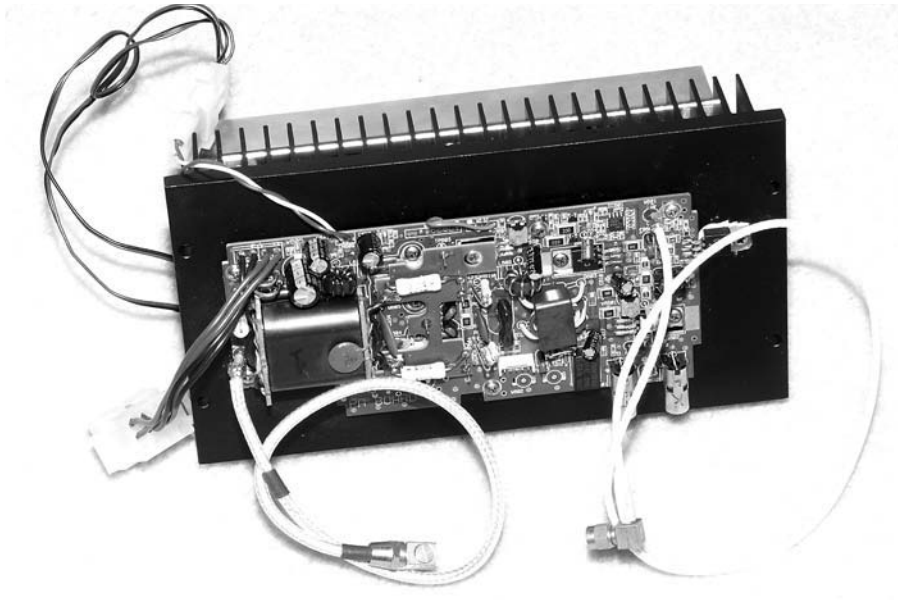
Looking at Figure 33, the 9 MHz wide IF signal (500 kHz) from IF9BC enters at J1. It is amplified and AGCed by the AD8367 amplifier at U1. From here, the wide signals are fed to the 2N2222 amplifier and the squaring circuits at Q1 and Q2. Another part of the signal is fed through a second path to a CP643 amplifier, Q3, to be output to an external spectrum analyzer with a 500 kHz bandwidth for viewing band activity at J2. To facilitate the spectrum analysis display function of the IF9NB, a modified SoftRock-40 SDR board was tested by KG6NK in a fixed 9 MHz receiver configuration, together with pertinent software and a PC equipped with a 16 bit audio card. This worked quite well over a displayed bandwidth of 20 kHz. The 16 bit card limited the dynamic range displayed. A 24 bit audio card would probably have given better results, but it was not tested.

The noise blanking function works as follows. The clipped signals (by CR1) from Q2 trigger one half of an adjustable pulse width one-shot, 74HCT123 at U2A. Pulsed blanking signals are output to BIPA via J5. Pulse width control is achieved from the front panel via the J5 connector as shown. A separate 9 MHz IF narrow signal coming from IF9RX is fed to the assembly via J3. It is converted to 455 kHz via a simple NE602 converter at U3. The on-chip local oscillator is a fixed quartz crystal, X1, oscillating at 8.545 MHz. The 455 kHz IF output is filtered via a 3 kHz wide Murata ceramic filter and is further amplified by a MAR-7 amplifier at U4. The oscilloscope signals are output at J4. This circuit is still being tested. This completes the IF9NB assembly description.

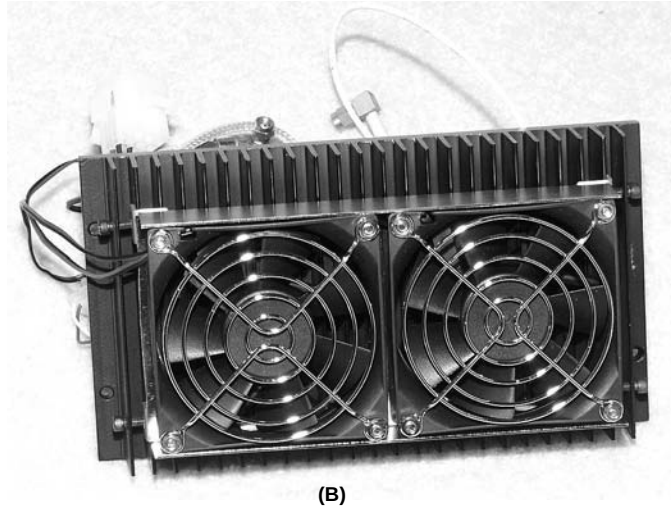
Switching Power Supply and Power-ON circuits

A special switching power supply (ATX-4) was built expressly for the *Star-10* by Phil Eide, KF6ZZ. The requirements called for a dual-output secondary (13.7 V dc and 24 V dc), triple EMI filtering, high speed over-voltage protection (that actually works), over-current protection, and a fast control loop to correct for anything the *Star-10* may demand. The design was derived from the ATX-1 design published in *QEX*.[2] ATX-4 is essentially the same as ATX-1. The demanding EMI control requirements, however, were imposed on the design, along with the most important design criteria, which was full protection of the expensive CA2832 amplifier blocks ($100 each) on the 24 V line.

Although beyond the scope of this article, the design of the ATX-4 has been very involved due to the radio frequency interference (RFI) requirement imposed on the power supply. Extreme EMI filtering has been used and the result has been outstanding. The ATX-4 has been used extensively



(A)



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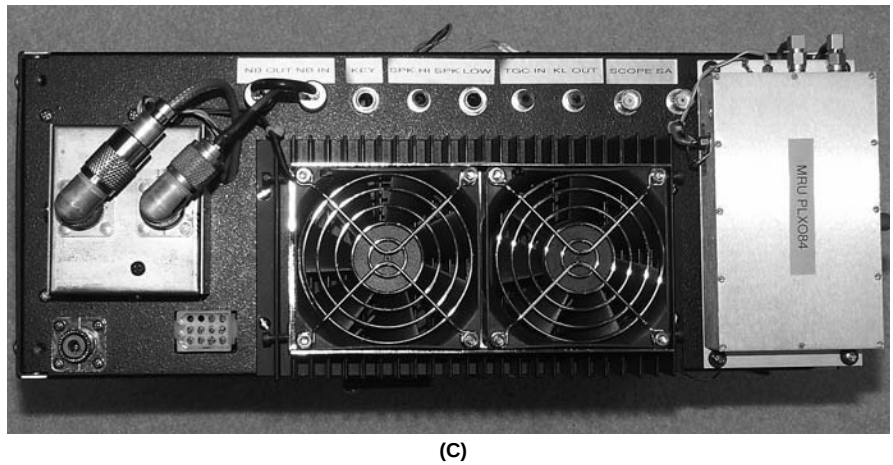


(C)

Figure 32 — Part A shows a photo of the RF power linear amplifier. B shows the cooling fans that are an integral part of the RF power linear amplifier assembly. They are mounted on the black anodized heat sink on the back of the assembly. The back of the *Star-10* transceiver is shown in Part C. The RF power linear amplifier and cooling fans are in the center. Sensory electronics are on the left and the master reference unit (MRU) is on the right.

with the *Star-10* and provides a totally clean RF environment on all bands of interest.

The ac power to the *Star-10* power supply is switched on and off from the front panel of the radio via a small power switch. This switch acts as a TTL level shifter to a solid state ac power relay (REDAC) located in a custom-made ac power strip in which the ac power cord of the power supply is inserted. The 5 V TTL voltage is derived from four AAA rechargeable batteries located under the bottom panel of the transceiver. The batteries are constantly being trickle charged by a small 6 V dc charger.

Four microprocessor cooling fans are used to cool the assemblies containing CA2832 amplifiers in the transceiver. These acoustically quiet fans use specially selected, dual-speed brushless motors that have been chosen on purpose because of their superior RFI performance. They are powered via a separate 12 V dc power supply in order to provide the greatest immunity to the receiver from RFI.

Putting it all Together

As previously mentioned, the *Star-10* final assembly has been the culmination of several years of RF design and development. It reflects modern state-of-the-art approaches to HF transceiver implementation. Its realization encompassed the many phases of engineering and development usually encountered in a complex commercial or military piece of equipment, from the system design through the circuit and software design, the multiple brass boarding, the complex testing and packaging into the final form factor as described in this series.

The *Star-10* packaging is complex and modular. All assemblies with the exception of the DFCB are enclosed in irridated machined aluminum RF enclosures available from COMPAC Corporation. These assemblies are mounted on two major shelves in the main enclosure as discussed in Part 2 of this series. These custom shielded assemblies are held together with multiple miniature flat screws, forming RF gaskets to provide better than 80 dB of isolation up to a GHz. The slots for interface connectors have been machined into the enclosures, thanks to Brendon Holt, KC5VCW. He donated his time and equip-

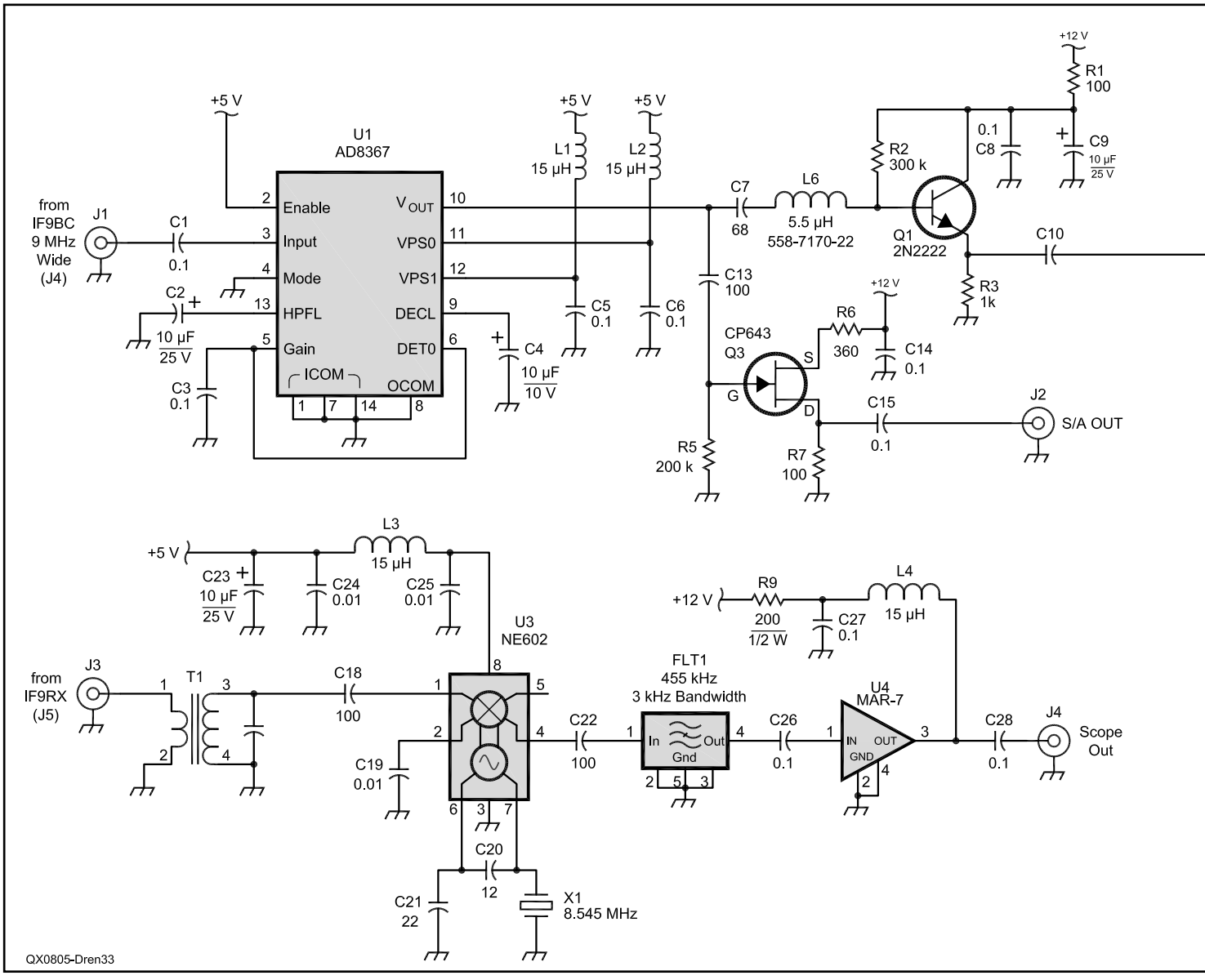


Figure 33 — Here is the schematic diagram of the IF9NB assembly. This assembly provides wide spectrum analysis functions at 9 MHz, noise blanker detector functions to be fed to the BIPA circuit in IF9BC, and an oscilloscope function through a fixed conversion to 455 kHz.

ment to the *Star-10* cause.

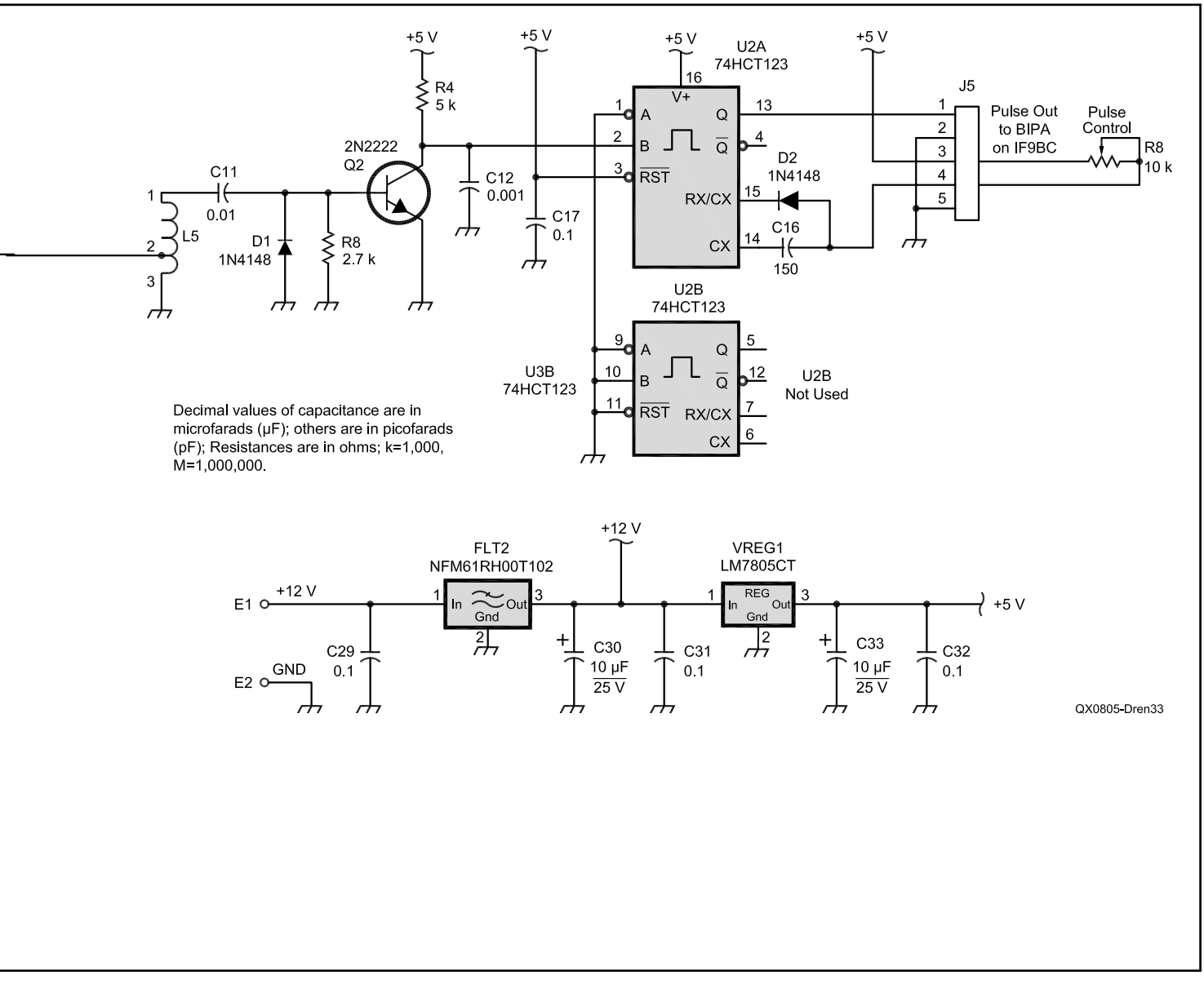
The *Star-10* circuit boards have been specially designed to install directly in the various sizes of machined aluminum boxes. They have been laid out expressly for the boxes and have been professionally executed on G-10 double sided circuit board material with plated through holes using multiple stitched ground planes, surface mount technology (SMT), along with hybrid assemblies.

The main enclosure was manufactured using aluminum panels that were professionally bent, sand blasted, irridated and painted with hammer baked black paint except in the areas where they meet, for RF shielding contacts. This enclosure was fabricated thanks to James Moon of M&R Sheet Metal & Mfg, Inc, in Tucson, Arizona.

The front panel is made of two large black anodized aluminum plates sandwiched together. They have been machined differently with respect to each other using cut-outs to hold the DFCB and keypad assemblies behind and hide them under panel holes, using flat screws and spacers. Thick film (0.8 mm Ortho Type III) membrane dials were manufactured from scratch using precision line artwork, photomechanical negative contact techniques and a large process camera. These dials have been sandwiched between the two anodized panels as shown in the transceiver main pictures. They are transparent in some areas to show through the displays, along with areas that have been selectively painted behind with silver paint to match the white silk-screened information painted on the black anodized front panel. Thus, a black and silver/white composite front panel resulted. I think this has a very "clean" look.

The *Star-10* assembly and testing came to full fruition during a three-week-long period in a well-equipped laboratory, courtesy of KG6NK, as shown in Figure 34. It should be noted that without the right testing tools, such a project could have not been completed. Although very intense, the final assembly went together without any major problems. There were no showstoppers.

Although the packaging was very tight, the radio performed as designed. As with any new design of this magnitude, slight changes had to be incorporated in some of the circuits and the inter-assembly interfaces during the



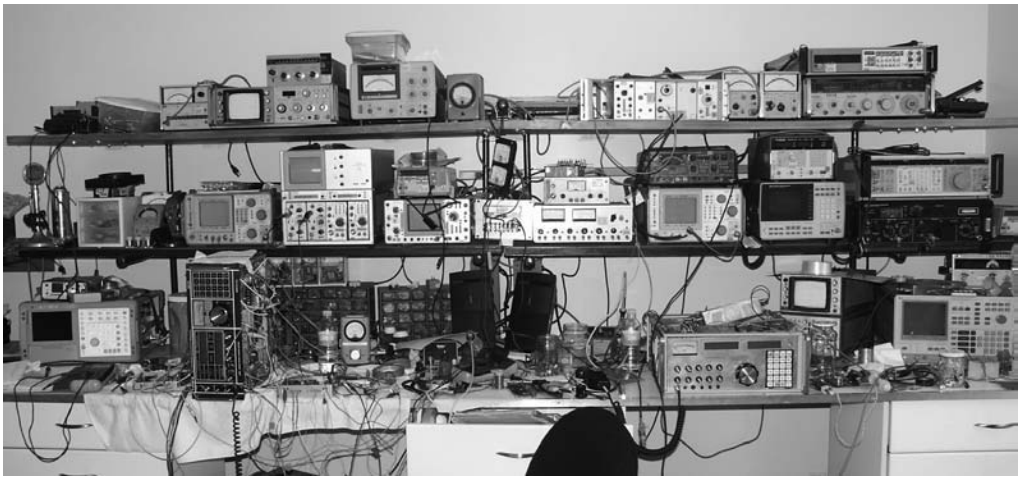


Figure 34 — The well-equipped KG6NK laboratory was used to complete the final wiring and testing of the *Star-10* transceiver. KG6NK's indisputable troubleshooting skills proved invaluable in the design, assembly, testing and especially in the final stages of the implementation.

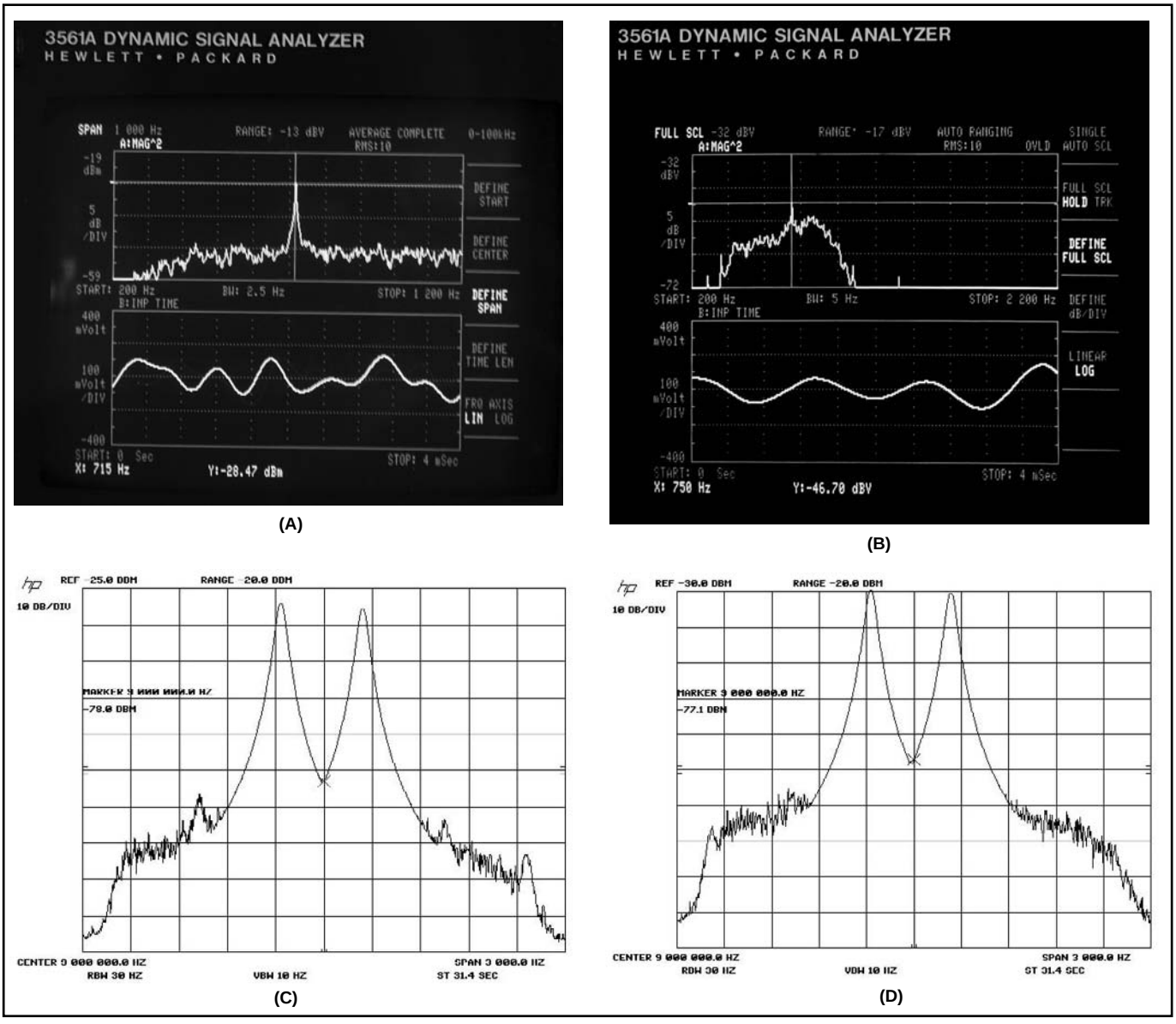


Figure 35 — Blocking dynamic range (BDR) at 5 kHz offset using 2.4 kHz ultimate bandwidth is shown in Part A. (Note: The values are expressed in dBm.) Part B shows the blocking dynamic range (BDR) at 5 kHz offset using 500 Hz ultimate bandwidth. (Note: The values are expressed in dBV.) The in band (2.4 kHz) receiver performance with two tones spaced at 500 Hz is shown in Part C. With the –15 dBm (S9+50 dB) signals applied at the receiver's input, in band spurs were 55 dB down. Part D shows the in band (2.4 kHz) receiver performance with two tones spaced at 500 Hz. With two RF signals 500 Hz from each other at –63 dBm (S9+10 dB) spurs were way down.

final assembly. These modifications have been introduced gradually until the system became stable. Most troubleshooting focused on finding and repairing pesky little contacts in silver or tin over gold connections in the signal connectors. Some of the coaxial cables have been found to be length sensitive and had to be cut to exact sizes. Several SMA type tubular, mil spec, RF attenuators have been occasionally inserted between RF assemblies. Comprehensive laboratory tests followed the final assembly.

A series of on the air tests followed. Reports from many DX stations proved that the transceiver's intelligibility in pile-ups is superior with the signal being picked up on the first or the second call despite the fierce competition. With the exception of some preliminary audio and compression level testing, crisp audio was always reported, proof of the microwave synthesizer's outstanding phase noise performance. The variable compression and noise gating features of the microphone circuits worked as designed. The receiver performance was equally good. The receiver's phenomenal IP3 spurious free dynamic range, and especially the blocking dynamic range allowed copying S1 or S2 SSB signals in the vicinity of 30 dB over S9 signals at only 3 kHz away from the desired signal. The receiver shines especially on CW during contests, when signals can be easily separated with precision at 500 Hz or less from each other by employing all 32 poles of cascaded IF filtering. Split operation was tested thoroughly as well as the RIT, pass band tuning (shift), memory, S-meter linearity, scanning and all other features.

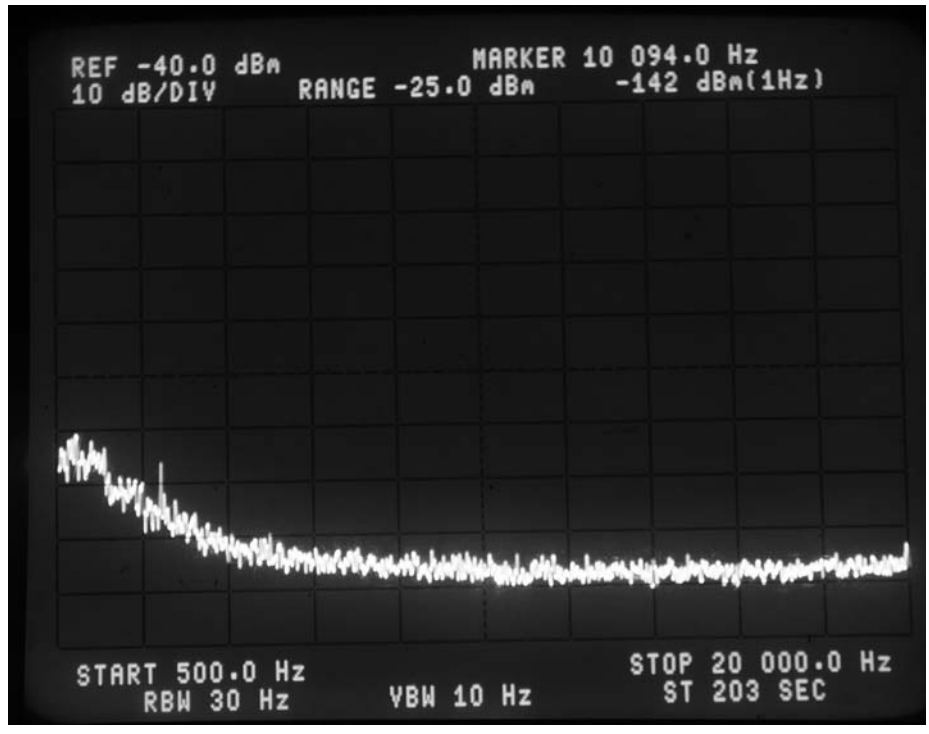


Figure 36 — The absolute phase noise measurement capability of the HP-3585A spectrum analyzer was calibrated using two HP-8640 generators in a classic mixing type phase noise measurement system. This capability was –142 dBc/Hz as shown.

Performance and Tests

Performance goals and specifications were presented in Part 1 of this article series. Comprehensive tests were performed in the laboratory. The MDS of the *Star-10* with the preamplifier ON was measured at –136 dBm in a 500 Hz ultimate bandwidth (with BIPA at zero dB). This was determined using a new calibrated Agilent E 6380A test set generator and an HP-400GL AC voltmeter and an HP-3561A . To verify accuracy of the Agilent 6380A, these numbers were also checked using a Fluke 6071A generator and a Tektronics 495P spectrum analyzer. The results were similar. This MDS is in line with predictions from Part 1 and is comparable with results obtained from a modified FT-1000D with the preamplifier ON. A test against the IC-7800 was also performed.

The 1 dB compression point of the FT-1000D with the preamplifier ON was found at –10 dBm. The 1 dB compression point of the *Star-10* receiver with the preamplifier ON and without the AIPA and or BIPA attenuators activated was found to be 0 dBm

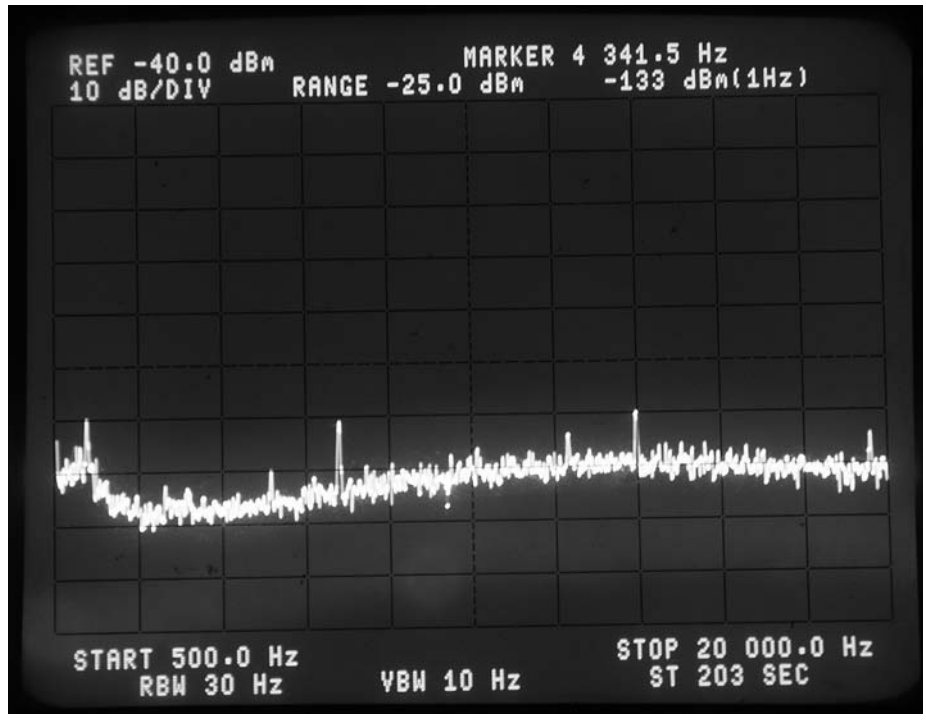


Figure 37 — Close-in phase noise performance of the FRU — FSYNTH — at 89.2 MHz (14.2 MHz) is –133 dBc/Hz. Phase noise performance has been tested and found to be uniform (within 1 dB) over the entire frequency coverage. The little spikes are spurs from the DDS, which are inside the loop filter, and cannot be eliminated. They are typically –100 dBc. These low spurs have not been audible in tests. See text.

(10 dB better). With AIPA and BIPA applied, the 1 dB compression point of the *Star-10* was found to be greater than +30 dBm. The receiver's composite linear dynamic range was found to be greater than 150 dB (500 Hz bandwidth, and all AGCs (AIPA + BIPA) turned on). This performance was listed in Part 1. The receiver's IP3SFDR was at least 130 dB using 20 kHz tone spacing (using a KW7CD test set with two combined quartz generators at 14.020 MHz and 14.040 MHz) and a 500 Hz bandwidth with the preamplifier on, and the AGC on. The *Star-10* receiver IIP3 was found at +45 dBm with the preamplifier on, just as predicted in Part 1.

The most demanding kind of dynamic range is, of course, the blocking dynamic range (BDR). *Star-10* receiver's blocking dynamic range (BDR) is due to an extremely crunch proof front-end design, the use of high-level mixers throughout, the superior microwave synthesizer used, and the superlative 32 poles of cascaded IF filters.

The *Star-10* blocking dynamic range was tested at 14.200 MHz using an HP-3561A dynamic signal analyzer as shown in Figure 35 A and B.

It was found that that with a –20 dBm interfering signal (the equivalent of an S9+ 53 dB signal) offset by only 5 kHz from the received frequency, the *Star-10* receiver can discern a –110 dBm signal (the equivalent of an S1 signal) with a 20 dB SNR when using the 500 Hz ultimate BW filter, with the preamplifier ON, no attenuators applied and no AGC action. The interfering signal level was then brought up to –8 dBm and even to 0 dBm before the –110 dBm desired signal at 5 kHz offset was finally blocked. This kind of interference is almost never encountered in real life, but the superior performance is very evident during contests and especially in the CW mode. The effect is very audible when tuning across a very busy band with signals bursting out of the MDS, and with little or no presence of nearby signals, a phenomenon not experienced with any other kind of transceiver I have ever tested. This radio is very quiet despite its sensitivity. As the band gets busier, the *Star-10* appears content, yet sensitive and very selective. In comparison with an IC-746 PRO or a 756-PRO that I tested against, there is no contest. These radios are just as sensitive (or even more so), but proportionally noisier than the *Star-10* when bands are busy (note: they bring the noise floor up due to IMD caused by a combination of factors including phase noise performance), while the *Star-10* pulls the signals out of the noise with ease.

Additional receiver tests were performed in the KG6NK laboratory using two in band RF signals 500 Hz from each other in the wide 2.4 kHz bandwidth. The measurements were observed at the second IF output. With two –15 dBm (S9+50 dB) signals applied at the receiver's input (in the 2.4 kHz BW) third order spurs were 55dB down. With two RF signals 500 Hz from each other at –63 dBm (S9+10 dB) spurs were way down. This is shown in Figure 35 C and D. This performance explains the superior experience observed with the *Star-10*, especially on CW during a busy contest.

The *Star-10* S-meter starts moving at an input signal level of –103 dBm (the equivalent of an S3). From this point on, the S-meter shows signals in linear dB (within 2 dB) up to an S9 + 40 dB (or –73 dBm + 40 dB = –33 dBm). Corrections for insertion loss of the various IF filters are automatically applied to the IF gain and S-meter upon filter selection, as discussed in the IF9RX section of Part 2. More AGC range could be used if applying the BIPA and AIPA controls. Automatic BIPA and AIPA control in the AGC loop(s) has not been implemented, leaving these controls in the manual mode. Using these controls has been minimal due to the outstanding dynamic range of the receiver.

The phase noise performance of the *Star-10* was measured directly at the synthesizer output using a phase-locked-loop measuring system involving a high level mixer, very linear amplifiers, filters and an HP-3585A spectrum analyzer which has the feature of reporting in dBm/Hz. The system was calibrated to display the noise directly in dBc/Hz. The offset from the carrier of interest was set from 500 Hz to 20 kHz. The instrument's capability was first verified by mixing two HP-8640 generator outputs locked to each other at 89.2 MHz (892 MHz initial FRU frequency divided by 10, or 14.2 MHz transceiver frequency). The resulting phase noise capability of the instrument is shown in Figure 36.

The FRU – FSYNTH — phase noise performance as implemented in the *Star-10* was found to be –133 dBc/Hz close-in, as shown in Figure 37. Better performance has been obtained by KG6NK in his version of the FSYNTH, as shown in Figure 38 A and C.

A –137 dBc/Hz (close-in) performance can be obtained from FSYNTH by tweaking the square wave DDS output level at the PLL phase detector input, separating ground planes between FSYNTH stages and by slightly changing the loop bandwidth. It should be noted that this performance is obtained because of the microwave frequencies used and only with a single VCO in the FSYNTH, instead of four as it is customarily done. Even better performance can be obtained with new microwave VCOs obtained from Synergy Microwave, the original manufacturer of *Star-10's* VCO. Experiments to improve on this performance are going on, with new VCOs

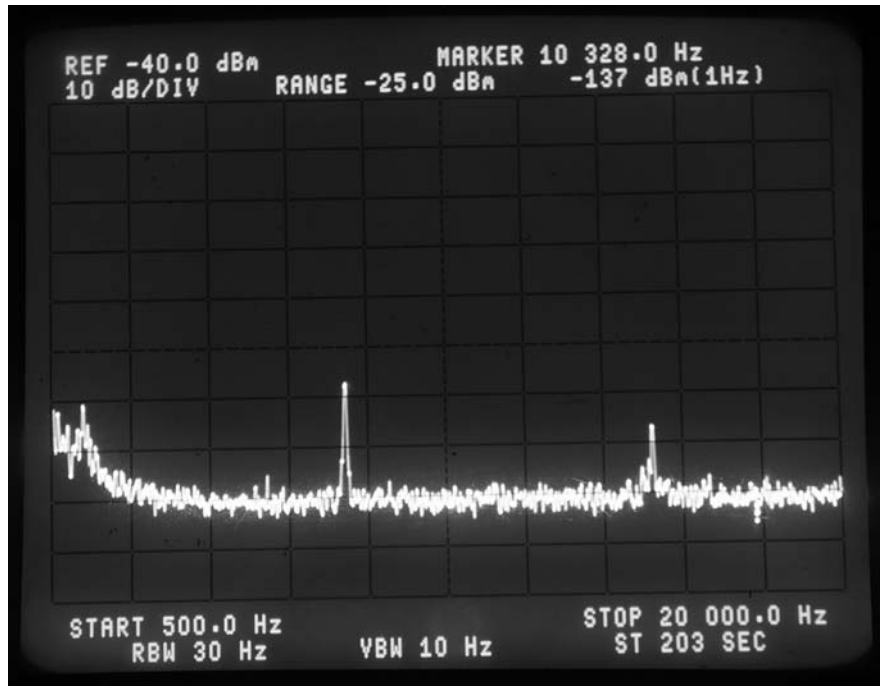


Figure 38A — KG6NK obtained –137 dBc/Hz close in phase noise performance from the FRU — FSYNTH — assembly by tweaking the circuits and widening the loop bandwidth. The previous in-band spur is –97 dBc. Listening tests proved that these spurs are not audible. Uniform performance (within 1 dB) has been obtained throughout the entire frequency range. The impact of the modifications on split operation lock-up and settling time have been analyzed and tested.

donated by Ulrich Rohde, N1UL.

The FSYNTH phase noise performance was further tested at several frequencies, 78.7 MHz (3.7 MHz), 82.1 MHz (7.1 MHz), 89.2 MHz (14.2 MHz), 96.2 MHz (21.2 MHz) and 103.4 MHz (28.4 MHz).

A final integrated phase noise plot of the FSYNTH from 10 Hz to 1 MHz offset was obtained using a PLL measuring system. The test was performed by KG6NK in his laboratory. A Bliley OCXO reference and its calibration plot against the Wentzel OCXO master was provided by John Miles, KE5FX. The FSYNTH frequency in this test was 100 MHz or 25 MHz receiver/transmitter frequency. See Figure 38B. A –138 dBc/Hz SSB phase noise was verified through this final test.

Transmitter two-tone intermodulation distortion tests were performed at 14.2 MHz with and without audio compression. The third order products were 32 dB down without compression and slightly worse with the audio compressor switched in. This is shown in Figure 38, Parts D and E. The harmonic rejection performance has been documented in detail in references 1, 2 and 3 from Part 2 of the article.

Transmitter SSB audio response measurements were performed in the upper and lower sidebands with full power (100 W) output by using an Amber 3501 audio distortion measuring system, a Bird-43 RF wattmeter and a dummy load. Although the theoretical transmitted audio frequency response was calculated to be from 300 Hz to 2700 Hz, the actual audio response under full transmit-

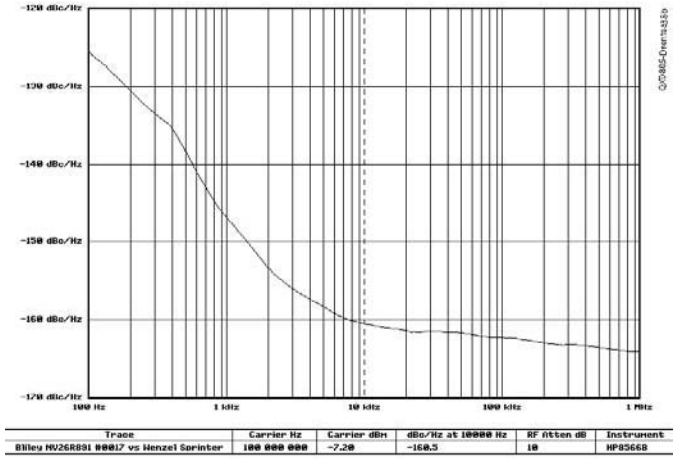


Figure 38 B — This plot shows the phase noise performance of the 100 MHz Bliley OCXO reference source used in these tests. It was calibrated against a very high quality Wentzel frequency standard. The plot shows the integrated single sideband phase noise plot from 100 Hz to 1 MHz. This calibration and plot are courtesy of John Miles, KE5FX.

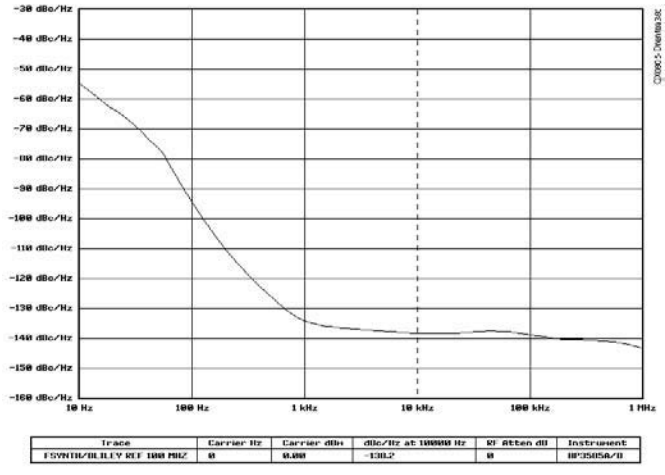


Figure 38 C — This plot shows the Integrated single sideband phase noise plot of an improved *Star-10* FSYNTH assembly from 10 Hz to 1 MHz. The performance is better than –138 dBc/Hz at 10 kHz offset. The test was performed by KG6NK in his laboratory and was obtained using a professional PLL measuring system, a Bliley OCXO reference source calibrated against a Wentzel frequency standard, and the HP-3585A spectrum analyzer. "Tool Kit PN " software was provided by John Miles, KE5FX and was implemented together with a Prologix interface, which was used to control the instrument, integrate the results, and display them. The FSYNTH frequency in this test was 100 MHz or 25 MHz receiver/transmitter frequency.

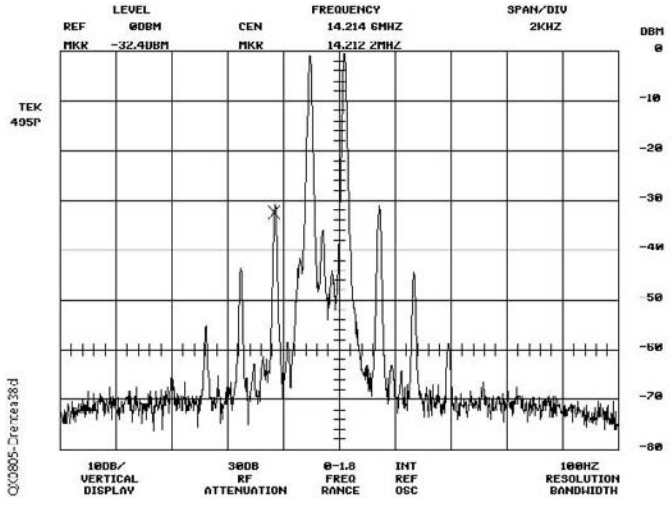


Figure 38 D — Here are the two tone transmitter test results, without compression. Third order products are 32 dB down. The tests show a clean noise floor, which is due to the FSYNTH performance.

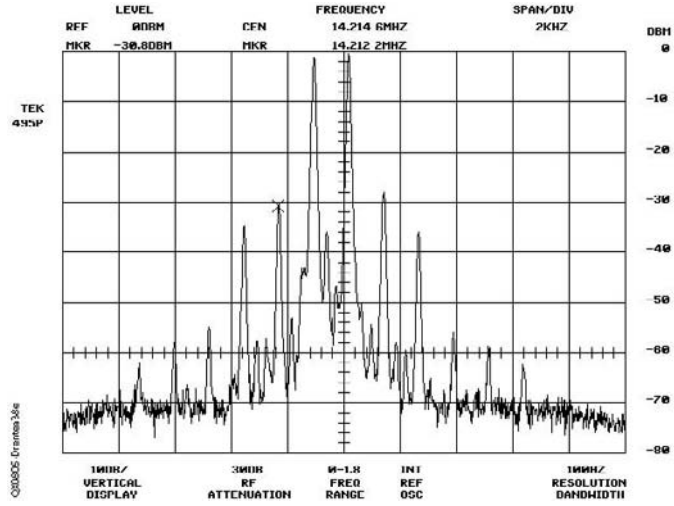


Figure 38 E — The two tone transmitter test with 2:1 audio compression turned ON is shown here.

ter output was found to be from 270 Hz to 2800 Hz at the 6 dB points. The output falls greatly before and after these points due to the 16 poles of transmit IF filtering. No splatter was ever reported from the *Star-10* during on-the-air tests. Harmonic rejection and image rejection tests have been previously performed as a function of the front-end half-octave filter banks and have not been repeated this time.

Lessons Learned

As with any new piece of equipment of this magnitude, a certain number of problems are usually expected. Because of the intense breadboarding and design verification before its final implementation, these problems have been kept to a minimum in the final version. In retrospect, most problems in the execution of *Star-10* have been mainly cold contacts in the interface control wires, connectors and relays. Some of the old relay contacts corroded and caused heating of the low pass filter banks in transmit. This situation was immediately corrected. Because of the tight *Star-10* package, access to some of these connectors has sometimes been difficult. Some problems also occurred in the SMT circuits.

After getting rid of most bugs, *Star-10* has performed reliably. Especially trouble free has been the DFCB command and control assembly and its associated software, which performed as designed after intense and careful analysis of the mathematics governing the system and operator interface. Numerous software upgrades were implemented and tested before the current trouble-free version. This combined with careful breadboarding, troubleshooting and testing the DFCB in the early phases made for an almost perfect software design. Also, the IF9TX, IF9RX and IF75BC and power linear amplifier have operated flawlessly from the start. Other assemblies required some tweaking, but have proved equally reliable after the initial hurdle.

One of the most important lessons learned from this design is that no matter how careful one is in selecting components, by the time the design is implemented, they become obsolete. Of course there is always a better way of doing things, in retrospect. This is not a new thing, however. Engineers everywhere face this kind of problem in an ever-changing industry.

A second lesson learned which goes hand in hand with the first one is to know when to stop designing circuits and not run the risk of breadboarding forever. This was hard. It required discipline and a firm gut feel about when to freeze the design.

Another good lesson learned is that no matter how careful one is in a design, things suspected to work well, don't, and things suspected to have problems might sometimes work just perfectly. This is also known as Murphy's Law.

An interesting conclusion after performing complex testing and operating the *Star-10* in rough contests is that, contrary to popular belief, roofing filters are not as important in improving dynamic range as once thought, if good front end performance is provided in the first place. As explained in Part 2, roofing filters with a 3 dB bandwidth of 10 kHz or less, that withstand the high signal levels required for ultra high dynamic range needed at this point in a system, are extremely demanding to manufacture from an IMD point of view. If the front end has the kind of performance realized in the *Star-10*, the roofing filters can be more forgiving. That is not to preclude that narrow roofing filters can greatly help overall performance of radios with lesser front-end dynamic range performance.

A final lesson learned is that no matter how good the design is; better AGCs and better noise blankers are always needed. *Star-10* makes no exception to this rule.

In operating the radio, a 500 Ω dynamic microphone with a flat response has been used. Some compression has been found useful, but not necessary, as the audio response is very crisp and distinct. Initial tests driving a full legal power linear amplifier revealed some RF feedback getting into the microphone circuits because my 20-meter beam is located right above the radio room. As any notorious RF feedback problem goes, this problem wasn't cured just with little ferrite beads and bypass capacitors as is usually found in transceiver microphone circuits. An investigation of the literature revealed not much information on RFI microphone filters.

A third order Butterworth audio low-pass filter with a 2.7 kHz cut-off frequency was designed and implemented at the transceiver microphone input, and the problem went away for good. This design was done using the AADE Filter software and is shown in Figure 39.

The *Star-10* transceiver has been in reliable operation, 24 hours a day, seven days a week for more than a year. Although three other transceivers are available here, using

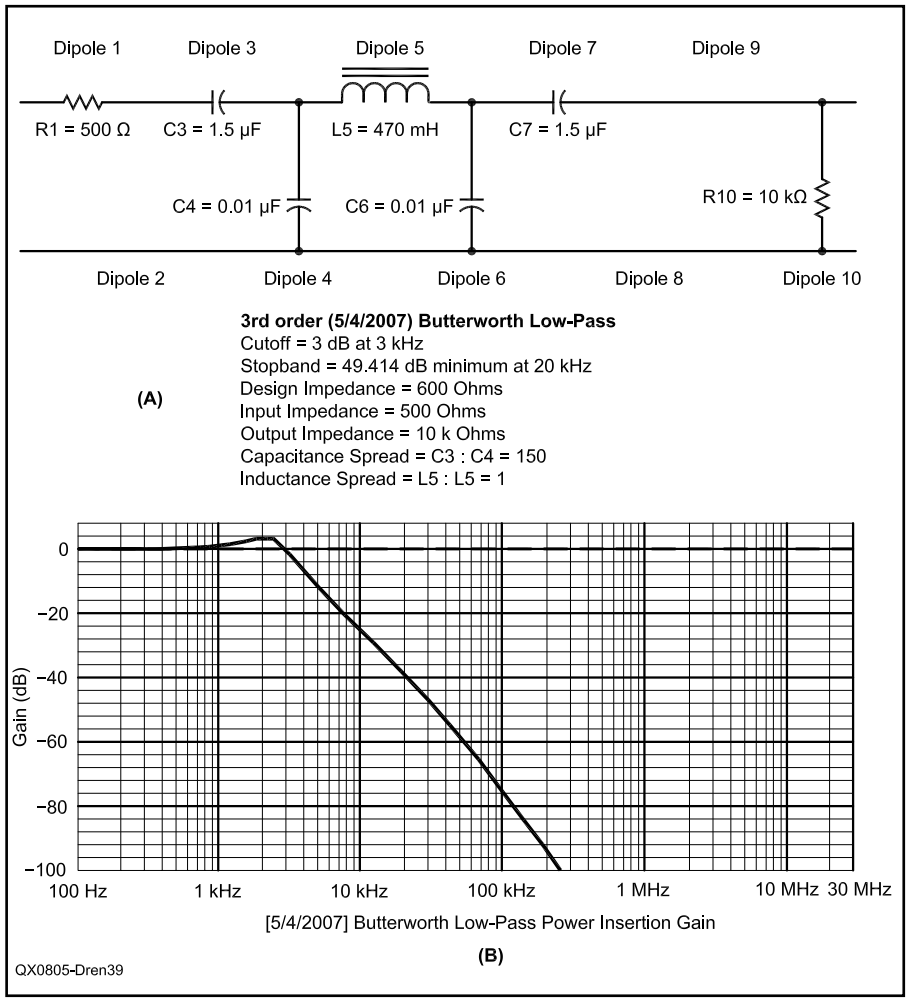


Figure 39 — Design of the third order Butterworth low-pass microphone input filter eliminates RF feedback caused by a nearby beam above the radio room when running high power.

this radio has been the preferred choice, especially when listening to busy bands. Operating this radio has been a joy due to its superior performance and its friendly user interface. *Star-10* stands ready for the upcoming, wildly predicted solar cycle.

Conclusion

The *Star-10* project has been a long and stressful engineering exercise. For the many who wrote in with their positive comments and compliments on the first two parts of the series, thank you.

This article was intended to share information. The *Star-10* transceiver was designed to prove that superior equipment can still be built and high performance combined with professional features can be designed and implemented to compete with any sophisticated transceiver on the market today. Despite this, the *Star-10* is not perfect. Even better transceivers can be built using this experience. I hope this series of articles has been an inspiration to equipment builders everywhere, to RF system designers and engineers, as well as to the armchair radio designers.

As I mentioned at the beginning of this article series, it has always been the dream of the technically inclined radio amateur to build and operate his or her own radio equipment from scratch. With a few exceptions of dedicated home brewers, it appears that operating your own home brewed radio on the bands today is a rarity. In using the *Star-10* on the air and mentioning that it is home brewed elicited some interesting reactions. Much to my surprise, comments like "Is it a kit?" or "Do they still do that?" have been commonplace.

I find this situation sad. Amateur radio used to be at the forefront of technology. Hams were the future engineers and scientists. They were persistent experimenters and innovators that achieved noteworthy technical success. It is my opinion that this trend must continue if ham radio is to remain the technical hobby it deserves to be.

It is a very proud feeling to operate equipment that you have designed and developed regardless of how simple or sophisticated it is.

Cornell Drentea, KW7CD took his first radio receiver apart (and put it back together) at the early age of six. He has been a Ham since 1957. Since then, he's built many radios and transceivers and made his passion for designing "radios" his life long profession. As an Amateur Radio operator, he is known for his extensive RF technology articles in magazines such as Ham Radio, Communications Quarterly, RF Design, *and* QEX. *Professionally, Cornell is an accomplished RF technologist, an engineer and a scientist with over 40 years of hands-on experience in the aerospace, telecommunications and electronics industry. He has been involved in the design and development of complex RF, Radar, guidance and communications systems at frequencies of up to 100 GHz. Cornell has developed several state-of-the-art RF products including ultra wide band high probability of intercept microwave receivers, complex synthesizers, multi-modulation transmitters, Doppler agile space transceivers as well as high power RF linear amplifiers. He received his formal education abroad with continuing studies and experience achieved in the United States. Cornell has presented extensively on RF design topics at technical forums such as IEEE, RF-Expo, Sensors-Expo and has given comprehensive professional postgraduate courses in RF receiver design, synthesizer design, sensors and communications. He has published over 80 professional technical papers and articles in national and international magazines. He is the author of the book,* Radio Communications Receivers, *McGraw Hill, ISBN 0-8306-2393-0 and ISBN 0-8306-1393-5, 1982 and holds five patents. He is currently available for consulting to large and small RF enterprises. You can find out more about Cornell, his consulting and his RF course offering entitled* The Art of RF System Design *on his web site:* **members.aol.com/cdrentea/myhomepage/**

Notes

[1]Analog Devices, *Microphone Preamplifier with Variable Compression and Noise Gating — SSM2166*, Application Note.

[2]Phil Eide, KF6ZZ, "ATX Adventures," *QEX,* Nov/Dec, 2004, ARRL, pp 36-46.

Additional Reading

Rohde & Schwarz, *Challenges in Testing Software Defined Radios*, **sdrforum.org/pages/sandiego_07_workshop/SDR%20Test%20Presentation%20v6.ppt**

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Eric Hakanson, Anritsu Company, "Understanding SDRs and their RF Test Requirements," RF Design Line; **www.rfdesignline.com/showArticle.jhtml?printableArticle=true&articleId=196601944**

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M. W. Shores, "Chart Pinpoints Interference Problems," *EDN*, Jan 15, 1969, pp 43-46.

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QEX

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Antenna Options

Reflections on Reflectors

Some reflectors reflect — and others do not. Consider the two different beams in Figure 1. One uses a planar reflector, while the other uses a parasitic reflector. The planar reflector actually reflects. In important ways, the parasitic reflector does not — at least not in the way we usually imagine the situation with parasitic beams.

The most common mental picture that we generate when first encountering the conventional names of Yagi elements is something like a lighthouse beacon. Each light has a reflector to determine the beam direction and a lens to direct and focus the light from the structure. So we link the lighthouse's Fresnel lens to the parasitic director or directors of a beam and we associate the beam's reflector with the lighthouse's reflector. Indeed, some lighthouses do not use reflectors, and so too we can actually construct parasitic beams without a reflector element. The mental picture is simple, straightforward, coincident with the beam element names — and mostly wrong.

Some beam types do reflect energy in the conventional lighthouse or flashlight sense. These beams differ in some important respects from parasitic beams, of which the Yagi-Uda array is the most common form. Since I have received numerous questions about the differences between — and the potential interchangeability of — the two types of reflectors, it seems useful to look briefly at these two options for creating directional antennas.

Reflectors that Reflect

Let's begin with reflectors that reflect: the planar (or curtain or sheet) reflector, the corner reflector and the parabola. Each type has special needs and many variations and we shall confine our discussion to the planar reflector as perhaps the simplest form of reflector screen. Planar reflectors are very old and often went under the name "billboard" reflectors in the 1920s. Figure 2 shows the basic principles of the planar reflector's operation, largely derived from optical principles applied to RF energy.

The basic unit for understanding the sketch is the *ray*. If we think of a dipole element (shown on end in the sketch) as emitting rays in all directions, we can trace the patterns that emerge. Some rays are completely reflected forward, where they add to or subtract from the rays from the dipole itself in standard interference patterns. Some rays to the side have no reflected rays for such combinations and hence form partially shadowed areas. Behind the reflector sheet is an area where almost no rays go, creating a full shadow. At the reflector edges, however, we encounter diffraction, with some energy scattered in virtually all directions. Hence, a planar reflector with

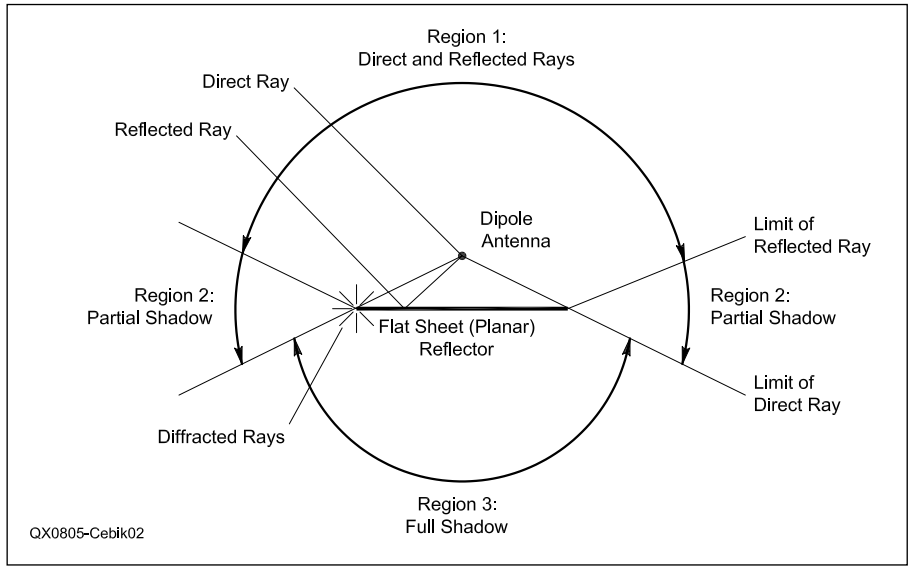

Figure 2 — Limitations of a planar reflector having a finite H-plane dimension. (Adapted from Kraus, *Antennas*, 2nd Ed, p 548.)

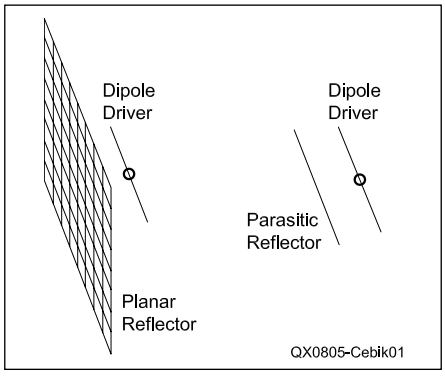

Figure 1 — The options for a dipole driven element, with a planar reflector or a parasitic reflector.

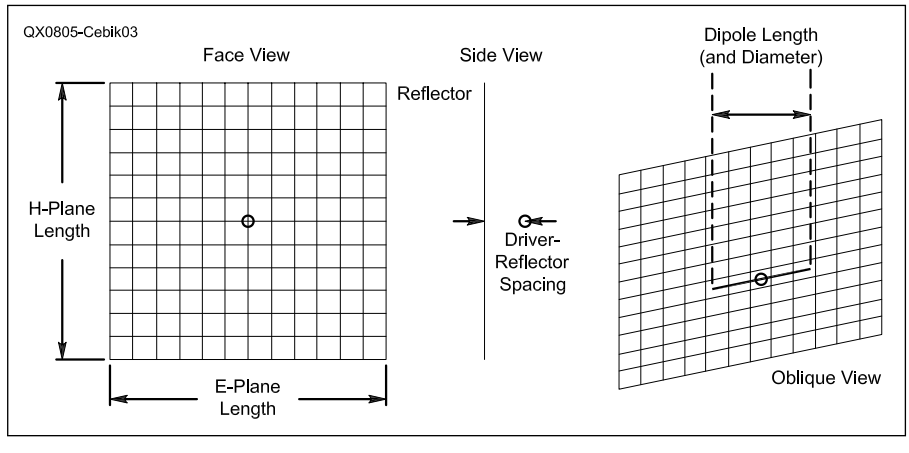

Figure 3 — The critical dimensions for a planar reflector with a dipole driver.

finite dimensions cannot create an infinite front-to-back ratio.

Ahead of them, we can place arrays of phase-fed driver elements, both simple and complex. For example, a common UHF beam uses a planar reflector with a double-diamond element. For clarity, however, we shall use a simple dipole as the driver. As shown in Figure 3, we place the dipole ahead of the reflector plane and the forward radiation consists of the direct rays from the dipole and the reflected rays from the sheet. The reflector size and the placement of the dipole are not arbitrary. Figure 3 shows most of the critical dimensions for making such a beam.

Let's begin by assuming that we wish to set the dipole's feed point impedance at 50 Ω. We shall remove this limiting assumption later. It will serve us to illustrate one or two points about planar reflectors, however. First, as shown in the top portion of Table 1, the size of the reflector does make a difference in planar-beam performance. If our main concern is the front-to-back ratio, then the size of the screen may grow indefinitely, especially off the ends of the dipole, to increase the ratio. If our concern is gain, then there is an optimal reflector size for maximum gain.

As a rule of thumb, the reflector should extend from 0.4 λ to 0.6 λ beyond the limits of the driving element or array. The larger the driver assembly that we use, the larger the screen must be to achieve maximum gain from the total assembly. As a side note, in the range of reflector sizes shown, using a constant dipole length and spacing from the reflector, the feed point impedance does not change significantly as we change the size of the planar reflector.

For the simple dipole driver, the 1.2-λ by 1.2-λ reflector provides maximum gain. A double-diamond or a bobtail curtain drive might provide up to 2 dB additional gain. As well, curtain arrays exist that place vertical and horizontal bays of drivers before very large screens for additional gain. We may increase the front-to-back ratio by increasing the E-plane dimension, the dimension of the reflector parallel to the driving element. If the screen is about 2 λ in this direction, the 180° front-to-back ratio will approach 30 dB. The worst-case front-to-back ratio will tend to remain relatively constant in the 22 to 24 dB range, however, despite high 180° values. Only the rear lobe in line with the axis of the beam undergoes radical reduction.

A second factor is the spacing of the dipole from the reflector plane. As shown by the modeled data in Table 1, we can achieve higher gain values and higher front-to-back ratios by moving the dipole closer to the screen. The closer spacing results in more complete illumination of the reflector by the dipole source. As the dipole approaches the reflector, its resonant length slowly changes. As well, the resonant impedance decreases. Whether the performance improvements are worth the inconvenience of requiring more complex matching methods for the amateur's standard 50 Ω cable is a user decision. Different driver assemblies have different optimal spacing values for a direct 50 Ω match to the feed line, and as driver assemblies grow more complex, the best match spacing may not be close to the best performance spacing.

When deciding between a planar reflector array and a parasitic beam, we must measure our communications needs against the likely performance of the potential antennas. Table 2 lists some of the key modeled performance characteristics in free space for the medium-size reflector with a dipole driver and of two types of Yagis: a 2-element driver-reflector array with the element spacing close to the value that yields the best front-to-back ratio and a 3-element relatively long-boom (0.345 λ) Yagi. The 2-element Yagi often serves as a seeming analog to the planar reflector array, but its performance does not approach either the gain or the front-to-back ratio of the true reflector antenna. The 3-element Yagi in the list beats the planar reflector in the front-to-back category but not in gain. Of course, we can always add an almost indefinitely large number of directors to the Yagi to improve its gain and to narrow its beamwidth in both the E-plane and the H-plane. See Figure 4 for free-space patterns in both planes for all three antennas.[1]

The ultimate decision on whether to use a Yagi or a planar reflector does not normally rest on small differentials in gain and

Table 1
Planar reflector-and-dipole performance as functions of reflector size and element spacing at 435 MHz with 4 mm diameter dipole.

Reflector size: constant 0.175 λ dipole spacing, constant dipole length of 0.442 λ.

Gain dBi	*F-B Ratio dB*	*Feed-Point Z R +/- j X Ω*	*SWR 50 420 MHz*	*SWR 50 450 MHz*
Small (0.8-λ by 0.8-λ)				
8.37	16.00	49.7 + *j* 2.0	1.76	1.71
Medium (1.2-λ by 1.2-λ)				
9.31	18.34	50.1 – *j* 0.3	1.80	1.65
Large (1.6-λ by 1.6-λ)				
8.64	22.96	49.5 + *j*0.2	1.81	1.67

Dipole-to-reflector spacing: reflector constant 1.2-λ by 1.2-λ.

Spacing λ	*Gain dBi*	*F-B Ratio dB*	*Feed-Point Z R ± j X Ω*	*Dipole Length λ*
0.185	9.25	18.17	54.3 – *j* 0.5	0.442
0.175	9.31	18.34	50.1 – *j* 0.3	0.442
0.165	9.37	18.51	45.8 – *j* 0.5	0.442
0.155	9.42	18.67	41.8 + *j* 0.2	0.4428
0.145	9.46	18.81	37.5 + *j* 0.1	0.4434
0.135	9.50	18.94	33.3 – *j* 0.6	0.444

Table 2
435-MHz performance of a planar reflector-and-dipole and of 2- and 3-element Yagis.

Gain dBi	*F-B Ratio dB*	*Feed-Point Z R ± j X Ω*	*2:1 SWR Limits F(low) MHz*	*F(high) MHz*
Medium reflector with a 4 mm dipole spaced 0.175 λ away.				
9.31	18.34	50.1 – *j* 0.3	<420	>450
2-element driver-reflector Yagi with 0.125 λ element spacing and 4 mm-diameter elements.				
6.27	11.26	32.8 + *j* 0.4	425	448
3-element Yagi with 0.348 λ boom and 4 mm-diameter elements.				
8.27	24.65	25.3 – *j* 0.4	428	443
Rod planar-reflector simulator (1.2 λ by 1.2 λ via 13 0.036 λ diameter rods spaced 0.1 λ).				
9.28	18.48	49.2 – *j* 1.0	<420	>450

Note: medium and rod planar reflectors use a 4 mm diameter dipole spaced 0.175 λ.

[1]Models for the antennas discussed in these notes are available in *EZNEC* format at the ARRL Web site. Go to **www.arrl.org/qexfiles** and look for **05x08_AO.zip**.

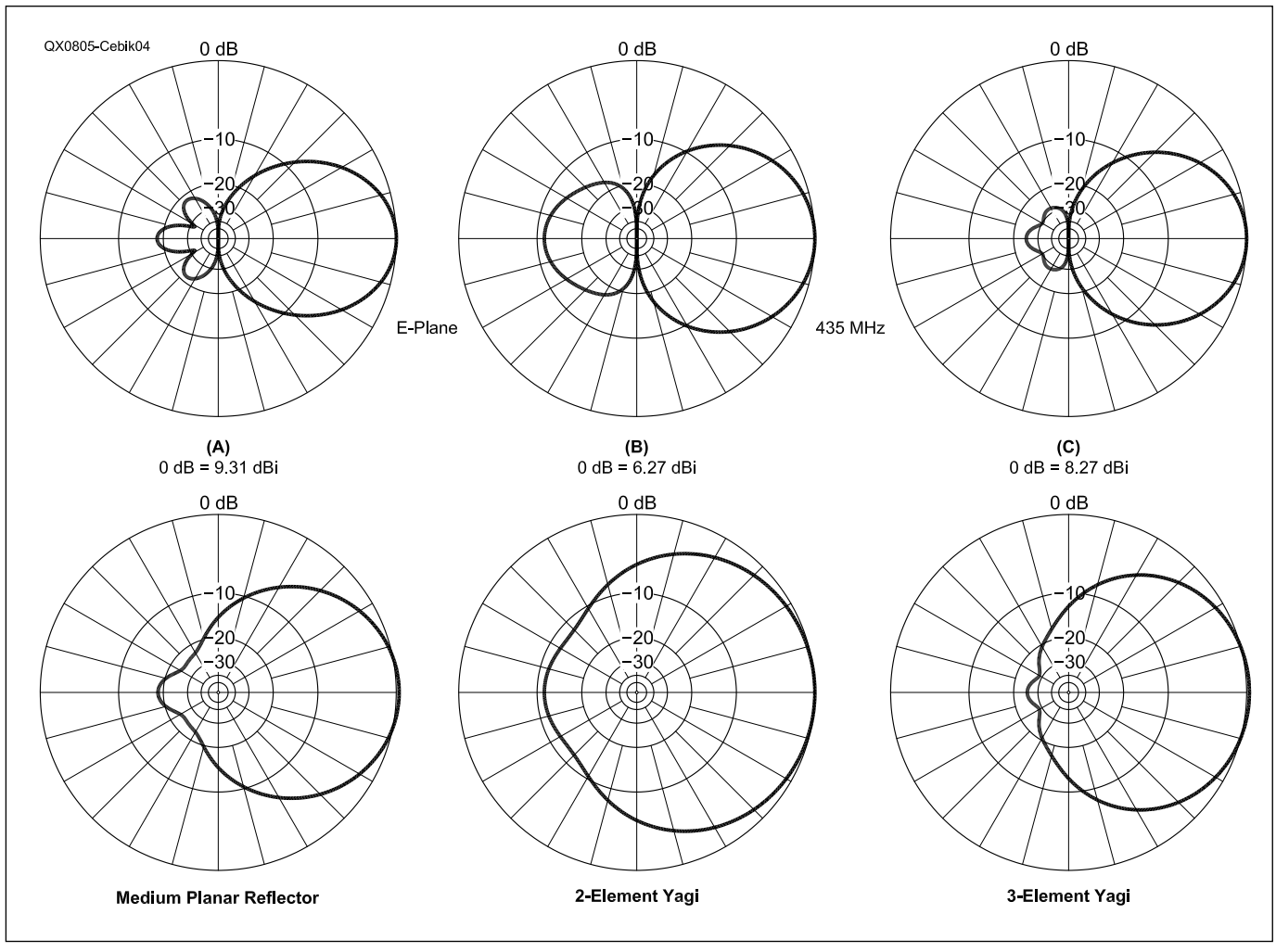

Figure 4 — Comparative E-plane and H-plane free-space patterns for: (A) a planar reflector with a dipole driver, (B) a 2-element Yagi and (C) a 3-element Yagi.

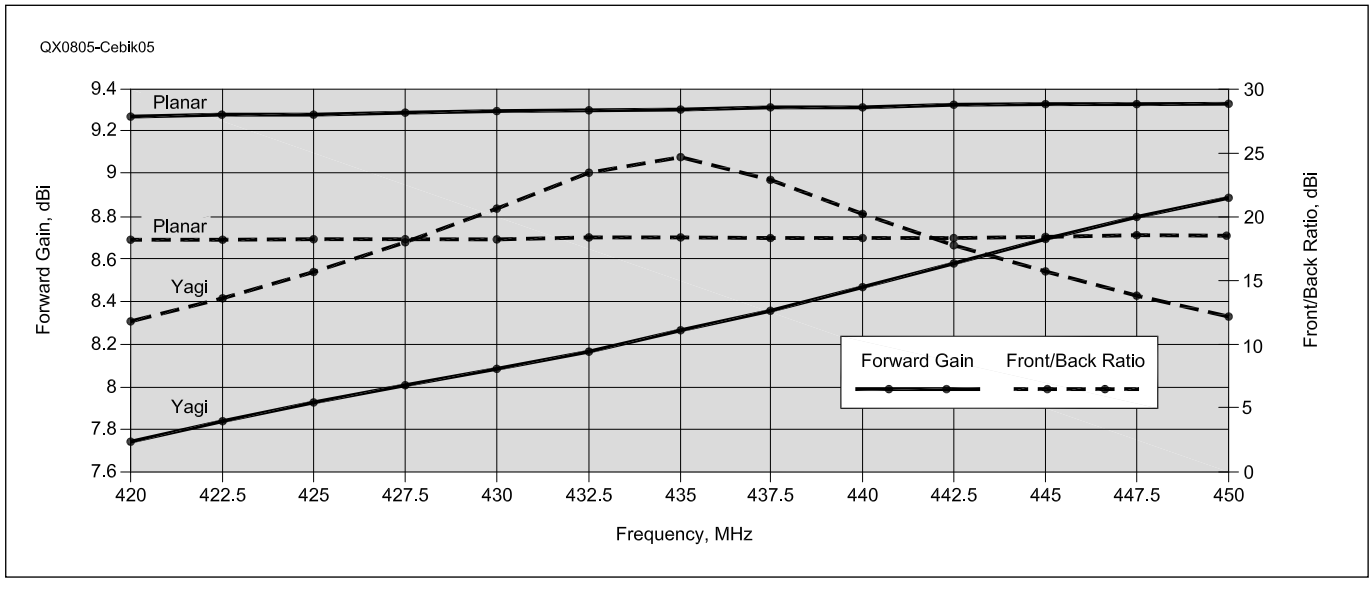

Figure 5 — Free-space forward gain and 180° front-to-back ratios for a planar reflector with a dipole driver (solid line) and for a 3-element Yagi (dashed line).

the front-to-back ratio. The Yagi, exemplified by the 3-element version in these notes, has by nature a fairly narrow operating bandwidth in which the performance values remain stable. We sometimes talk of broadband vs narrowband Yagis, but such discussions are relative to Yagis alone. Compared to the planar reflector array, all Yagis are narrowband antennas.

Figure 5 provides data on the modeled gain and front-to-back performance of the 3-element Yagi and the simple planar reflector array. The planar array values are very nearly flat from 420 to 450 MHz. The degree of increasing gain is comparable to the increase that we associate with the dipole alone, as it grows longer as a function of wavelength. In contrast, the Yagi gain shows a continuous rise with frequency. Just above the band edge, it will peak and then the Yagi will reverse its direction. The front-to-back ratio of a Yagi peaks at mid band and declines toward the band edges.

Paralleling the performance curves are the SWR curves. Figure 6 shows three curves, each referenced to the self-resonant impedance of each antenna. The broadest curve belongs to a simple dipole, in this case, using a 4 mm diameter element, like all other elements in these notes. The planar array curve comes next and shows that the antenna provides impedance bandwidth almost as wide as the gain and front-to-back curves. In contrast, the 3-element Yagi provides less than a 2:1 SWR only over about half of the 70 cm band.

Table 2 has a special final entry. We may simulate a solid planar reflector by using a series of rods in the plane of the driver. Obtaining the performance of a solid or screen reflector has several requirements. As shown in Figure 7, the total area of the rod reflector, much used in the past for television antennas, must equal the area of the screen reflector. In addition, the simulated solidity of the screen depends upon using a number of rods and an individual rod diameter that together fill in the screen. The fewer the rods we use, the fatter we must make each rod. The present example uses 13 rods, each 0.036 λ (25 mm at 435 MHz) in diameter. In most applications, the performance of a rod reflector is the same as an equal-sized screen. In other optically based reflector forms, such as corner reflectors, the rod reflector will show hybrid characteristics, partly parasitic and partly optical.

Parasitic "Reflectors"

Applied to a parasitic array, the term *reflector* is simply a conventionalized term used to locate the appropriate element. The fact that it is normally — but not always — longer than the driver element leads to misimpressions about how it works. In fact, parasitic arrays are special forms of phased-element sets in which we let the geometry of the elements determine the correct relative current magnitudes and phase angles of the elements for directional operation. For arrays based on half-wavelength elements, we normally measure the current magnitude and phase angle at the element center, where the current reaches its peak value.

When we have only two elements of equal or nearly equal length, we can find relative current magnitude and phase angle combinations that yield a maximum front-to-back ratio and other combinations that yield maximum gain. The values for each combination vary with the spacing and the exact length of the elements involved. Let's turn to a 10 meter portable beam that I built a number of years ago. Table 3 shows the dimensions of the array, and the two lower entries provide the ideal figures for either a very high 180° front-to-back ratio or for maximum gain (with a front-to-back ratio in the 7 to 8 dB range).

Figure 8 provides outlines of two forms for the same element set. The first form

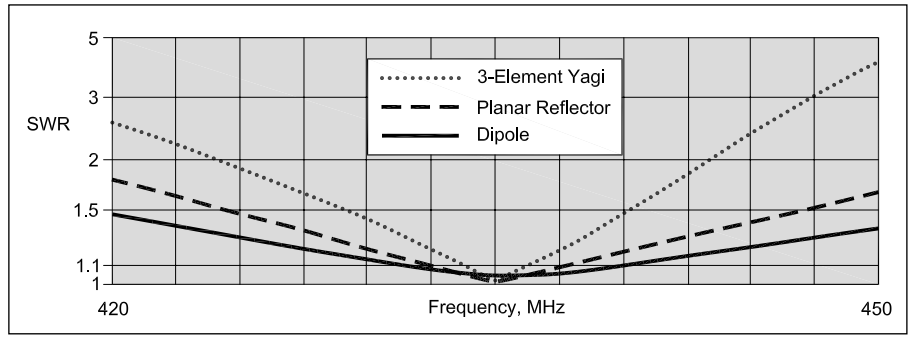

Figure 6 — SWR curves relative to the resonant impedance of a simple dipole (solid line), a planar reflector with a dipole driver (dashed line) and a 3-element Yagi (dotted line).

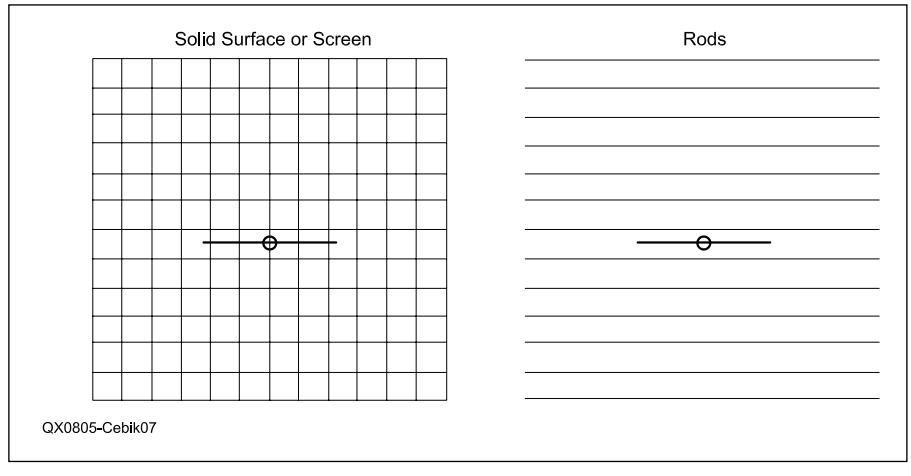

Figure 7 — General layout of a wire-grid planar reflector simulating a solid or screen surface and of a series of rods having the same limiting dimensions.

Table 3
Performance comparison of parasitic and phased 2-element beams. Note: Both 28.5 MHz beams are identical: rear element length = 211.2", forward element = 198.0", spacing = 57.6". Phased version uses a 4"forward line and a 54"aft line of 50 Ω 0.66 VF cable with an addition λ/4 matching section to the main feed point.

Type	*Gain dBi*	*F-B Ratio dB*	*Element Currents and Phase Angles* *Rear*	*Forward*
Parasitic	6.24	10.99	0.664 @ 140.3°	1.0 @ 0.0°
Phased	6.45	21.00	0.871 @ 135.4°	1.0 @ 0.0°
Ideal for maximum F-B ratio			0.995 @ 127°	1.0 @ 0.0°
Ideal for maximum forward gain			0.963 @ 160°	1.0 @ 0.0°

employs the beam as a standard driver-reflector Yagi. As the tabular values show, confirmed generally by the free-space E-plane pattern, the beam has modest performance but is typical of the genre. The second form of the beam adds a harness of transmission lines that improve the current magnitude and phase angle relationships between the forward and the rear elements relative to the beam direction. (It is somewhat of a mistake to label phased-array elements as a driver and a reflector.) The gain increases slightly, but the most noticeable operational improvement is the front-to-back ratio. As the E-plane pattern shows, the entire rearward radiation has decreased very significantly.

The exercise simply points to two significant facts about parasitic reflectors. First, we use a reflector size and spacing to obtain as best we can within physical geometry limits a current magnitude and phase angle combination to enhance the directivity of a beam. Second, relative to the driver, the reflector phase angle will normally be positive. As we add directors to a Yagi array, the role of the reflector changes. Although we may adjust its position and length to enhance performance slightly, it serves largely to set the driver's impedance. How much of a role the reflector element plays in obtaining a desired level of gain or front-to-back ratio depends upon the particular Yagi design.

As we increase the number of elements in a parasitic beam, the simple relationships in the current amplitude and phase angle among the elements tend to shift. The reflector remains at a positive phase angle relative to the driver in almost all cases, while the first director ahead of the driver will have a negative phase angle relative to the driver. (For exercises in this regard, we normally set the driver current magnitude at 1.0 and a phase angle of 0.0°. The normalized setup eases the process of comparing values among beam designs.) As soon as we use even one director, the idealized

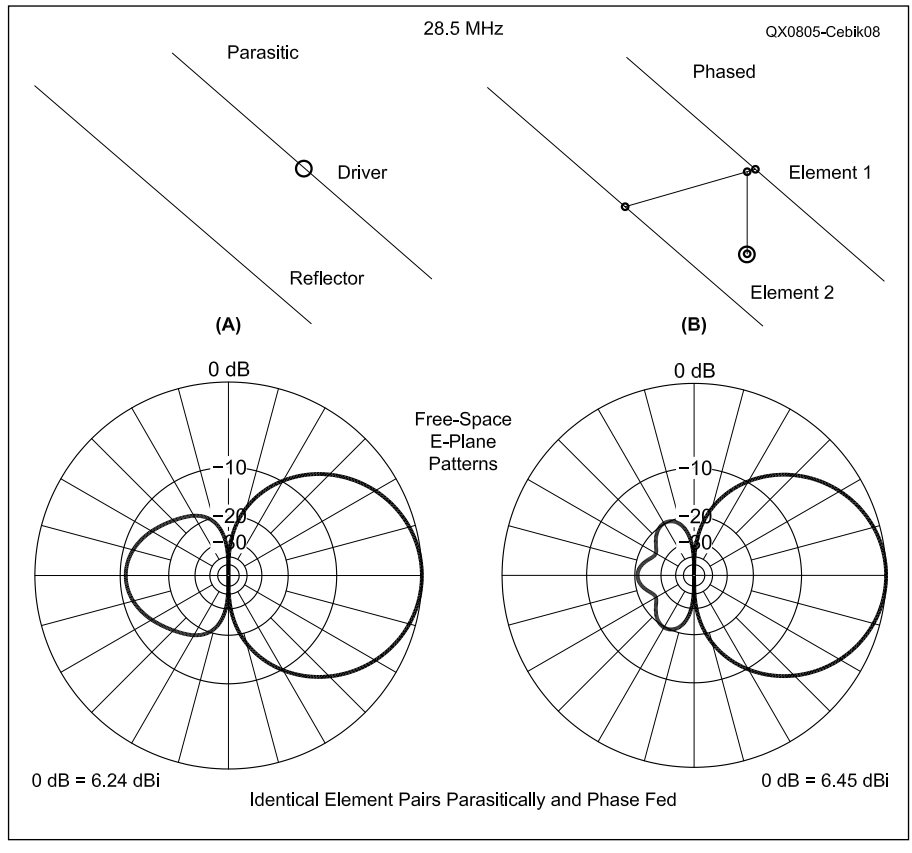

Figure 8 — Two identical sets of 10-meter elements set up for parasitic feeding and for phase feeding, with corresponding free-space E-plane patterns.

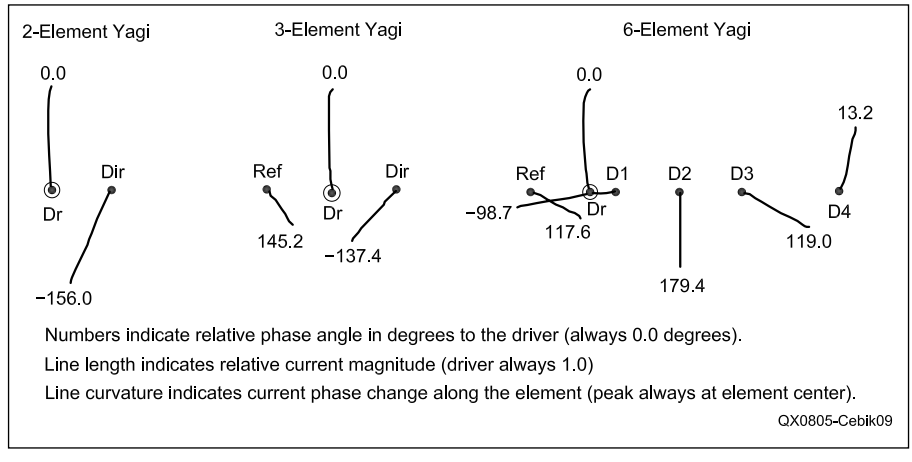

Figure 9 — The relative current magnitudes and phase angles on the elements of various types of Yagi antennas.

Table 4
Element center relative current magnitudes and phase angles of three different Yagi antennas; see text for brief beam descriptions.

No. of Elements	*Element Name*	*Relative Magnitude*	*Phase Angle*
2	Driver	1.0	0.0
	Director	0.995	–156.0
3	Reflector	0.401	145.2
	Driver	1.0	0.0
	Director	0.635	–137.4
6	Reflector	0.536	117.6
	Driver	1.0	0.0
	Dir 1	0.955	–98.7
	Dir 2	0.727	179.4
	Dir 3	0.714	119.0
	Dir 4	0.650	13.2

2-element relationships become void relative to specific values.

Table 4 provides the element-center current magnitude and phase angle values for three Yagi beams: a 2-element driver-director array, a 3-element antenna and a 6-element OWA (optimized wideband antenna) design. Figure 9 shows the current magnitudes and phase angles in graphical form. The length of each line is proportional to the relative current magnitude, while the angle is proportional to the phase angle relative to the vertical line for the driver current. Some of the lines have perceptible curves, indicating the change in the current phase angle along the element from the center peak to the element end that intersects with the edge dot representing the element. In this set of examples, a counterclockwise direction indicates a negative phase angle, while a clockwise direction indicates a positive phase angle. (If you model antennas and replicate this exercise using par-

asitic beams of your choice, be certain that all elements — and sections of elements in stepped diameter element designs — use the same orientation. Universally reversing the element direction will reverse the clockwise counterclockwise orientation of the graphs, while randomly changing element and element section directions will yield a largely unreadable graph.)

The 2-element Yagi shows a relative director current that is nearly identical to the value of the driver, with a relative phase angle of –156°. At the design frequency (435 MHz), the two elements have nearly ideal conditions for achieving a high front-to-back ratio. Maximum front-to-back values would require a relative current magnitude of about 1.025 with a phase angle of –154° at the element spacing shown (0.08 λ). (Note that with two elements, the required ideal current magnitudes and phase angles will be the same relative to the forward and rearward elements. In a parasitic design, however, the particular element we feed makes a considerable difference in the ability to find a geometry that will produce desirable results. The present design produces excellent performance, but only over a very narrow bandwidth.)

The current magnitudes and phase angles associated with the 3-element Yagi coincide roughly with at least the phase-angles rules of thumb. The reflector phase angle is positive, while the director phase angle is negative. The exact values are functions of the element lengths and their spacing from the driver. There are numerous configurations for 3-element Yagis, each suited to a specific performance task. In each case, the exact values will be different from those shown for the same beam.

Table 5
Free space performance comparison among identical 435 MHz element sets (driver plus 10 directors, all 4 mm in diameter) with different reflector assemblies.

Reflector Type	*Gain dBi*	*F-B Ratio dB*	*Feed-Point Z R ± j X Ω*
None	12.99	13.08	48.1 – *j* 7.5
1 element	14.15	21.45	57.5 + *j* 9.8
3 elements	14.31	37.10	60.4 + *j* 8.7
Screen	14.28	33.25	59.2 + *j* 12.8

Note: single reflector element is 348 mm long; additional two reflectors are 350 mm long and spaced 15 mm behind the center reflector and 210 mm above and below the main element axis. The screen required for the performance shown is 500 mm by 500 mm and in the normal single-reflector position.

The 6-element Yagi illustrates how complex the pattern of current magnitude and phase angle values may become as we add directors and configure them for desired performance levels. The example beam has a wide bandwidth (relative to Yagis as a whole) in part controlled by the close spacing of the driver and the first director. Above the design frequency, the first director's current magnitude will actually exceed the magnitude on the driver and forms a secondary driver to control performance at the higher end of the operating spectrum. Hence, the current magnitude and phase angle values on the array element will shift with the operating frequency.

In fact, we normally design parasitic beams by reference to the performance they yield, letting the current magnitudes and phase angles be whatever they must be to obtain that performance. Antenna modeling software abets this process, since the performance values generally appear with polar plots of anticipated radiation patterns. Hence, many beam designers never look at the current values on the elements. This process helps us forget that parasitic reflectors do not reflect in the optical sense. Rather, they remain part of the phasing system for a directional set of elements.

The Interchangeability of Planar and Parasitic Reflectors

The idea of replacing a parasitic reflector with a planar reflector is natural, but

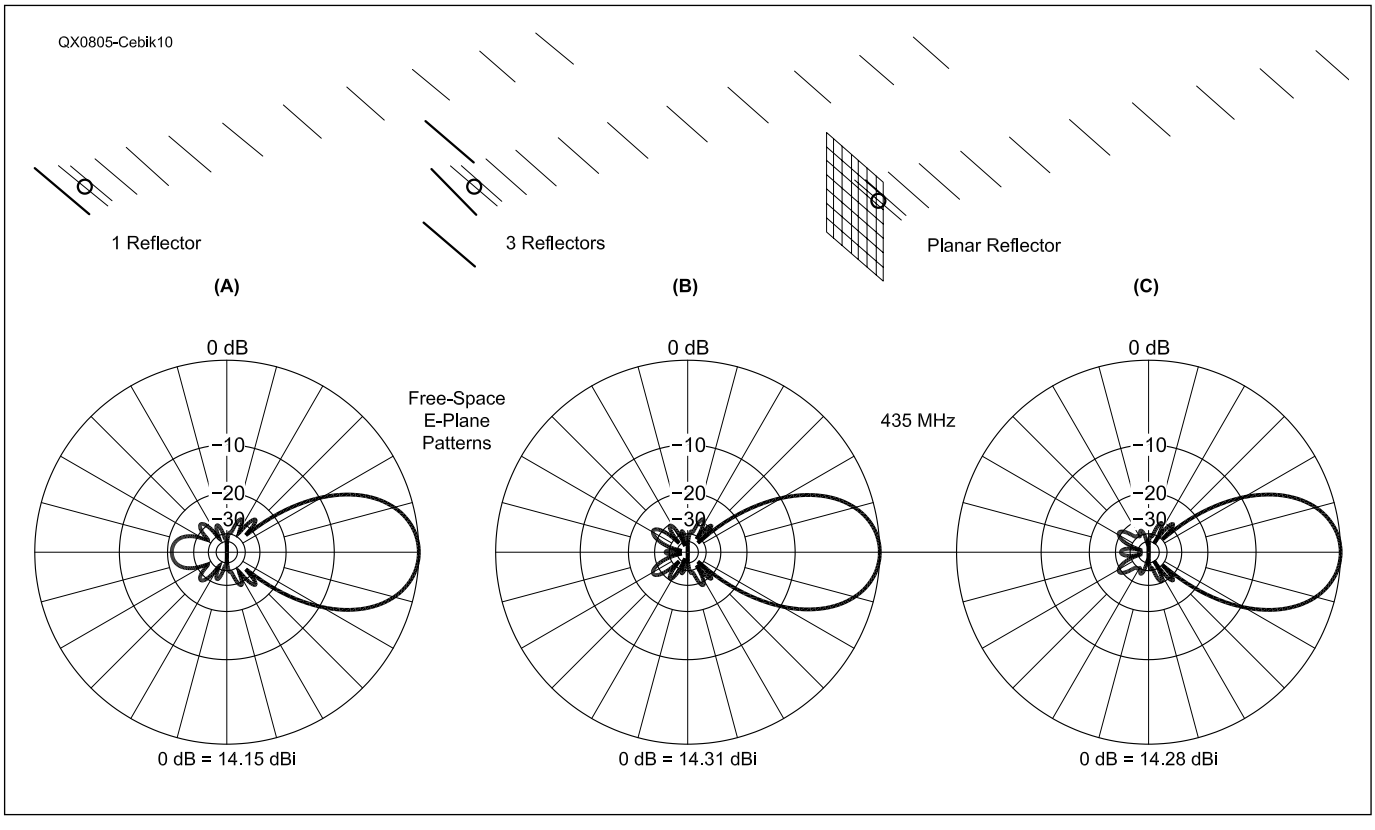

Figure 10 — Identical driver and 10-director element sets with different types of reflector elements.

filled with questions. The key question is whether we gain anything in the process. Long-boom Yagi enthusiasts have pondered this question since (at least) DJ9BV's use of a reflector plane consisting of four reflector elements. The spacing between the reflectors was too wide to form a true planar reflector, but the builder claimed additional performance relative to a single reflector.

The feasibility of replacing a single parasitic reflector with a planar reflector depends in large part on the radiation directed toward it. Therefore, the key test is whether the set of elements from the driver forward and with no reflector element has a large rearward lobe or a set of lobes. In such cases, a planar reflector or some other system of reflectors may improve performance over a single parasitic reflector. Figure 10 outlines a series of 70-cm arrays that use a driver with 10 identical directors. The sketches show a single parasitic reflector, a system of three reflectors and a planar reflector. Table 5 shows the results of the experiment.

A single reflector element provides good performance from the array. The free space gain is over 14 dBi, and the front-to-back ratio is greater than 20 dB. The second step adds two further reflectors, each about 2 mm longer than the original and spaced 15 mm behind the central reflector element. The vertical distance between these reflectors is 420 mm. The augmented parasitic system increases the gain by less than 0.2 dB. The 180° front-to-back ratio gives us an illusion of a high improvement in the rearward direction, but the pattern in Figure 10 shows that there are quartering rear sidelobes that are down by only about 5 dB relative to the single-reflector version.

The final step in the progression replaces the system of reflector elements with a planar reflector. To obtain the performance of the three-reflector model, the screen required 500 mm by 500 mm dimensions. Whether either *improved* reflector system is worth the construction effort may depend as much on mechanical factors as on performance benefits. The three-reflector system is complex, requiring a boom extension and a vertical support for the elements. The planar reflector might consist of light screen material, but it would require bracing to maintain its shape. Both augmented reflector systems would add to the wind forces on the antenna. Hence, the decision to use an augmented reflector system must weigh performance against potential mechanical disadvantages.

A planar reflector may give the illusion of improving the performance of a smaller Yagi. Consider the 2-element driver-director array that we used to show current magnitudes and phase angles on the elements. Since it has no reflector, perhaps adding a planar reflector might improve performance. Figure 11 shows the outline and the free-space patterns of the two arrays. The pattern with the higher gain belongs to the version with the planar reflector. In this case, the presence of the reflector appears to improve performance — at least with respect to gain — by almost 2 dB. The key pattern modification is the reduced beamwidth of the planar version.

Consult Table 6. The first two entries confirm the impression that we gleaned from the patterns. The final entry shows what is actually happening. With only a dipole, a planar array has virtually the same performance as the reflector with 2 elements ahead of it. The director adds nothing to the planar array performance, but does reduce the feed point impedance. For the best performance, we might keep the planar reflector and do away with the parasitic director.

Planar and other optically based reflectors depend upon the illumination provided by the source. Planar arrays are most effective with either single drivers or collections of phase-fed drivers properly spaced ahead of them. Corner arrays tend to require single dipole drivers or end-to-end arrays of drivers, since the illumination of a corner reflector with a 60° to 90° angle is quite complex. Parabolic reflectors operate best when the total driving source energy points toward and illuminates the entire parabolic surface. Ray tracing graphs and equations best describe the function of each type of reflector.

In contrast, parasitic reflectors require positions and lengths that determine the optimal current magnitude and phase angle for directional-beam operation. The exact values depend upon the complex interaction of all of the antenna elements, however. Although we can certainly design Yagi and other parasitic beams without reference to element current magnitudes and phase angles, reference to these parameters may help us understand why a Yagi is not a flashlight.

Table 6
Comparative free-space performance of 3 antennas.

Antenna Type	*Gain dBi*	*F-B Ratio dB*	*Feed-Point Z* $R \pm j\,X\ \Omega$
2-ele. Dr-Dir Yagi	6.64	20.29	21.1 – *j* 0.5
2-ele. Yagi + planar reflector	9.17	19.31	19.1 + *j* 4.0
Dipole + planar reflector	9.31	18.34	50.1 – *j* 0.3

Note: 2-element Yagi element spacing is 0.08 λ. Added 1.2 λ by1.2 λ planar reflector is spaced 0.08 λ behind the driver. The planar reflector and dipole spacing is 0.175 λ.

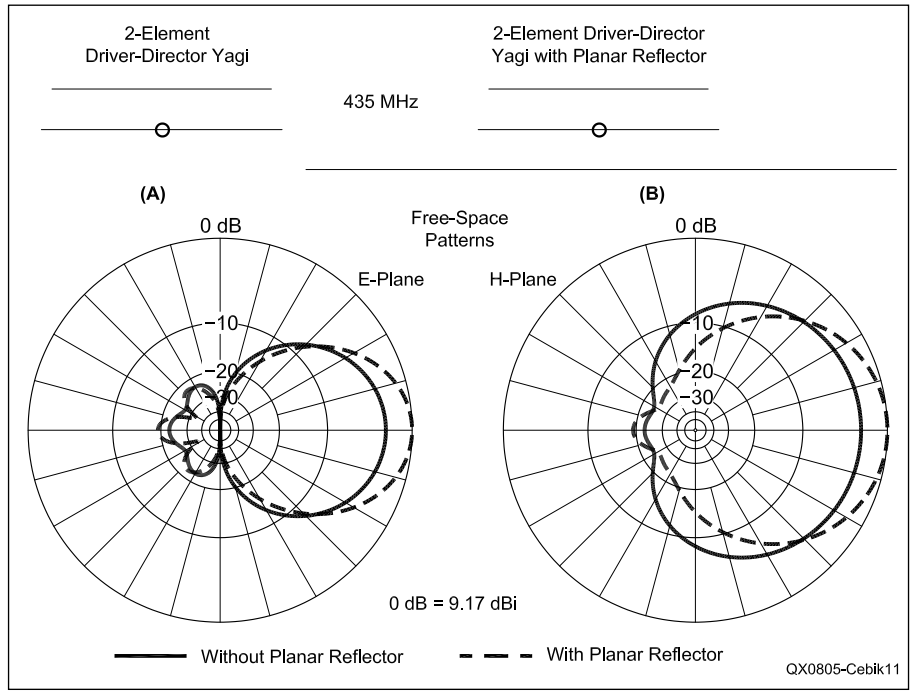

Figure 11 — General outline and free-space patterns of a 2-element driver-director Yagi, with and without a planar reflector (solid line = without planar reflector; dashed line = with planar reflector).

Raymond Mack, W5IFS

17060 Conway Springs Ct, Austin, TX 78717-2989

Out of the Box

New Sources for UHF and Microwave Semiconductors

This is a double purpose announcement. The first is that the group that was originally the Hewlett-Packard Semiconductor Group, then Agilent Semiconductors after the spin-off, is now known as Avago Technologies. The other news is that Mouser Electronics is now a distributor of the Avago line of RF parts, including silicon and GaAs low noise transistors and ICs. Many of the microwave parts you have seen in *QEX* articles are available from stock. As a bonus, Mouser provides direct links on their web page to Avago design information on each part. Clicking on the datasheet link takes you to an Avago web page with datasheet and application information.

If you cannot find the parts you need at Mouser, you can try Digi-Key who also stock Avago parts. You will find links on their web page to Avago data sheets, as well.

Avago Technologies
350 W Trimble Rd
San Jose, CA 95131
Tel: 800-235-0312
www.avagotech.com

Mouser Electronics, Inc
1000 North Main St
Mansfield, TX 76063
Tel: 800-346-6873
Local: 817-804-3888
Fax: 817-804-3899
www.mouser.com

Digi-Key
701 Brooks Ave South
Thief River Falls, MN 56701
Tel: 800-344-4539
Local: 218-681-6674
Fax: 218-681-3380
www.digikey.com

Unusual Local Sources for Parts

While searching for things unrelated to Amateur Radio recently, I discovered two unlikely sources of electronic items.

Meter Fuses

Fluke and other digital voltmeters use large cartridge fuses for the ammeter portion. The smaller fuse is 1 A and the larger fuse is 15 A. Lowes Home Centers carry a KTK-15 that will replace the 15A fuse. They also have a 1 A fuse but it is currently on closeout.

Magnet Wire

It is much easier to keep the windings straight in multiple winding transformers if each winding is a different color of wire. Unfortunately, Belden magnet wire is only readily available in one color which is essentially red. RadioShack has a small assortment of magnet wire in varying colors, with each color a different wire gauge. A more surprising source of smaller gauge wire (no. 18 down to about no. 30) is Michael's Craft Stores. They carry enamel covered copper wire for decorative craft use in a very large number of colors.

Since this wire is not intended for electronics use, it is most useful for low voltage circuits. If you need to use it at high voltage, you will want to do a voltage withstand test. I was surprised that even Belden magnet wire was compromised in a two layer toroid that had 1000 V ac across the coil, so testing for your application is indicated.

Atmel Microcontroller Design Tools

Thomas C. Baier, DG8SAQ, wrote an article in the Jan/Feb 2008 issue of *QEX* describing a USB adapter to interface a DDS based Vector Network Analyzer to a computer. This device used a small Atmel microcontroller as the USB controller. This is the first Amateur Radio project I remember seeing that has used a microcontroller other than a PIC. I use the Atmel parts in my day job, so I can pass along some hints on their use.

Programming

Dr. Baier described using *PonyProg*, some logic, and the parallel port of the computer to program the Atmel AVR devices. The logic required is very simple but it still requires you to buy the parts and assemble the interface to translate from the parallel port to the ISP (In System Programming) interface of the microcontroller. For not much more than the cost of the parts for the parallel port interface, you can buy the AVRISP mkII from Digi-Key or Mouser ($35.91). This device connects to three IC pins on the target ISP connector and a USB port on the computer. The AVR Studio development environment does not need a third party driver like *PonyProg* to support this programmer.

You do not lose the three pins for I/O operation. Including isolation resistors in the design allows the three pins to do double duty as programming pins and I/O pins.

Debugging

Atmel has several ways to debug code on their parts. All methods give you a debugger environment similar to what you may have used for *Delphi* or *C* development on *Windows*. The function keys do the same functions that are assigned in Microsoft *Visual C++*, so there is less of a learning curve.

The method with the least hardware support is the simulator. This creates a virtual Atmel CPU on your PC. This method is severely limited for testing real hardware, however.

The larger CPUs (like the ATMega32) have a JTAG interface using four pins, which allows direct control of internal resources and full debugging support. These ICs have internal emulation logic so a dedicated ICE (In Circuit Emulation) chip is not required. This debugging is supported by the JTAGICE mkII ($317.87). This mode allows you to set breakpoints, watch variable values, and read or write any data memory location including the I/O registers. JTAG is included only on the larger microcontrollers because you cannot use the four pins for I/O as well as debugging. The JTAGICE also connects to the PC by way of a USB port.

The price tag is non-trivial, but the amount of time saved for two or more complex designs will easily pay for the device. The cost of an ICE pretty much locks you in to a particular manufacturer for future projects, but Atmel has a broad line of parts. You do not need the AVRISP if you use the JTAGICE, because the ICE has a programming feature.

Atmel has implemented a debug connection for its small microcontrollers like the ATTiny2313 called *debugWIRE*, which uses the reset pin to communicate with the internal emulation logic. This method only eliminates one I/O pin as the price of doing full debugging. The JTAGICE mkII is also used for *debugWIRE* operation.

Both *debugWIRE* and JTAG debugging write BREAK instructions to the FLASH memory. The large number of writes decreases the longevity of the FLASH, so you may want to buy an extra part for long term use once the software is finalized.

Atmel
2325 Orchard Parkway
San Jose, Ca 95131
www.atmel.com

Mouser Electronics, Inc
1000 North Main St
Mansfield, TX 76063
www.mouser.com

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701 Brooks Ave South
Thief River Falls, MN 56701
www.digikey.com

Letters to the Editor

A Low-Cost, Flexible USB Interface (Jan/Feb 2008)

Hi Larry,

Thanks for publishing my article in such a nice way. When I looked at it in *QEX* I noticed a little typo in the schematic of Figure 1 on page 11. The signal at U1, the ATTiny2313 IC, pin 15 now reads "DDS SC Lock." It should read "DDS Clock." Maybe you print a little correction note in the next issue of *QEX*.

— Thanks and 73, Thomas Baier, DG8SAQ, University of Applied Sciences, Prittwitzstrasse 10, 89075 Ulm, Germany; **baier@hs-ulm.de**

Hi Tom,

I apologize for that error on the schematic diagram. Thanks for helping us make our readers aware of the correction.

— 73, Larry Wolfgang, WR1B, QEX Editor; **lwolfgang@arrl.org**

Empirical Outlook (Mar/Apr 2008)

Hi Larry,

I enjoyed your comments in Empirical Outlook, and agree that there is a lot of good experimentation out there that doesn't get written up. I personally get a big kick out of writing technical material, (as well as a lot of other stuff), and I would be more than happy to be a "ghost writer" for any experimenter who might think he needs one.

I'm sure there might be a few others out there as well, and I encourage any more experienced wordsmiths to, perhaps, think about doing this as well.

— Sincerely, Eric Nichols, KL7AJ, Hard Right Productions, 3763 Lyle Ave, PO Box 56235, North Pole, AK 99705; **kl7aj@acsalaska.net**

A Squelch Amplifier (Jan/Feb 2008)

Larry,

There is an error in the schematic (Figure 7 on page 38) for the +DC to –DC converter that is part of the article "A Squelch Amplifier," in the Jan/Feb 2008 issue of *QEX*. Capacitor C6 is installed backwards. The + terminal should be connected to ground, because the input voltage for U1 is negative.

I wish the circuit board was a little smaller. This circuit would be an excellent replacement for the various Kenwood radios that experience unstable output due to failure of the –6 V regulator that is the ALC reference voltage.

— 73, Steve Lund, K6UM, 15385 NE Kincaid Rd Newberg, OR 97132-6926; **k6um.steve@gmail.com**

Dear Larry,

Thanks for forwarding Steve's message. I note that C6 and C7 are both in error. The + side of both capacitors must be connected to ground. Also, the output labeled $+E_0$ is actually an unregulated –V output. The output from the "REG Out" terminal is a regulated –V output.

— 73, John Laughlin, KE5KSC, 11918 Pompano Ln, Houston, TX 77072; **johnel@earthlink.net**

Dear Steve and John,

Thank you for writing with those corrections. The mistakes on Figure 7 were either errors in the way I marked up the original drawing for our graphics artist, or errors he made that I didn't catch in the reveiw process.

— 73, Larry, WR1B; **lwolfgang@arrl.org**

Carbon Composition, Carbon Film and Metal Oxide Film Resistors (Mar/Apr 2008)

Dear Larry,

I just wanted to let you know I really enjoyed the article in the Mar/Apr 2008 issue by K8ZOA, Carbon Composition, Carbon Film and Metal Oxide Film Resistors. I found it quite interesting and picked up a lot of good knowledge from it. Sorry I can't wax eloquent; I don't do eloquent, but I do know when a good, well written article on a seemingly basic subject warms the cockles of my homebrewer, engineer-wannabe heart.

— 73, Mike Czuhajewski, WA8MCQ, 7945 Citadel Dr, Severn, MD 21144; **wa8mcq@verizon.net**

Hi Mike,

Thanks for the note to let us know you enjoyed Jack's article. I was also fascinated to read the report on his research. It looks like good science, with carefully documented measurements under reasonably controlled conditions.

— 73, Larry, WR1B; **lwolfgang@arrl.org**

The Direct-Reading Reflection Coefficient and Power Meter (Nov/Dec 2007)

Dear Larry,

Thanks for publishing the errata / comments list for my Nov/Dec article in the Jan/Feb *QEX* Letters column.

There are "typos" and then there are "thinkos." Further thought and experimenting have convinced me that using the RC/P meter's reflection coefficient mode for insertion loss measurements is neither as simple nor as useful as it first appeared to be.

First of all, the resolution and stability of the RC zero adjustment make measurement of small values of RC very difficult, requiring frequent re-zeroing. A multi-turn wire-wound zero adjusting pot would presumably cure this problem.

More importantly, phase shift through the device under test invalidates the attenuation results, unless at the test frequency the total forward and reverse direction phase shift is negligible or a multiple of 360°.

For example, a shorted transmission line will have a real and minimum impedance at lengths of multiples of a half wavelength, and in principle, the reflection coefficient at these frequencies can be scaled to give the loss at the operating frequency. This is a very tedious and indirect measurement, and all told, measurement of attenuation by substitution in the power meter mode is far preferable.

With the benefit of hindsight, I'd delete the fourth sentence of the Introduction, and the fourth paragraph under Operation, so perhaps a further errata note is indicated.

In the Introduction, I would delete the sentence that says, "Among other applications, the meter provides a very simple and useful way to measure the loss of a device or a transmission line *from one end!"* The fourth paragraph in the Operation section begins with the sentence, "This effect of loss on RC provides a useful way to measure loss."

— 73, Ralph Gaze, W1RHG, 35 Linda Terrace, Portsmouth, RI 02871; **rgaze@arrl.net**

Hi Ralph,

Thanks for your further thoughts and clarifications about your direct-reading reflection coefficient and power meter. It is still an interesting and useful project, even if the loss measurement isn't as easy as you originally thought.

— 73, Larry, WR1B; **lwolfgang@arrl.org**

Antenna Options (Jul/Aug 2007)

I have two questions regarding the Antenna Options column in the Jul/Aug 2007 issue of *QEX*. The first question concerns the Stub Loaded 2-Element Moxon Rectangle discussion. On page 55, the author says that the electrical length of the loading stub for a 30 m Moxon is 140.6 inches. When I calculated the required electrical length of the 30 m stub (at 10.125 MHz) I came up with a value of 169.8 inches. Please re-check and confirm the electrical length value for the 30 m stub that was published in the article.

Second question: On page 55, in the first paragraph under the heading "The Stub Loaded 2-Element Yagi," the author says,

"On 40 m the coax length is 258.8 inches, while on 30 m, the length is 182.3 inches." The author does not specify whether he is talking about the physical or electrical length of the coax stub. Which is it? I suspect he is referring to the stub's electrical length, but it is not clear.

You may be interested to know that I am using your Antenna Options notes to construct a reversible, stub loaded 2-element 17 m Yagi in my attic.

The Yagi will replace a 17 m Moxon that is now located there. The Moxon has worked very well but the dimensions of the attic prevent me from rotating the antenna. Because I cannot rotate the Moxon, I have been looking for ideas for bi-directional gain antennas that will fit in my attic. Your column in the Jul/Aug 2007 issue of *QEX* solved my problem. I elected to use the reversible Yagi concept rather than the reversible Moxon because the Yagi is, for my situation, simpler to construct.

— 73, Frank Riley, KK0K, 11721 Woodward St, Overland Park, KS 66210; **frankriley@kc.rr.com**

Dear Frank,

The Yagi stub lengths are electrical lengths for both the 40 and 30 m versions of the 2-element stub-loaded reversible Yagi, as shown in the model. For the stub-loaded Moxon, electrical lengths were intended, as shown in the models with a VF of 1.0, but, alas, I goofed on 30 m, and used the physical length based on a foam coax VF of 0.82. So, Frank, you are correct about the electrical length being just under 170 inches (0.146 λ, or close to 52.5 electrical degrees). Keep in mind, however, that real-world antenna site factors will require experimental determination of the final stub length for the situation.

I hope this helps.

— 73, L. B. Cebik W4RNL, 1434 High Mesa Dr, Knoxville, TN 37938; **cebik@cebik.com**

Thanks for the correction and clarification, L. B.

— 73, Larry, WR1B; **lwolfgang@arrl.org**

Signal Resilience to Ionospheric Distortion of HF Digital Chat Modes (Nov/Dec) 2007)

Daniel,

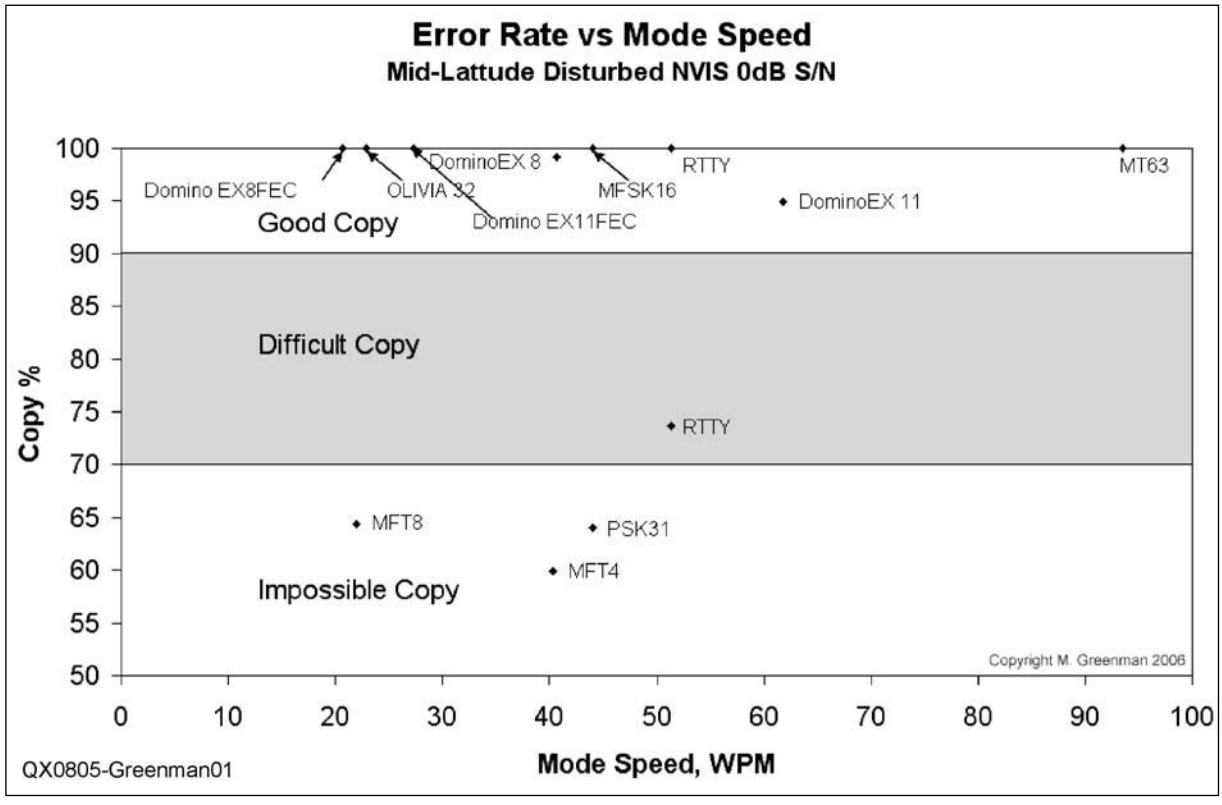
First, may I congratulate you for the excellent article, "Signal Resilience to Ionospheric Distortion of HF Digital Chat Modes," published in the Nov/Dec 2007 issue of *QEX*. The article is well written, and it is encouraging to see that serious attempts at analyzing digital mode performance (apart from mine, and that of Steve Richards, G4HPE) are now being undertaken. I fully appreciate how much work is involved in making these measurements.

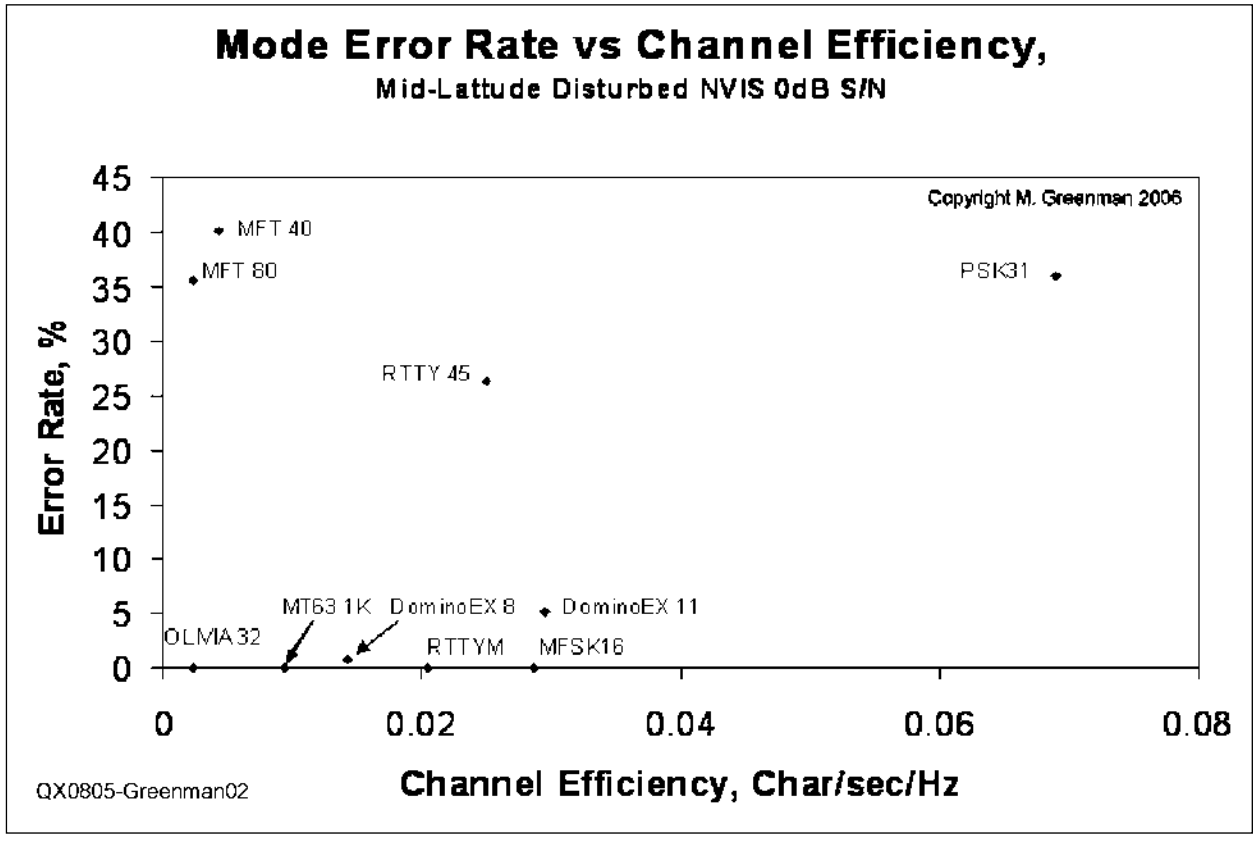
I have been making assessments of digital modes for some time now, partly as an on-going research, partly to compare software packages, and partly to compare new developments with the existing modes. I was pleased to discover that you use the same tools (specifically the PathSim program by Moe Wheatley, AE4JY), and that your method of rating copy performance is similar to my own. (You use %error, while I use %copy, but they are equivalent since %error = 100 – %copy.)

I have made PathSim recordings using DIRECT path for just about every mode imaginable. I used a one minute recording of "Quick Brown Fox," and play the file back through the required simulation, then rate the % copy manually by counting good characters and total characters (the latter by playing back with DIRECT path and no noise). When I started, there was no error rate measurement tool available. My measurements for the paths you discuss agree very well, despite slight differences in methodology.

There are, however, a few points where I feel you could have made a better emphasis, or provided more thorough results. These are:

1. You make no comment about which modes have FEC or high redundancy, and which do not. Users will wish to know how the modulation technique is affected by propagation, and in some cases this is masked by the use of FEC. I recognize that in some modes you can't turn the FEC off, but it does distort the results. For example, I know performance of MFSK16 (which I designed) is rather more modest with the FEC off.

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DominoEX 8
DominoEX 11
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0.04
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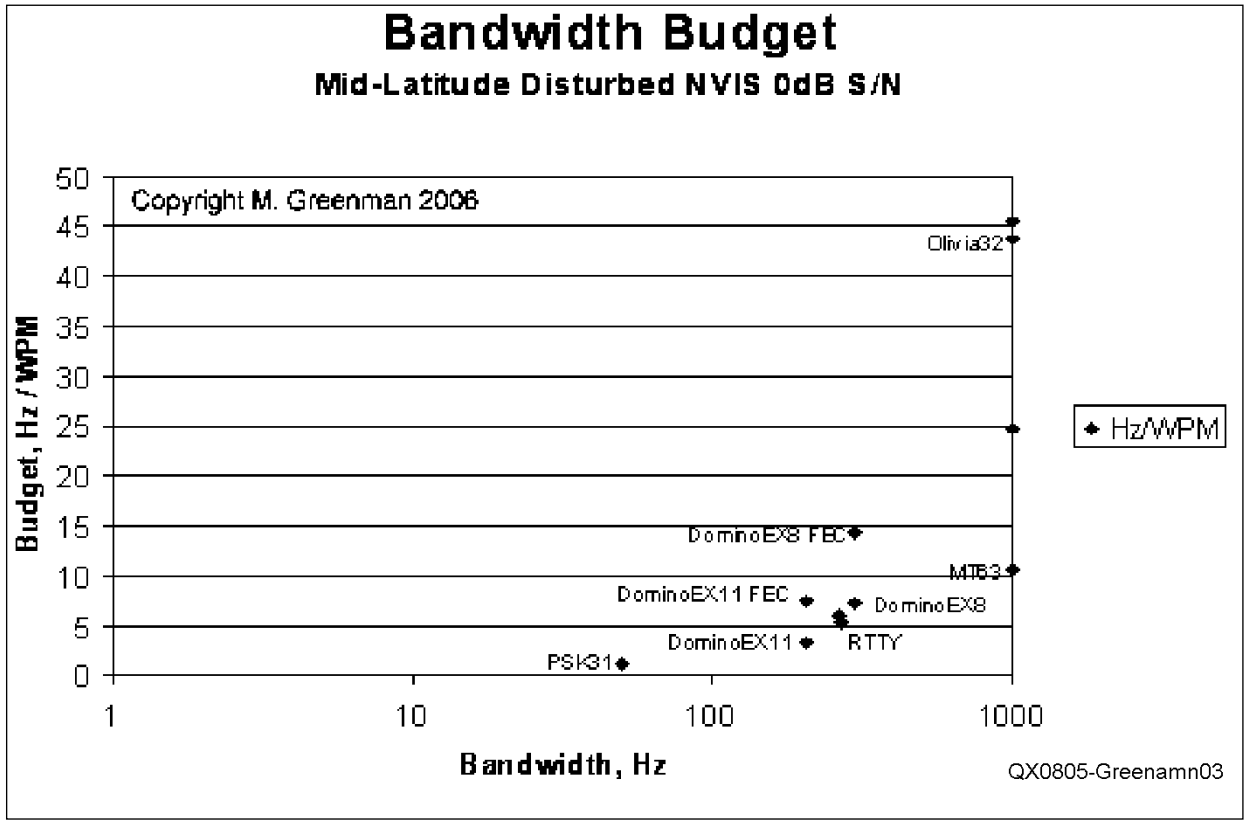
Channel Efficiency, Char/sec/Hz
QX0805-Greenman02


Bandwidth Budget
Mid-Latitude Disturbed NVIS 0dB S/N
Copyright M. Greenman 2006
Olivia32
DominoEX8 FEC
MT63
DominoEX11 FEC
DominoEX8
DominoEX11
RTTY
PSK31
Hz/WPM
Budget, Hz / WPM
0
5
10
15
20
25
30
35
40
45
50
1
10
100
1000
Bandwidth, Hz
QX0805-Greenamn03

2. On a related point, the FEC affects the throughput (typing speed) and adds significant latency (receiver delay), and users will be interested to know the cost of using the FEC.

3. You make no differentiation between wide bandwidth modes and narrow modes. There is significant interest in keeping bandwidth usage to a minimum and an assessment of the bandwidth cost (bandwidth per unit throughput) is very useful. Modes that are intentionally narrow-band should not be criticized for poorer performance without this understanding (and vice versa).

4. There is no assessment of mode throughput. Sure, MT63 performs very well in tests, but it has high redundancy (equivalent FEC rate of 7:64) and for a raw throughput of 640 bps achieves only 100 WPM. Similarly, while you give one of the plethora of Olivia modes good ratings in some tests, the bandwidth of 1 kHz and throughput of barely 25 WPM with horrendous latency are significant factors to users. (See later — I've included some bandwidth budget information.)

5. While you encourage operators to choose a mode that best suits conditions (and I heartily agree!), you then test some modes only in configurations that do not suit the conditions. In particular I am disappointed that you only tested DominoEX at 11 baud. It performs far better in 8 baud mode under many conditions, and DominoEX4 under AWGN performs at –18 dB S/N and still achieves 25 WPM with no latency (compare that with Olivia!)

6. Further relating to DominoEX, one of the important design points of this mode is that the receiver FFT should operate with 4× the resolution of the tone spacing. This provides for the ability to round out fractional differences due to drift, tuning offset, and most importantly, Doppler. This is done correctly only in the ZL2AFP DominoEX software, which even includes a Doppler meter. However, this approach is *not* used in MultiPSK (which instead uses AFC), and I believe this will lead to poorer performance in conditions with considerable Doppler shift, such as NVIS and Flutter. My point is that care needs to be taken to ensure that the performance measured is not an artifact of the software used. Another way to look at this is that the simulator provides us with a very good way to rate the performance of the receiving software!

7. Finally, I am sorry that you did not include an NVIS simulation (such as "Mid Latitude Disturbed NVIS"), which is very typical of low HF band operation — and let's be honest — these are very common conditions. In order to correct this, I've attached my own assessment of this simulation. Figure 1 shows the results of my error versus speed measurements. The error versus efficiency data of Figure 2 was measured at 0 dB S/N. Figure 3 is a bandwidth budget graph, again assessed at 0 dB S/N. I have figures for other amounts of AWGN, but will have to go back to the data to produce graphs with the same axes as yours.

As you probably will appreciate, at this point in the sunspot cycle, I've been working on designing modes that give good performance on noisy bands under NVIS conditions (80 m at night). I feel that with DominoEX, we have an excellent mode for these conditions, and it certainly helps if the range of simulations used in assessment point out clearly which mode is best under each of the conditions, but at what speed, what latency, and at what cost of bandwidth.

Perhaps there will soon be a Part 2 to your article!

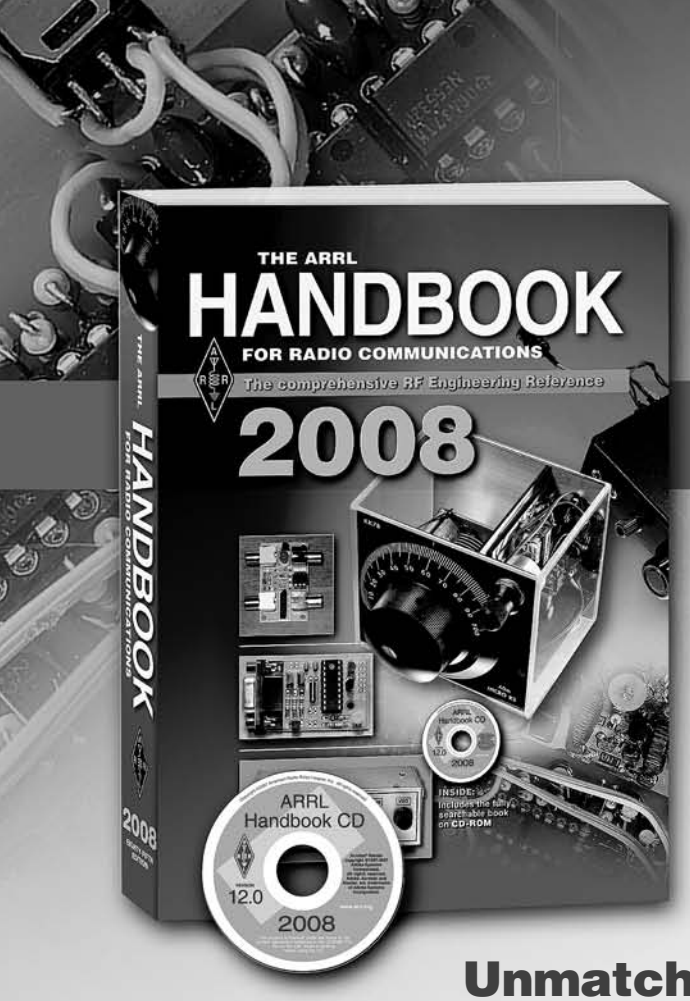
— 73, Murray Greenman ZL1BPU, 94 Sim Road, Karaka, RD1 Papakura, NEW ZEALAND; **murray@rakon.co.nz**

Hi Murray,

Thanks for your mail. I could not dream of a better critical opinion. I have read your comments and suggestions with great attention. I do consider your book and your Web site as the best references on the subject.

Thanks Murray. Your intervention is exactly what makes me love ham radio.

— 73, Daniel Crausaz, HB9TPL, Russel 7, CH1025 St, Sulpice, Switzerland; **cecidan@bluewin.ch**



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This is a microwave conference, so papers must be on topics for frequencies above 900 MHz. Examples of such topics include microwave theory, construction, communication, deployment, propagation, antennas, activity, transmitters, receivers, components, amplifiers, communication modes, LASER, software design tools, and practical experiences. Authors retain the basic copyright, and by submission, consent to publication in the *Proceedings* and possible publication of the *Proceedings* in CD/DVD format. If you are interested in submitting a paper please contact Jon Platt, WØZQ, at **w0zq@aol.com** for additional information. The deadline for papers is Sunday, August 31, 2008. If you are interested in presenting at Microwave Update please contact Barry Malowanchuk, VE4MA, at **ve4ma@shaw.ca**.

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- Since the HL-450B is compatible with our optional external remote controller (HRC-60), operation is possible from remote locations, if plugged into the socket at the rear panel.
- The HL-450B is equipped with a hard-key terminal to allow precise send / receive switching with the radio. Built-in ALC circuit helps suppress excessive output and avoid the signal distortion.
- The HL-450B has various protection circuits such as for high antenna SWR, over drive, over current, etc. When any abnormal condition is detected, operation is automatically shut down.
- The large analog power meter is easy to read and the output can always be monitored.

Built-in functions

1. Send / receive switching terminal (hard key)
2. Protection circuit (antenna SWR, over-current, over-voltage, over-drive, over-temperature, band mis-set)
3. Output power meter
4. ALC terminal
5. External controller (HRC-60, optional) terminal.

Specifications

Freq. Band:
All HF amateur bands of 3.5 - 28MHz

Operation Mode:
SSB, CW, FM

Output:
SSB (PEP) / CW 400W max.
350W typ., 300W min.

RF Input
50W

DC Power Supply
DC 13.8V 60A max.

Input / Output
50 ohms

Final Transistor
THP - 120 x 4

Cooling System
Forced-air cooling

Input / Output Connector
UHF (SO-239)

Accessories
DC power cord (red / black pair) 6' x1,
Coaxial jumper cable: 2' x1,
Stand-by cable (with RCA plug) 4' x1,
Spare fuses: 30A x4, Instruction manual, warranty card

Dimensions
8.7 x 3.5 x 13 inches (WxHxD)

Weight
Approx. 11lbs.

Option
External remote controller – HRC-60
Matching DC power supply – HP-450
(Light weight switching mode, 13.8V 60A)

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