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Issue No. 262



KG2MG shows you how to make complex impedance measurements with a bidirectional coupler and an HP 35s calculator.

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About the Cover

In this issue Michael Bowman, KG2MG, shows you how to make complex impedance measurements with minimal equipment. Our cover photo shows his measurement system consisting of a coupler, a signal generator, an oscilloscope, a DUT test cable, a checklist and a programmable calculator. Also visible is Michael's homebrew component that applies three calibration standards to a system's remote test cable: Short, Open and Matched Load.



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Raymond Mack, W5IFS

Empirical Outlook

Your regular editor, Larry Wolfgang, WR1B, is tied up with the 100th anniversary of Boy Scouting at the National Jamboree as one of many representing Amateur Radio. It is quite an honor. I am filling in for him this issue.

Bringing Digital Radio to Amateur Radio

Those of us who are Baby Boomers started in electronics before many people knew what digital electronics meant. Electronics meant military communications and radar, TV and radio, and telephones. Car phones and calling internationally were things only the rich or businesses could afford. Computers were expensive, big, and incomprehensible. Our children grew up in a more or less completely digital world, talking around the world essentially for free (10 cents per minute to call Paris, France and 11 cents per minute to call Paris, TX on a wireless phone) and having computers at their fingertips. It has been a struggle with that perspective to interest young people in radio. We may have come full circle now that significant amounts of digital operation involves radio in some form. One of the goals for those of us working on high speed multi-media (HSMM) is to provide a means for young people to combine computers and radio as either a hobby or a vocation.

Multiple groups of amateurs in Austin are working together to implement a mesh network of HSMM nodes. Think of this as similar to the D-Star network, but operating at a much higher data rate. The groups in Austin include ARES, Roadrunner Microwave Group, Texas Emergency Management, and Red Cross. There is also a fair amount of work being done in Dallas and Plano. Glenn Currie, KD5MFW, gave a presentation to a standing room only group at the Austin Summerfest this past Saturday, so interest is growing significantly. The group doing the heavy lifting of developing software and hardware has been very busy over the past year.

The original motivation for putting together the mesh node system was to develop a system that amateurs can deploy in a disaster area to provide modern communications capabilities. Operations in the aftermath of Hurricane Katrina and Hurricane Ike indicated that amateurs would need to provide even more than just voice communications. Amateurs are using the mesh concept to build a network where each node has the intelligence to automatically connect with all other compatible nodes that it can "see". The network is self configuring, so you don't need to know more than how to hook a CAT-5 cable from your computer to the HSMM node. WiFi, on the other hand, builds a system that connects two nodes at a time and requires significant understanding of networking to connect wireless access points (nodes) into a working network. The goal in Austin is to create a mesh network that connects all of the local hospitals to the Red Cross and the state emergency management center. Individual amateur stations are also part of the network to provide redundant means of entry and exit from the local network to the outside world just as would occur during a real disaster. One application is creating gateways between the mesh network and the Internet.

A "killer application" and instructions suitable for "ordinary" amateurs were two major pieces missing from the puzzle until recently. It appears that one killer application for HSMM mesh networks may be voice over IP. The group has developed software and hardware that allow a PC and mesh node to implement a private business exchange (PBX) with multiple phone connections. Work is continuing on the PBX applications. A second killer application may come from being able to connect smart phones like Android and iPhone to the mesh network. There was enthusiastic interest from young people at Summerfest for this application. The group has also made significant progress in developing useful instructions for those of us who are barely able to spell "PC". Jim Kinter, K5KTF, has put together a Web site (hsmm-mesh.org) that captures all of the information currently available. It has links to external information on the Linksys routers that are modified to become a HSMM mesh node as well as documentation on how to convert a router to a mesh node. The Web site is also the starting point for you to contact the folks working on the hardware and software if you wish to contribute to the effort.

If you understand networking, integrating applications on a PC, and can put that information on paper so others can understand it, your talents are definitely needed. If you have the connections to convince Broadcom that it is a civic benefit to assist with technical information on the BCM5232, your talents are needed.

The Roadrunner Microwave Group has members who are looking at ways to implement long haul circuits to connect geographically separated mesh networks. The goal is to connect mesh networks in all the major metropolitan areas as well as smaller areas such as Kerrville, Bastrop, and Corpus Christi. Ideas for methods are always welcomed. Part of that effort is to identify alternate 802.11 hardware that has technical support from the manufacturer, so we can avoid the problems of not knowing what is really inside the Broadcom IC.

There are any number of activities that will help with the process of turning mesh networks into a robust emergency tool as well as a source of recreational enjoyment. There is a need for software folks to help with the development of the node firmware. There is also a need for folks who understand the PC part of the software equation to help with ideas for new killer applications. One of the most important things you can do is to get a node on the air and start using the system. It's no fun talking to yourself!

It is interesting that the concept of a mesh network is a modern embodiment of the original purpose of the ARRL: it is an Amateur Radio relay network.

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- 1) provide a medium for the exchange of ideas and information among Amateur Radio experimenters,
- 2) document advanced technical work in the Amateur Radio field, and
- 3) support efforts to advance the state of the Amateur Radio art.

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A Simple Path to Complex Impedance

Make complex impedance measurements with a bidirectional coupler, some voltage measurements and a program for an HP 35s calculator (or an Excel spreadsheet).

There are many high-performance portable and PC-based radio frequency (RF) impedance analyzers and vector network analyzers (VNAs) available for amateurs to buy, as well as stand-alone lab-grade analyzers. I used to have such instruments at work, but since becoming unemployed in the economic downturn, I have lost my access to the lab-grade equipment. That prompted me to design a “simple path” to complex impedance measurements using my inexpensive programmable HP 35s calculator. I do not have Microsoft *Excel* on my computer, so a spreadsheet to perform the calculations did not seem like an inexpensive option.

The laboratory-grade RF impedance analyzers and VNAs have in common one key feature — error correction. Since we amateur radio operators prefer using our own existing test equipment whenever possible, I designed a reflection-based bench-top method, or system, for making one-port complex impedance measurements incorporating a vector error-correction technique.¹ And I almost can’t believe how well it works!

In this article, I spell out the fundamental equations for performing complex impedance measurement with one-port error correction. My intent is to arm the reader with all of the equations and techniques that they will need, in addition to providing the specifics on the way that I implemented the calculations. Because the fundamental equations are not limited to use on any particular calculator or computer, I fully anticipate that

readers will work out endless variations on my method. After writing and submitting the article, I discovered that with Microsoft *Works* on my computer, I was able to program the equations into a spreadsheet, and then save that file in *Excel* format. The *Excel* spreadsheet file is available for download from the ARRL *QEX* Web site.²

A Simple Idea

During an encounter with a new RF measurement problem, I developed a new way to utilize or augment my old test equipment. Like most amateurs, I own simple test equipment: a two-channel analog oscilloscope for measurements, an RF signal generator to generate continuous sine waves, a junk box brimming with electronic parts,

and a soldering iron for sticking things together. After some research, I surmised that a system comprising my existing bench-top test equipment, a bidirectional coupler, some calibration loads, and a programmable calculator, could accurately measure the complex load impedance of a device under test (DUT) at a test frequency of interest (Figure 1).

The process is to first generate a stable reference RF signal with a 50 Ω RF signal generator, then drive the signal through a coupler and remote DUT test cable to three different calibration loads (SOLs — more on these, later), and measure the three pairs of transmitted (forward traveling) and reflected (reverse traveling) voltage vectors from the coupler.³ A calculator program will use the

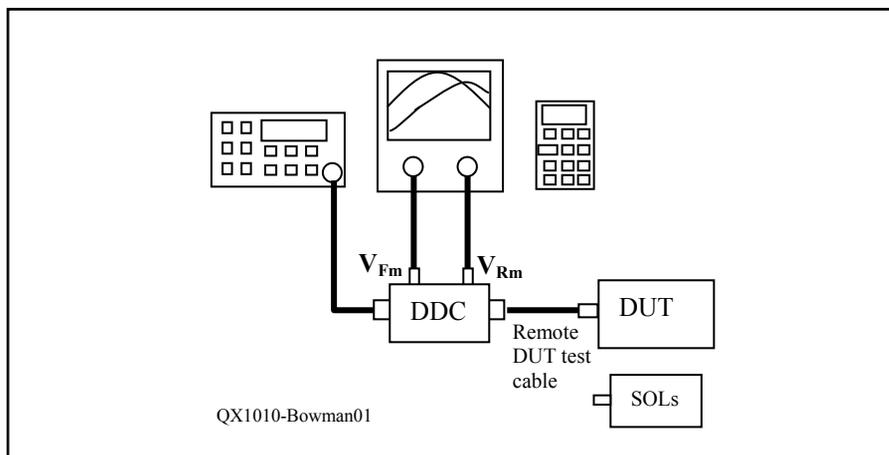


Figure 1 — Initial configuration.

¹Notes appear on page 15.

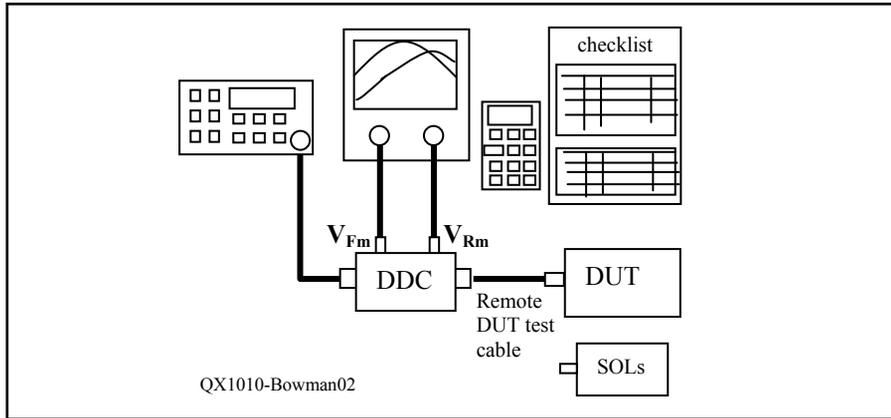


Figure 2 — Final configuration with a checklist.

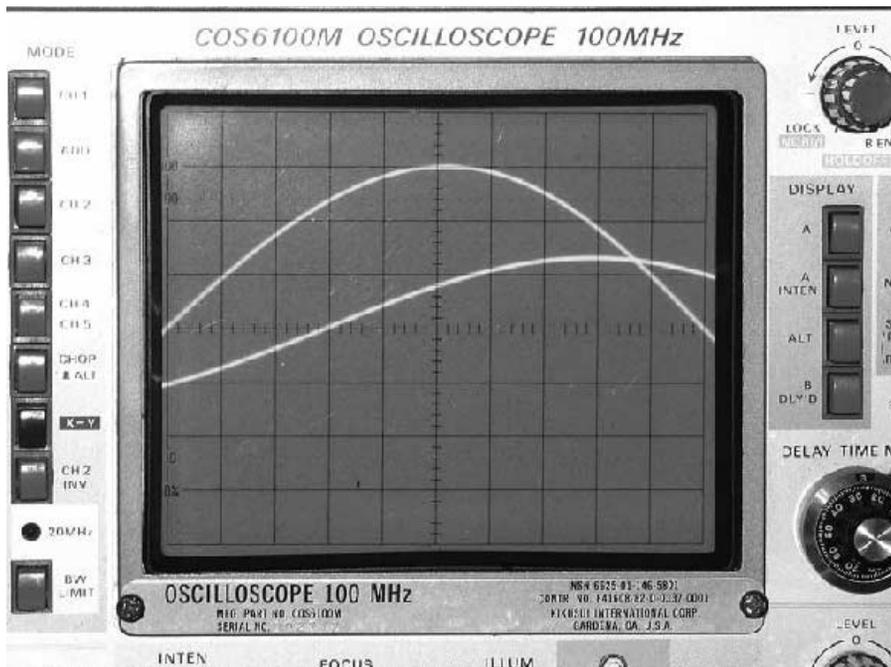


Figure 3 — Typical display of two vector voltages as they may appear during a calibration or a DUT measurement, with both voltages vertically centered on the screen, and one voltage designated as the reference.

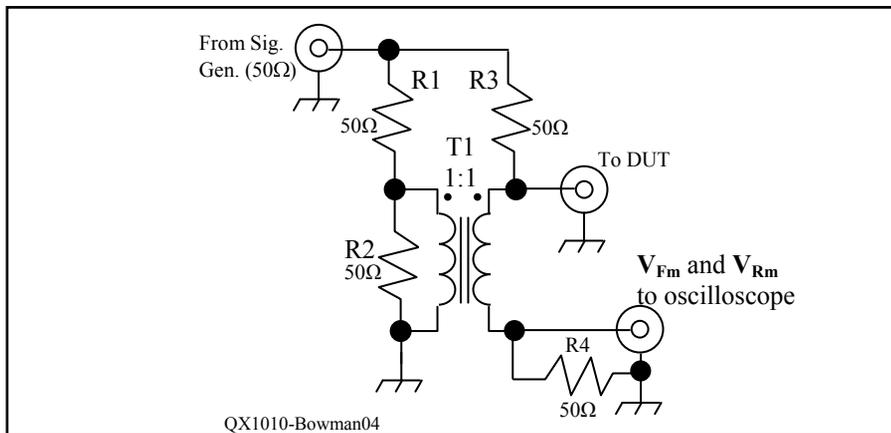


Figure 4 — A schematic diagram of a return loss bridge (RLB). The forward and reflected voltages aren't available simultaneously. (See Note 4.) This version has an on-board 50 Ω termination (R4) at its detector port, but the termination may instead be located at the oscilloscope input.

three pairs of calibration voltage vectors to generate three complex error vector terms that correct the magnitude and phase errors contributed by the coupler, oscilloscope, connectors, and test cables.

Next, voltage vector measurements are taken from the coupler while connected to the DUT through the remote test cable. Lastly, the calibration and DUT voltage vector measurements are processed by an error-correcting impedance measurement program, which calculates the corrected complex load impedance. The oscilloscope and coupler function together as a crude vector voltmeter to measure the magnitude and phase of the coupled forward (V_{Fm}) and reflected (V_{Rm}) voltage vectors from the coupler. The calculator program processes all of the measured (uncorrected) voltage vectors into system calibration data, and ultimately solves equations that yield the DUT's error-corrected complex load impedance. Validation tests confirmed that such a one-port impedance measurement system with a simple vector error-correction method is effective at high frequencies (HF). Eventually, I saw the merit of adding a checklist to log data and serve as a guide during the measurements (Figure 2).

In the bench-top impedance measurement system, two RF voltage sine waves, or voltage vectors, are simultaneously displayed on an analog oscilloscope screen, separated in phase from each other (Figure 3). Each voltage vector "X" has a magnitude V_x , and a phase angle θ_x relative to some reference voltage vector. Each voltage vector is actually an RF voltage sine wave whose magnitude and phase components can be expressed in polar notation as $V_x \angle \theta_x$, or more concisely in bold print as V_x . In Figure 3, the oscilloscope time base is adjusted to display exactly 180° of a reference voltage vector across the horizontal axis. Configured this way, the horizontal axis has a scale of 18° per major division, and relative phase angles can be read to within about 1.8°. Figure 3 also shows a lower amplitude voltage vector lagging the reference voltage vector by about 52.2°. In polar form, the lower amplitude signal can be written as $2.6 \angle -52.2^\circ$ and the reference signal can be written as $6 \angle 0^\circ$.

Using the oscilloscope phase measurement method just described, the capability to make accurate phase angle measurements is limited by the fastest sweep speed of the oscilloscope time base. Phase measurements with my 100 MHz oscilloscope were possible up to about 28 MHz. Higher bandwidth oscilloscopes would allow phase measurements at proportionally higher test frequencies, with the maximum performance being limited by the shared bandwidth of the oscilloscope and the coupler.

Developing the Simple Idea

When first researching reflection-based measurement techniques, I read information about return loss bridges (RLBs) and couplers. One reference stated that either a RLB or a coupler can be used in making the reflection-based voltage vector measurements from which vector information can be calculated, such as a DUT's load voltage reflection coefficient Γ_L and complex load impedance Z_L .⁴ The theory and methods of the RLB and coupler are well-documented. Vector error-correction methods, on the other hand, were a different story. Eventually, I worked everything out, but there were some twists.

At first glance, an RLB looked to be the simpler circuit for this system. Most RLBs consist of a two-leg resistive bridge and an RF output balun (Figure 4). But after extensive experiments using an oscilloscope and RLB for making both the magnitude and relative phase measurements, the bidirectional coupler appeared to be the more direct approach (Figure 5). A coupler could simultaneously provide the coupled forward and reflected voltages at its coupled ports — precisely the arrangement needed to measure the voltage reflection coefficient Γ_L of the DUT using an oscilloscope, and something that an RLB can't directly produce due to its circuit topology.⁵ Consequently, the bidirectional coupler was selected as the simplest circuit for use in measuring the coupled forward (V_{Fm}) and reflected (V_{Rm}) voltage vectors.

I breadboarded a 20 dB coupler (Figure 6) following the schematic from Figure 5, but without the Faraday shield. The power levels used during tests were those that my RF signal generator was capable of, up to +13 dBm. So I expected that coupled output signal levels would be roughly in the -7 dBm to -40 dBm range, or about 100 mV_{rms} to 2.2 mV_{rms} across 50Ω . I had planned to use only my oscilloscope to measure the coupled voltage magnitudes and phase, provided that the signal magnitudes were high enough for good resolution. My analog oscilloscope's vertical gain was limited to 1 mV/division, but initial experiments confirmed that it was enough.

In the local RF library, I found a calibration method that applies three calibration standards to a system's remote DUT test cable: a Short, an Open, and a matched Load (the SOL standards).⁶ I breadboarded mine using BNC connectors (Figures 7 and 8). The SOL standards are integral to the one-port calibration of this reflection-based system. Impedance measurements begin as a two-phase process: an initial SOL calibration measurement, and then the DUT measurement. The calibration measurement quantifies the main systematic magnitude

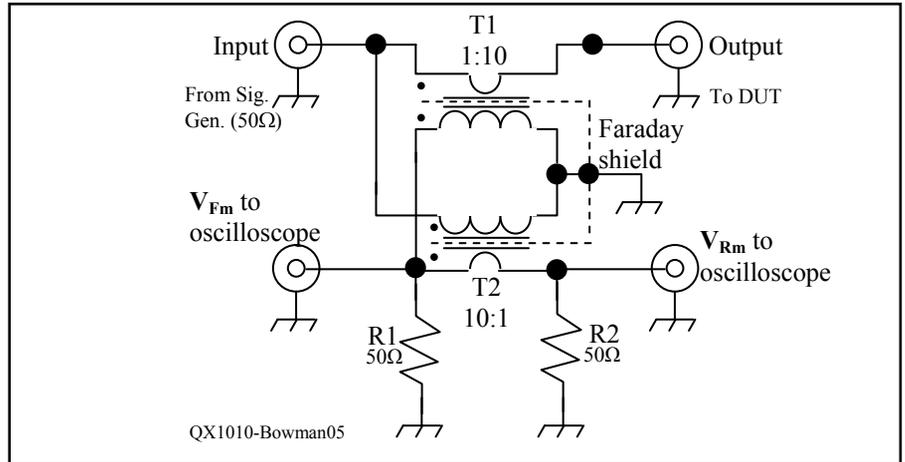


Figure 5 — A bidirectional coupler. The measured forward and reflected voltages are available simultaneously. (See Note 3.) This version has on-board 50Ω terminations (R1, R2) at the coupled ports, but the terminations may instead be located at the oscilloscope inputs.

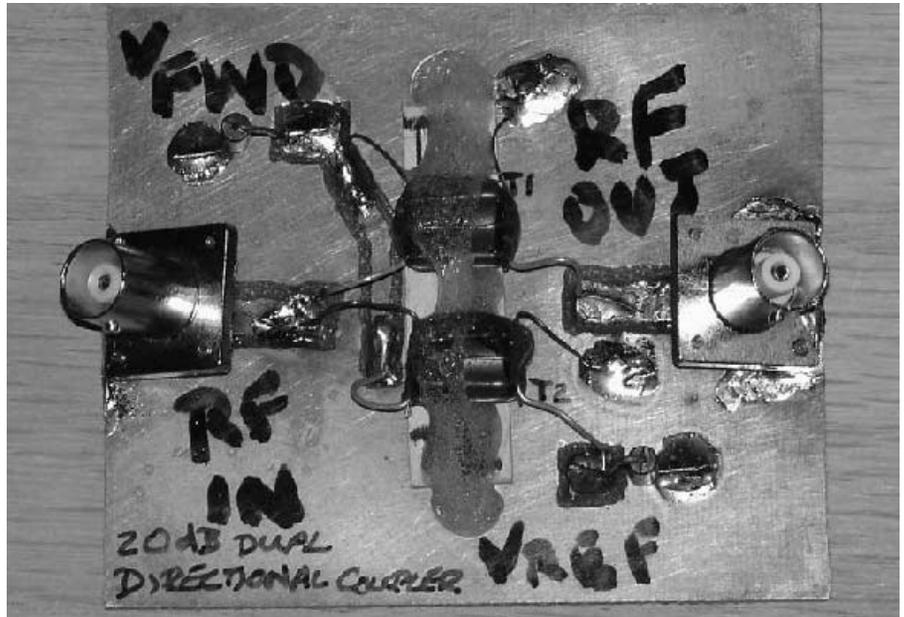


Figure 6 — The coupler breadboard. Made with type FB-43-6301 ferrite beads and no. 30 AWG solid wire, it's suitable for MF and HF use. Despite its rough construction, error correction enabled good results.



Figure 7 — The breadboarded SOL calibration "standards." I tried different ways of making the loads, so there are extras just for the sake of experiment.

and phase errors that affect the accuracy of the DUT load impedance measurement. In a coupler-based measurement system, the voltage vectors appearing at the coupled ports are plagued with errors that are contributed by all components of the system. These vector measurements are commonly referred to as “uncorrected.” During the SOL calibration, three pairs of coupled voltage vectors (forward and reflected voltages) are measured and recorded. These pairs of measured calibration voltage vectors contain the information from which we can determine three systematic error vector terms that can be used to correct the three main errors of the system.

For most impedance measurement systems, the calibration and correction processes are handled by either a microcontroller or a PC. But for this method, a programmable

calculator (Figure 9) runs “D,” a program that processes the calibration and DUT voltage measurements (Table 1A). Three pairs of SOL calibration voltage vectors are stored in polar form (r, θ) in the calculator, along with the pair of DUT voltage measurements. Then the program calculates the calibration information (the three complex error vector

terms), the error-corrected DUT load reflection coefficient, and other corrected data. I took the time to derive the three basic error vector terms and the error-correction algorithm by constructing and analyzing a signal flow graph (Figure 17) of the impedance measurement system.⁷ It was challenging, to say the least.⁸ Believe me, programming it

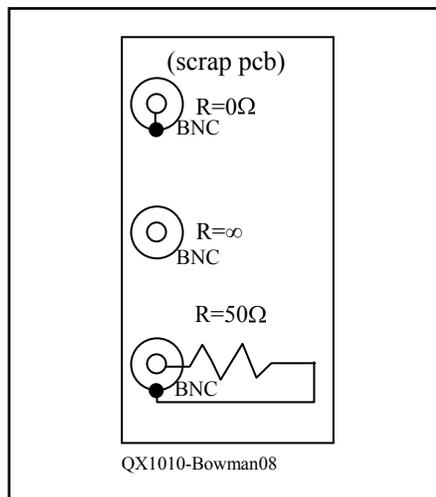


Figure 8 — The basic SOL calibration “standards” on BNCs. Homebrewed loads such as these are quite adequate for use as calibration standards at HF.

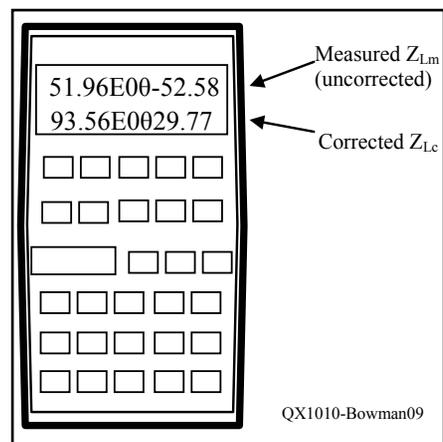


Figure 9 — A typical programmable calculator and its display of DUT complex impedances. This display is in polar format, with magnitude to the left of the “0” symbol, and phase to its right.

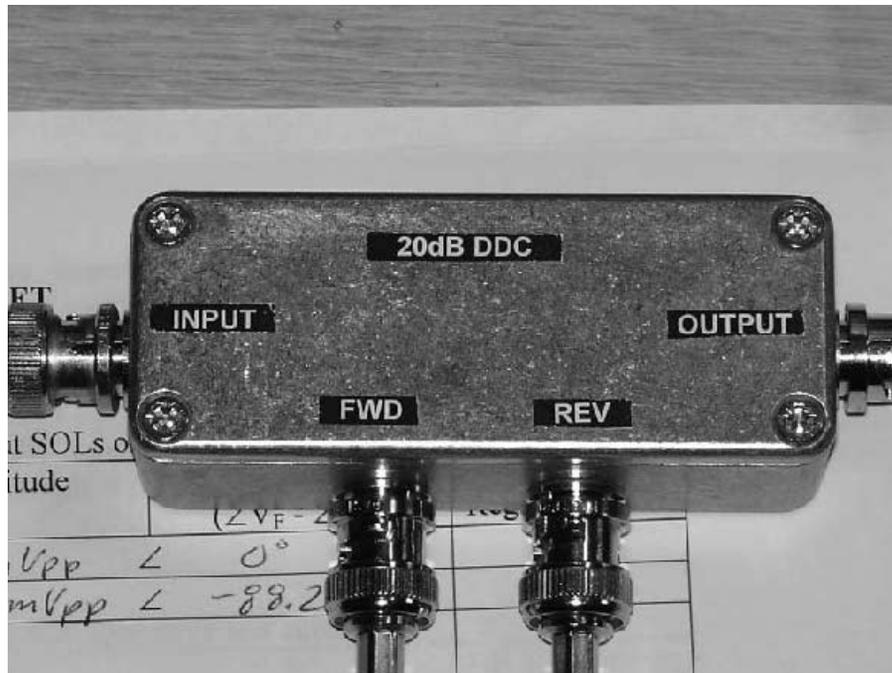


Figure 10 — The working bidirectional coupler. Built for the comparison tests, this device (Faraday shields and all) was still plagued with errors. With error correction, the system delivered good results.



Figure 11 — The bench-top system. This is all there is to it: a coupler, a signal generator, an oscilloscope, a DUT test cable, a checklist, the SOLs, and a programmable calculator.

into the calculator was much simpler.

With this method, there was the obvious need for consistency in hardware warm up, hardware settings, calibration, and data recording. However, a great feature of error correction is that all of the coaxial cable lengths are non-critical. In fact, it's unnecessary to have matched lengths of cable between the oscilloscope and the coupler. And although the breadboard worked well in preliminary tests, I built another bidirectional coupler (Figure 10) that included the Faraday shield (Figure 5) and an aluminum enclosure. Its measured directivity was an unspectacular 27 dB, but when applied in conjunction with the vector error-correction method, the system results were very good.

The voltage vector measurements were made with a 100 MHz bandwidth analog oscilloscope whose display was sharp and its triggering stable. Nevertheless, the impedance measurement method's weakest links were the oscilloscope readings made during SOL calibration and DUT impedance measurements. An RF vector voltmeter or a digital oscilloscope would have improved the readings, but I don't own either. The tradeoff was simplicity and availability.

The use of a checklist and/or data table for calibration and DUT measurement became

highly desirable. For example, a table of written calibration and test data (Table 2A) was very useful for troubleshooting the system after getting seemingly impossible impedance results. In another instance, it eliminated the need to recalibrate after I had accidentally deleted the calculator's stored calibration data. Using a checklist, a complete SOL calibration cycle (from measurement to calibration data entry) only took about four minutes. A typical DUT measurement was turned around in about one minute.

An indispensable piece of the system was the programmable calculator, one that was capable of complex math and storage operations. Otherwise, the storage and programming of complex numbers and their instructions tended to be overwhelming. For example, the programmable calculator that was used in this system was my work calculator (an HP 35s), which cost about sixty dollars back in 2007. All told, the bench-top impedance measurement system was very easily assembled (Figure 11).

Program "D": The Equations for Error Correction

The following equations are solved by the program "D." They were derived from my

analysis of the signal flow graph of the error adapter model (Figure 17). The equations appear to be simple, but they present a daunting task to calculators lacking complex number functions and storage. Programmable calculators capable of complex number operations and storage are both common and inexpensive.

$$\Gamma_{Lc} = \frac{\Gamma_{Lm} - E_D}{E_T + E_S \cdot (\Gamma_{Lm} - E_D)}$$

where Γ_{Lc} is the corrected load reflection coefficient of the DUT.

$$Z_{Lc} = Z_0 \cdot \frac{(1 + \Gamma_{Lc})}{(1 - \Gamma_{Lc})}$$

where Z_{Lc} is the corrected DUT load impedance.

$$Z_{Lm} = Z_0 \cdot \frac{(1 + \Gamma_{Lm})}{(1 - \Gamma_{Lm})}$$

where Z_{Lm} is the measured DUT load impedance.

$$VSWR_c = \frac{(1 + |\Gamma_{Lc}|)}{(1 - |\Gamma_{Lc}|)}$$

where $VSWR_c$ is the corrected DUT standing wave ratio, or SWR_c for more brevity.

Table 1A
DUT Impedance Measurement Program "D"

Program line #	INSTR						
D001	LBL D	D026	-	D051	RCL J	D076	1
D002	RCL H	D027	÷	D052	+	D077	-
D003	RCL G	D028	STO I	D053	÷	D078	RCL O
D004	÷	D029	RCL Y	D054	STO N	D079	1
D005	STO M	D030	RCL Z	D055	1	D080	+
D006	RCL B	D031	-	D056	+	D081	÷
D007	RCL A	D032	2	D057	50	D082	LOG
D008	÷	D033	x	D058	x	D083	20
D009	STO X	D034	RCL X	D059	RCL N	D084	X
D010	RCL D	D035	RCL Z	D060	+/-	D085	+/-
D011	RCL C	D036	-	D061	1	D086	STO P
D012	÷	D037	x	D062	+	D087	RCL G
D013	STO Y	D038	RCL X	D063	÷	D088	RCL H
D014	RCL F	D039	RCL Y	D064	STO L	D089	+
D015	RCL E	D040	-	D065	RCL N	D090	RCL G
D016	÷	D041	÷	D066	ABS	D091	RCL H
D017	STO Z	D042	STO J	D067	1	D092	-
D018	2	D043	RCL M	D068	+	D093	÷
D019	x	D044	RCL Z	D069	RCL N	D094	50
D020	RCL X	D045	-	D070	ABS	D095	x
D021	RCL Y	D046	RCL M	D071	+/-	D096	STO K
D022	+	D047	RCL Z	D072	1	D097	RCL L
D023	-	D048	-	D073	+	D098	RTN
D024	RCL X	D049	RCL I	D074	÷		
D025	RCL Y	D050	x	D075	STO O		

Table 1B
Example of an HP 35s Calculator Display

51.96E0 0-52.58 First Line: Uncorrected DUT Impedance.
93.56E0 029.77 Second Line: Corrected DUT Impedance.

$$RL(\text{dB})_c = -20 \cdot \log_{10} |\Gamma_{Lc}|$$

where $RL(\text{dB})_c$ is the corrected DUT return loss in dB

$$\Gamma_{Lm} = \frac{V_{Rm}}{V_{Fm}}$$

where Γ_{Lm} is the measured (uncorrected) load voltage reflection coefficient of the DUT, and V_{Rm} and V_{Fm} are the measured reflected and forward voltage vectors of the DUT.

$$E_D = \Gamma_{loadm}$$

where E_D is the directivity error vector term; one of three systematic error terms.

$$E_S = \frac{2 \cdot \Gamma_{loadm} - (\Gamma_{shortm} + \Gamma_{openm})}{(\Gamma_{shortm} - \Gamma_{openm})}$$

where E_S is the source mismatch error vector term; one of three systematic error terms.

$$E_T = \frac{2 \cdot (\Gamma_{openm} - \Gamma_{loadm}) \cdot (\Gamma_{shortm} - \Gamma_{loadm})}{(\Gamma_{shortm} - \Gamma_{openm})}$$

where E_T is the reflection tracking error vector term; one of three systematic error terms.

$$\Gamma_{shortm} = \frac{V_{Rshortm}}{V_{Fshortm}}$$

where Γ_{shortm} is the measured short circuit reflection coefficient.

$$\Gamma_{openm} = \frac{V_{Ropenm}}{V_{Fopenm}}$$

where Γ_{openm} is the measured open circuit reflection coefficient.

$$\Gamma_{loadm} = \frac{V_{Rloadm}}{V_{Floadm}}$$

where Γ_{loadm} is the measured 50 Ω load reflection coefficient. It is also equivalent to the complex directivity error vector term, E_D . Z_0 is the characteristic (50 Ω system reference) impedance.

Program "D": The Pseudocode

Prior to running program "D" (Table 1A), record the three pairs of measured SOL calibration voltage vectors and the pair of measured DUT voltage vectors in a table or checklist (Table 2A). Such written records are useful for troubleshooting. The three pairs of SOL voltage vector measurements are then stored (in polar form) into their memory locations in the calculator, as are the pair of measured DUT voltage vectors. Program "D" is now ready to run.

Program "D" performs the following:

1) From the measured forward and reflected voltage vectors of the DUT (V_{Fm}

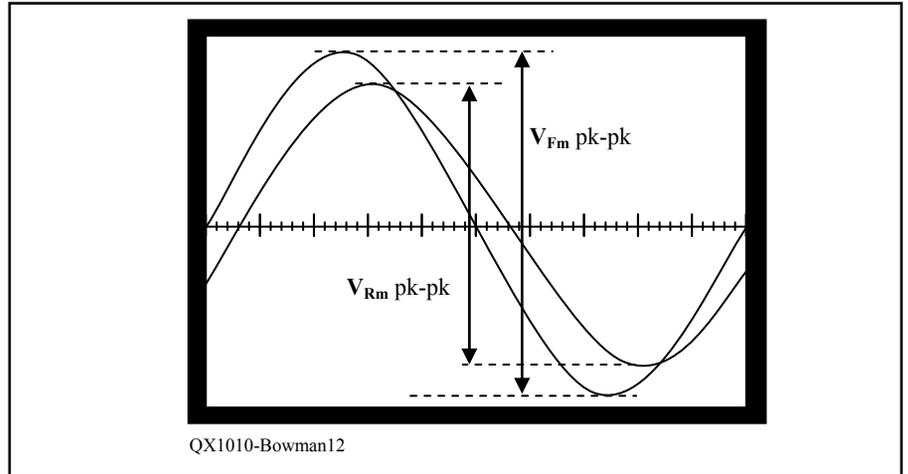


Figure 12 — Magnitude Measurement Technique. Prior to calibration, adjust the vertical gain of both the V_{Fm} and the V_{Rm} channels to get the best resolution while driving the SOL open. Then do SOL calibration, recording the pk-pk magnitude of each pair of voltage vectors.

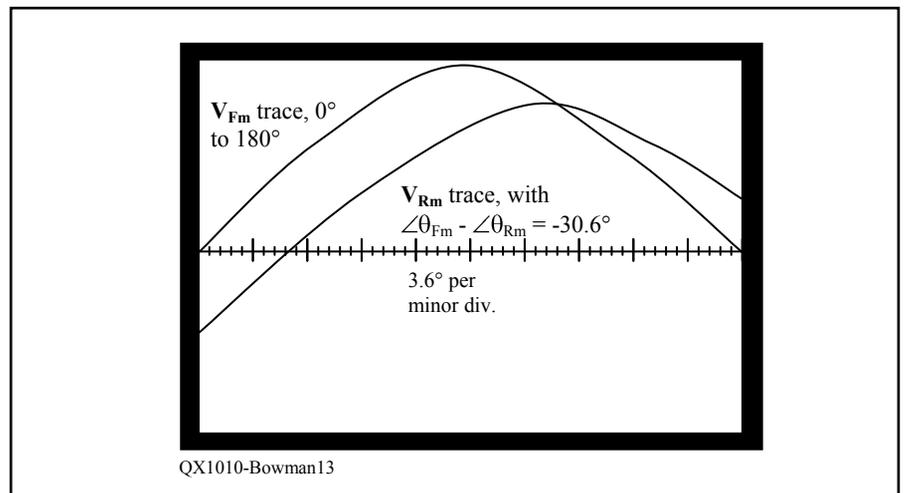


Figure 13 — Phase Measurement Technique. Vertically center the V_{Fm} and V_{Rm} signals, adjust horizontal sweep so that exactly 180° of the V_{Fm} signal is displayed, then measure their phase difference. This phase measurement technique has about 1.8° of resolution.

and V_{Rm}), calculate and store the measured complex load voltage reflection coefficient (Γ_{Lm}) of the DUT.

2) From the measured short circuit forward and reflected voltages ($V_{Fshortm}$ and $V_{Rshortm}$), calculate and store the measured complex reflection coefficient (Γ_{shortm}) of the short circuit calibration standard.

3) From the measured open circuit forward and reflected voltages (V_{Fopenm} and V_{Ropenm}), calculate and store the measured reflection coefficient (Γ_{openm}) of the open circuit calibration standard.

4) From the measured 50 Ω load forward and reflected voltages (V_{Floadm} and V_{Rloadm}), calculate and store the measured reflection coefficient (Γ_{loadm}) of the 50 Ω calibration standard. This is also the directivity error vector term E_D .

5) From the measured reflection coef-

ficients of the short and open (Γ_{shortm} and Γ_{openm}), calculate and store the source mismatch error vector term E_S .

6) From the measured reflection coefficients of the short, open, and 50 Ω load (Γ_{shortm} and Γ_{openm} and Γ_{loadm}), calculate the reflection tracking error vector term E_T .

7) From the measured load voltage reflection coefficient (Γ_{Lm}) of the DUT and the directivity error vector term (E_D) and the source mismatch error vector term (E_S) and the reflection tracking error vector term (E_T), calculate and store the corrected load reflection coefficient Γ_{Lc} of the DUT.

8) From the corrected reflection coefficient Γ_{Lc} of the DUT, calculate and store the corrected DUT complex impedance Z_{Lc} .

9) From the corrected load reflection coefficient of the DUT (Γ_{Lc}), calculate and store the corrected SWR (SWR_c).

Table 2A

DUT Impedance Measurement Checklist

Input Table

Step 1: Calibration Measurements (put SOLs on DUT test cable)

Short Circuit Cal	Vector Voltage	Magnitude, pk-pk	Test PWR: Phase Delta, degrees ($\angle\theta_{Fm} - \angle\theta_{Rm}$)	Test Freq: HP 35s Storage Register
	$V_{Fshortm}$		\angle	A
	$V_{Rshortm}$		\angle	B
Open Circuit Cal	V_{Fopenm}		\angle	C
	V_{Ropenm}		\angle	D
50 Ω Load Cal	V_{Floadm}		\angle	E
	V_{Rloadm}		\angle	F

Step 2: DUT Impedance Measurement (Put DUT on DUT Test Cable)

DUT Impedance Measurement	Vector Voltage	Magnitude, pk-pk	Phase Delta, degrees ($\angle\theta_{Fm} - \angle\theta_{Rm}$)	HP 35s Storage Register
	V_{Fm}		\angle	G
	V_{Rm}		\angle	H

Output Table

Step 3: Executing "D" processes the inputs and delivers the following outputs

Error-Correct Measurements	Outputs	Description	HP 35s Storage Register
	E_S	The source mismatch error term	I
	E_T	The reflection tracking error term	J
	Z_{Lm}	Measured (uncorrected) DUT impedance	K
	Z_{Lc}	Corrected DUT impedance	L
	Γ_{Lm}	Measured reflection coefficient of DUT	M
	Γ_{Lc}	Corrected reflection coefficient of DUT	N
	SWR_c	Corrected SWR	O
	RL (dB)_c	Corrected Return Loss in dB	P
	Γ_{shortm}	Measured reflection coefficient of short	X
	Γ_{openm}	Measured reflection coefficient of open	Y
	$\Gamma_{loadm} = E_D$	Measured reflection coefficient of a matched load = the directivity error term	Z

Table 2B

Displayed output data

\angle	Uncorrected DUT Impedance.
\angle	Corrected DUT Impedance.

10) From the corrected SWR, calculate and store the corrected Return Loss (RL(dB)_c).

11) From the measured forward and reflected voltages of the DUT (V_{Fm} and V_{Rm}), calculate and store the measured DUT impedance Z_{Lm} .

12) Display the corrected and the uncorrected values of the DUT impedance (Z_{Lc} and Z_{Lm}) in polar form (r, θ).

Program "D": The Instructions

The instructions (Hewlett-Packard HP 35s) for the error-correcting DUT impedance measurement program "D" are in Table 1A. The voltage vector measurements from the SOL calibration and the one-port DUT load are read from the oscilloscope and entered in calculator polar form (r, θ) into the storage registers. The program generates the corrected DUT impedance from these measured inputs.

The program does not prompt for inputs. All inputs are entered directly into the HP 35s memory storage registers A through H prior to execution of the program. All outputs are

stored in registers I through P and in X, Y, and Z. They can be recalled for display. The error-corrected DUT impedance and measured DUT impedance are both automatically displayed upon program termination.

After XEQing "D," the first (top) line in the display is the measured (uncorrected) value of DUT impedance, the second (bottom) line in the display is the corrected value of DUT impedance.

Table 2A can function not only as a test record, but as a useful checklist. Table 2B displays the outputs after XEQing "D."

Steps and Techniques for the SOL Calibration and DUT Impedance Measurement

With the open SOL standard on the remote DUT test cable, adjust the generator power and the oscilloscope vertical amplifier scale settings to give the best resolution (both vertical settings will be the same scale). From now on, *do not change the vertical amplifier or generator settings.*

1) For the SOL calibration measurements,

connect one at a time to the remote DUT test cable and measure the pair of forward and reflected voltages ($V_{Fshortm}$ and $V_{Rshortm}$, V_{Fopenm} and V_{Ropenm} , and so on) for each load. Start by vertically centering both forward and reflected voltages on the screen (Figure 12). Adjust the time base and horizontal control so that at least one cycle of the voltage is visible. Measure the peak-to-peak magnitude and record it in the checklist (Table 2A).

2) For the SOL phase measurements, adjust the time base and its calibration knob to show exactly 180° of V_{Fm} from end to end of the horizontal grid (Figure 13). This makes V_{Fm} the reference vector, always with a phase of zero. For each SOL load, measure the phase difference between V_{Fm} and V_{Rm} . Record phase difference ($\angle\theta_{Fm} - \angle\theta_{Rm}$) in the checklist. This completes the calibration.

3) Now connect the DUT to the remote test cable and make the magnitude and phase measurements of its voltage vectors using the same techniques described in steps 1 and 2 above. Record the measurements in the checklist (Table 2A).

4) Store all recorded SOL calibration and DUT measurements from Table 2A in their calculator storage registers. Execute “D,” the DUT impedance measurement program. When done, the corrected and measured values of the DUT impedance appear on the calculator screen (Figure 9). Now that the system is calibrated, further DUT measurements are possible without recalibration, unless the test system hardware, or the oscilloscope vertical amplifier settings, or the signal generator settings are changed.

Note: The peak-to-peak voltage units of measurement (UOM) allow greater measurement resolution. If peak or rms UOM are preferred, then that UOM *must be used consistently throughout* the data entry process. Program “D” works with any voltage UOM, but only if it is the only UOM being used.

Why Error-Correct?

Consider just two of the system components in this bench-top method: the coupler and the remote DUT test cable. Both contribute significant magnitude and phase errors that can be corrected. The coupler’s magnitude and phase errors are interrelated errors, due mostly to transformer leakage and winding asymmetry. Such errors reduce the coupler’s directivity. Directivity, the ability to differentiate between the forward and reflected waves, is very important for making impedance measurements. The DUT test cable causes a relative phase shift between the forward and reflected waves, which can be the major source of phase error in the system, depending on the cable’s wavelength (Figure 14).

The uncorrected phase errors in V_{Fm} and V_{Rm} are due in part to the coupler’s directivity acting out of phase vectorially with the actual forward V_{Fa} and reflected V_{Ra} voltage vectors. The worst case phase error possibility is when the error acts orthogonally to the actual vector (Figure 15). Additional, and possibly

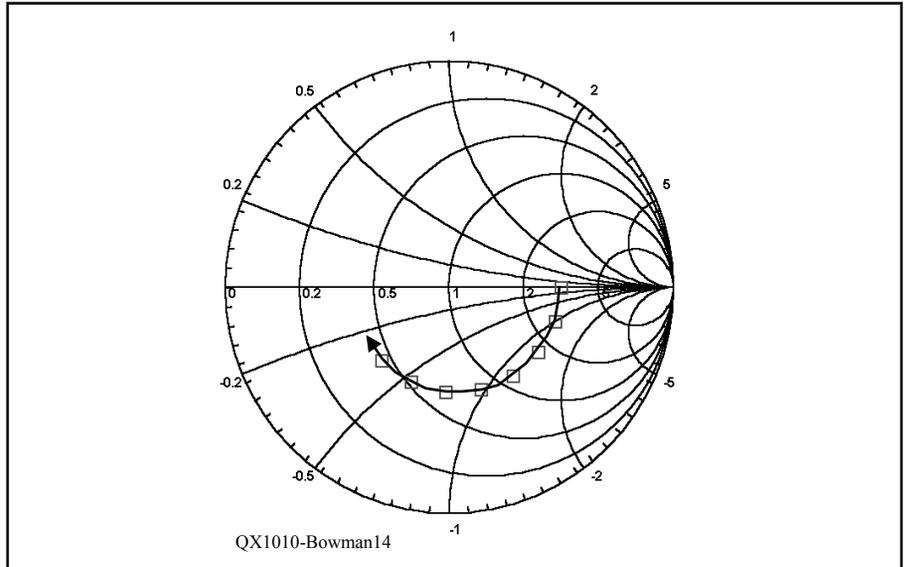


Figure 14 — How phase of the impedance shifts along an SWR circle with increases in DUT cable length.

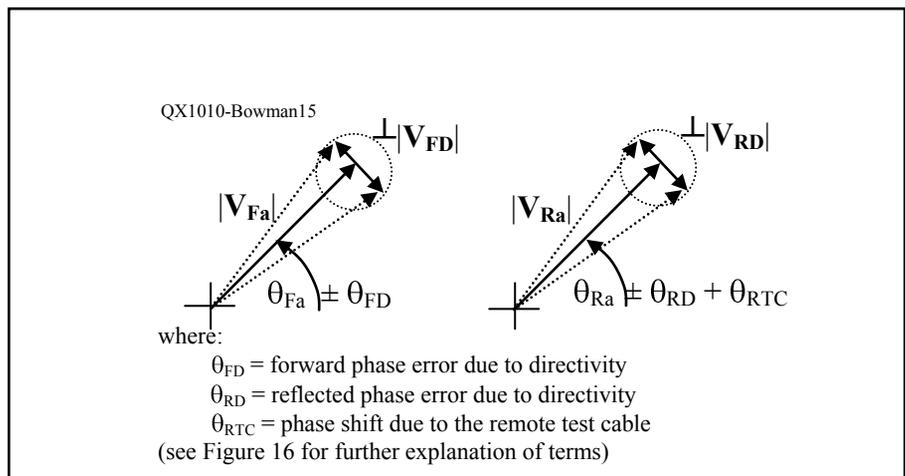


Figure 15 — Worst case phase error possibilities due to coupler directivity.

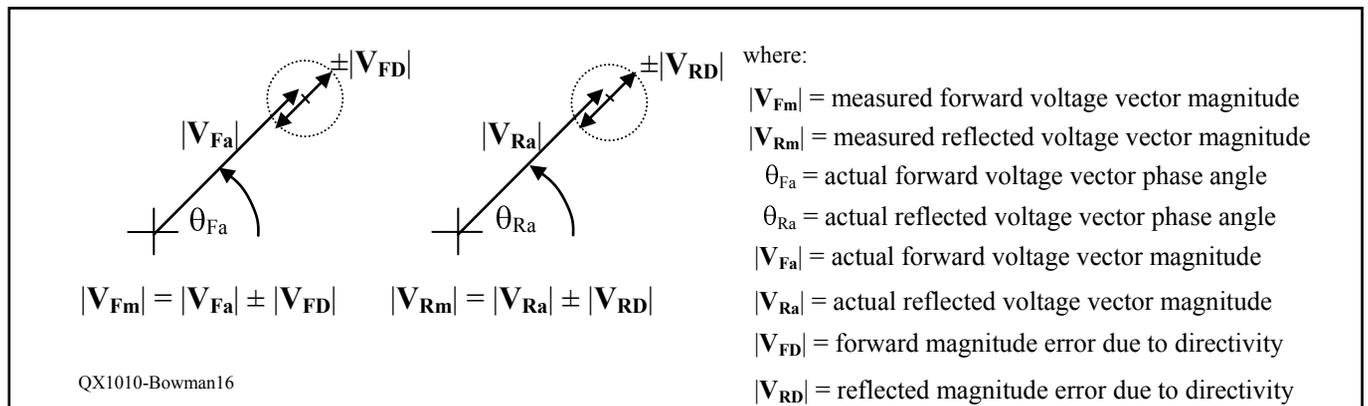


Figure 16 — Worst case magnitude error possibilities due to coupler directivity.

significant, phase error is contributed by the remote test cable between the DUT and coupler.

The uncorrected magnitude errors intrinsic to V_{Fm} and V_{Rm} are due mainly to the coupler directivity error adding or subtracting vectorially with the actual forward V_{Fa} and reverse V_{Ra} voltage vectors. The worst case possibility for magnitude error is when the error adds or subtracts in phase with the actual vector (Figure 16), leading to a magnitude error in the reflection coefficient.⁹ Additional errors in the magnitude and phase are contributed by the remote DUT test cable, other interconnecting cables, connectors, adapters, and even the oscilloscope. All of these errors need to be corrected, and they will be with the calculator running the error-correcting DUT impedance measurement program.

How the Errors were Modeled and Corrected

The error-correction algorithm was developed from equations that describe the measurement system, with all of its test fixture errors, as a two-port network with voltage waves flowing through it. The coupler actually makes the measurement system a four-port network. But, since the measured coupled voltages are images of the voltage waves flowing through the coupler from input to output, and since vector error correction will be performed, only the system's error voltage vectors from input to output need to be modeled and analyzed.

The DUT is a one-port network that is connected to the measurement system. The voltage signals that we desire to measure are the actual voltage waves, or vectors, that flow at the reference plane between the measurement system's remote DUT test cable and the DUT input port. For the purpose of modeling and correcting the errors in the non-

ideal measurement system, our vectors of interest are the measured forward (incident) traveling waves, the reverse (reflected) traveling waves, and the measurement system's error vector terms, i.e., the systematic errors. The error vectors are caused by the intrinsic features and imperfections of the test fixtures and settings. They transform the actual voltage waves at the reference plane into the error-plagued measured voltage waves.

A signal flow graph is one way to model the voltage and error vectors that flow and exist within the network, in other words the measurement system and the DUT connected to it. Signal flow graphs that model the undesired error vectors are commonly referred to as error adapter models. The error adapter model is a numerical model of the errors in the physical measurement system that transform the actual voltage vectors at the reference plane into the measured voltage vectors of the coupler. From the error adapter model of the system comes closed-form expressions (linear equations) that contain terms for the coupler measured voltage vectors, systematic error vectors, the measured DUT reflection coefficient, and the corrected DUT reflection coefficient. These equations, and others, are programmed into the calculator.

The signal flow graph (Figure 17) includes signals contributed by the signal source, the oscilloscope, the coupler, the SOL standards, the test cables, and the DUT. The coupler is physically separate from the DUT, but it samples, through the remote DUT test cable, the actual voltage vectors V_{Fa} and V_{Ra} that exist at the reference plane. The remote DUT test cable, the coupler, and other system components transform them into the measured voltage vectors, V_{Fm} and V_{Rm} .

The "reference plane" is the plane of separation between a measurement system and an actual DUT. The information on the measurement system side of the reference plane

contains systematic errors that distort, or transform, the actual information that exists on the DUT side of the plane.¹⁰ Because of the systematic errors in the measurement system (quantified during the calibration as E_D , E_T , and E_S and key to the Error Adapter Model), and the coupler's coupling factor, the measured voltage vectors differ significantly from the actual voltage vectors at the DUT. Calculating the DUT impedance from the measured voltage vectors at the coupler would not yield the actual DUT impedance Z_{La} . The measured coupler voltage vectors, V_{Fm} and V_{Rm} , can calculate only the measured (uncorrected) load voltage reflection coefficient Γ_{Lm} , which in turn can yield only the measured load impedance Z_{Lm} , which has errors. Therefore, to determine the actual DUT voltage reflection coefficient Γ_{La} , the standard practice in complex impedance measurement is to first perform a calibration step.

The SOL calibration quantifies the major systematic errors that exist on the measurement system side of the reference plane, so that the errors can be removed from the DUT impedance measurement later on to yield the corrected DUT load reflection coefficient Γ_{Lc} and corrected DUT load impedance Z_{Lc} . The two phase process in complex impedance measurement is an acknowledgment of the physical difference between the coupler's measured voltage vectors, V_{Fm} and V_{Rm} , and the DUT's actual voltage vectors, V_{Fa} and V_{Ra} . With calibration and error correction, the corrected value of DUT impedance Z_{Lc} approaches the much needed actual DUT impedance Z_{La} .

The Error Adapter Model is a two-port model of the test fixture systematic errors that are between Z_{Lm} and Z_{La} . The network equations that are derived from this model can be solved for the error vector terms that are needed to correct the measured (uncor-

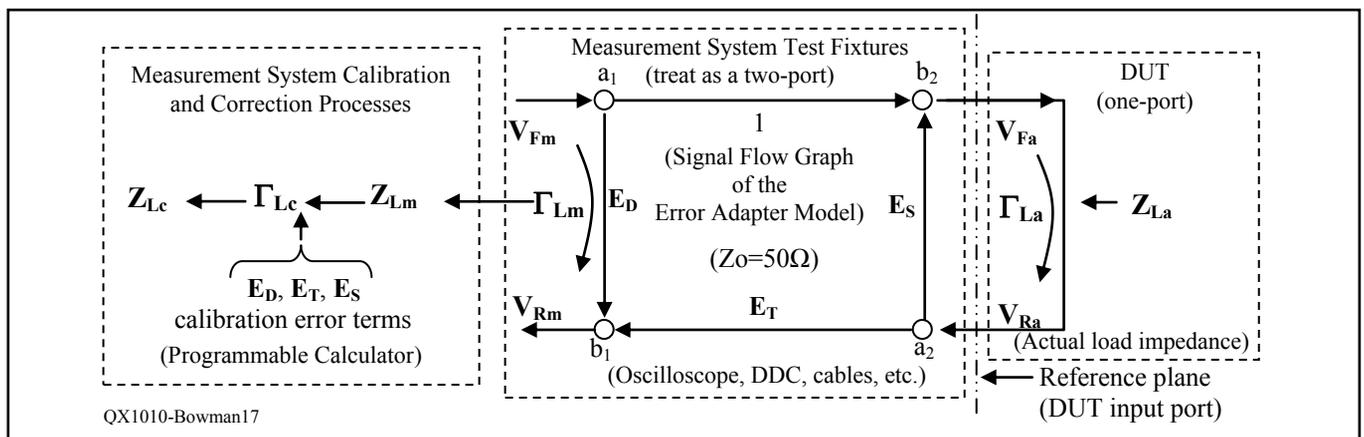


Figure 17 — The signal flow graph of the impedance measurement system.

rected) DUT reflection coefficient Γ_{Lm} , where:

Z_{La} is the actual DUT complex load impedance.

Z_{Lm} is the measured (uncorrected) DUT complex load impedance.

V_{Fa} is the actual forward voltage vector at the DUT.

V_{Ra} is the actual reflected voltage vector at the DUT.

V_{Fm} is the measured coupled forward voltage vector from the coupler.

V_{Rm} is the measured coupled reflected voltage vector from the coupler.

Z_{Lc} is the corrected DUT complex load impedance.

a1, a2 are the input voltage wave nodes of the Error Adapter Model.

b1, b2 are the output voltage wave nodes of the Error Adapter Model

Γ_{La} is the actual load voltage reflection coefficient of the DUT complex load impedance.

Γ_{Lm} is the measured load voltage reflection coefficient of the DUT complex load impedance.

Γ_{Lc} is the corrected load voltage reflection coefficient of the DUT complex load impedance.

E_D is the directivity error vector term; one of three systematic errors.

E_S is the source mismatch error vector term; one of three systematic errors.

E_T is the reflection tracking error vector term; one of three systematic errors.

Validation by Comparison

After all of the test equipment, calibration, and error-correction methods were built up and running, a simple comparison test was planned in order to estimate the overall system performance (Figure 18). A variety of complex impedance RF loads were made for tests at 14 and 28 MHz. The loads, when plotted on a Smith Chart, would lie upon circles of constant SWR. Impedance measurements that were made using the bench-top method were then compared to impedance measurements of the same loads made by a lab-grade VNA. The load magnitudes came from six different load resistances (5, 25, 33.3, 75, 100, and 500 Ω) mounted on BNC connectors in an aluminum project box (Figure 19). The load phases were created from combinations of three different lengths of RG58C/U coaxial cables (0.44, 0.88, and 1.35 meters). The load resistors set the SWR magnitude to either 1.5, 2, or 10, and the different lengths of coaxial cable created phase shifts when they were connected to the load resistors (Figure 20). The resistor values were selected to cause the coupler outputs to generate both high and low vector magnitude ratios (where errors in resolving the imped-

ance magnitudes are most apparent) of the measured V_{Fm} and V_{Rm} voltages. The load phasing cable lengths were chosen to evenly space eight impedances around a constant SWR circle on a Smith Chart.

Following a two-hour test equipment warm up, the exact experimental sequence was to first calibrate the system by applying

the SOL load standards directly to the remote DUT test cable. Calibration measurements were then made, recorded in a table, and entered into their memory locations. Next, a load resistor with a phasing cable was connected to the remote DUT test cable via an adapter, and its voltage vectors were measured and recorded in a table. Measurements



Figure 18 — Impedance tests being performed with careful logging and storage of measurements.

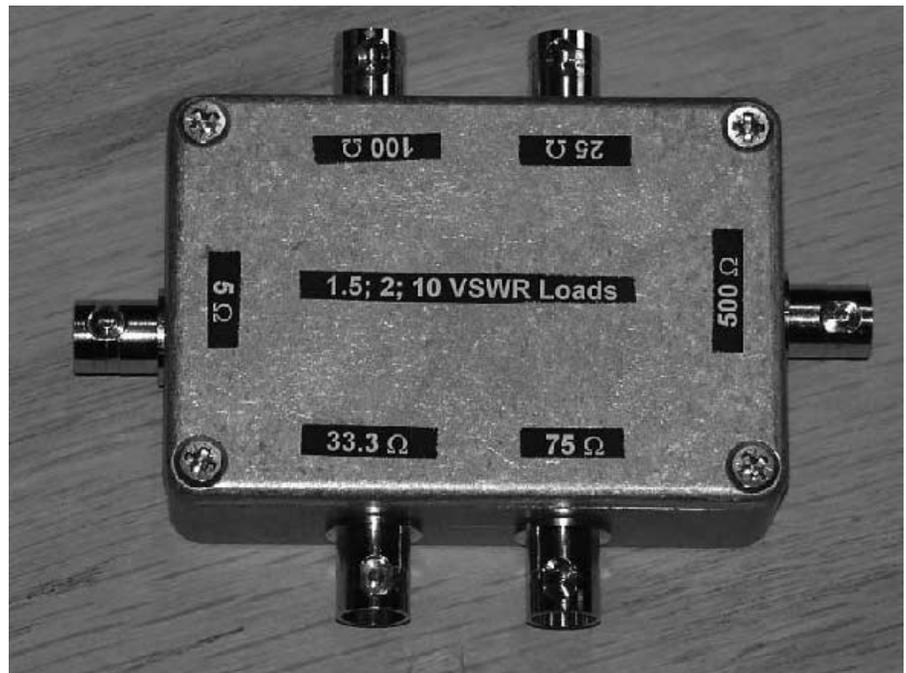


Figure 19 — The load test box. It has six different resistive loads that were phase shifted with transmission lines.

were repeated for each resistor and phasing cable combination, with the measured voltage vectors for each combination entered into the table.

Finally, the measured voltage vectors for each combination were processed by program "D," and the error-corrected impedance results were tabulated (Tables 3A, B and C and 4A, B, and C). All error-corrected load impedance results were transferred to a Smith Chart. Following this sequence, a lab-grade VNA measured the same resistor and phasing cable combinations and its results were compared to the bench-top method

(Tables 3A, B and C and 4A, B, and C, and Figure 21 A and B). The average errors and standard deviations indicate good agreement between the VNA and the bench-top method using simple three-term vector error correction.

Acknowledge Limits and Achieve Success

While this bench-top method is not state-of-the-art, the required hardware is simple and effective, and as revealed by actual test data, its performance is suitable for the

needs of most Amateur Radio operators. The method could even serve as the basis for a microcontroller one-port analyzer project. In order for the method to work, the test equipment must be well warmed up, the generator and oscilloscope amplitudes must be adjusted for the best resolution of the calibration measurements; the interconnecting cables, the remote DUT test cable, the SOL standards, and any RF adapters must be in good shape and used correctly; the calculator's DUT impedance measurement program "D" must have been loaded without error, and the calibration and DUT measurements

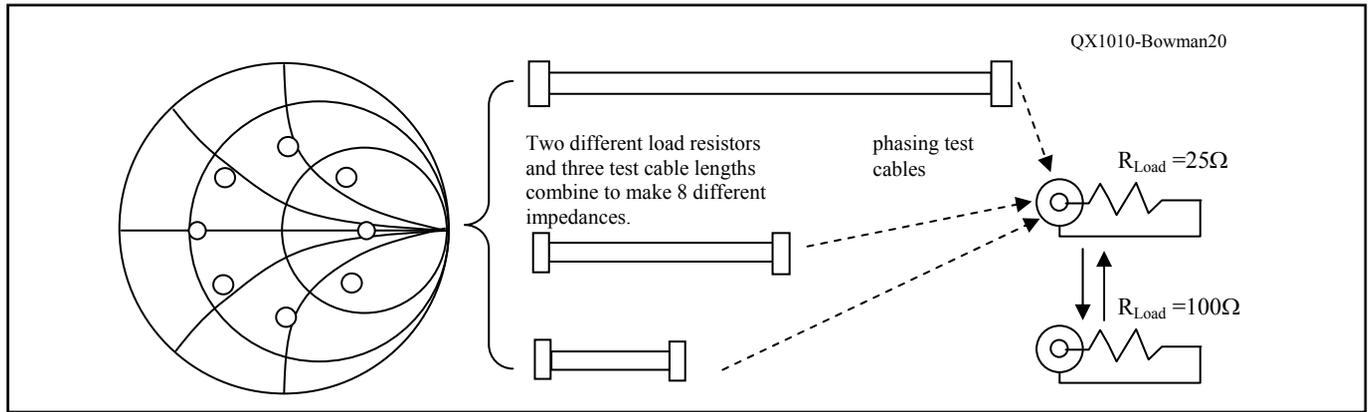


Figure 20 — General approach to creating a constant SWR circle of impedance. The load resistors depicted here are for an SWR of 2.

Table 3A
Comparison Test of Complex Impedance Measurements — VNA versus Bench-Top Method

Test Freq: 14 MHz	SWR					
	1.5		2.0		10.0	
Test Power: (0 dBm)	VNA	Bench-Top	VNA	Bench-Top	VNA	Bench-Top
Load	Impedance	Impedance	Impedance	Impedance	Impedance	Impedance
1	33.40∠+0.55°	33.96∠-0.63°	25.11∠+1.37°	25.19∠-0.05°	4.95∠+3.59°	4.70∠-0.17°
2	39.21∠+17.30°	40.20∠+15.80°	33.63∠+29.11°	34.25∠+28.60°	23.01∠+73.62°	23.95∠+72.74°
3	53.21∠+22.28°	53.82∠+20.60°	54.28∠+35.94°	56.18∠+34.12°	54.83∠+76.94°	57.27∠+75.68°
4	70.46∠+13.42°	70.20∠+11.87°	85.45∠+23.24°	85.12∠+21.80°	137.80∠+69.04°	141.90∠+67.00°
5	75.00∠-0.18°	72.40∠-2.13°	100.4∠-0.03°	101.60∠-0.56°	502.5∠-3.38°	482.20∠-5.05°
6	66.33∠-16.24°	65.70∠-17.10°	78.76∠-27.98°	77.34∠-28.81°	113.70∠-74.15°	109.60∠-75.50°
7	50.42∠-21.77°	50.14∠-23.73°	49.88∠-36.02°	49.39∠-37.38°	47.92∠-77.69°	47.31∠-77.90°
8	38.95∠-14.94°	38.60∠-16.20°	32.23∠-25.47°	32.51∠-27.17°	19.46∠-69.95°	19.80∠-73.20°

Table 3B
Percent Error at 14 MHz Between VNA Magnitude and Bench-Top Measurement

	1.5 SWR	2.0 SWR	10.0 SWR
Max Error (%)	3.47	3.50	5.05
Average Error (%)	1.45	1.36	5.05
Standard Deviation (%)	0.99	0.97	1.23

Table 3C
Degrees Error at 14 MHz Between VNA Phase Angle and Bench-Top Method Phase Angle

	1.5 SWR	2.0 SWR	10.0 SWR
Max Error (%)	1.96	1.82	3.76
Average Error (%)	1.49	1.20	1.80
Standard Deviation (%)	0.36	0.48	1.11

must be logged and stored carefully.

The bench-top method employs vector error correction for the three major systematic errors, but it doesn't correct temperature-induced drift errors, frequency drift, errors with the SOL standards, test equipment setting, reading, repeatability and linearity errors, or random noise and RF interference errors (especially if the DUT is an antenna). Be sure to limit the test signal to frequencies and levels that won't cause interference. Verify your generator's output impedance versus output amplitude. The one that I used in bench tests had a broad 50 Ω "sweet spot" at the higher power settings. Since I "eyeballed" my measurements from a 100 MHz analog oscilloscope, your results would be even better if you happen to own a digital oscilloscope or a vector voltmeter. After initial calibration and DUT measurement, it's good practice to recalibrate every so often. How often depends upon your test equipment's tendency to drift. Subsequent DUT measurements don't always require a new calibration unless drift is noticeable, or unless there were changes made to the system hardware or settings. The calculator DUT impedance measurement program does not wring out every available piece of error-corrected data; plenty of other corrected data are possible. And finally, don't forget to use the companion DUT Impedance Measurement Checklist, or some variation of it. That 8½ by 11 inch piece of paper serves as both a log and a guide to keep us on our simple path to complex impedance!

Notes

¹What is vector-error correction? In impedance measurement systems, vector-error correction is a numerical method of correcting the intrinsic errors of a measurement system through use of an array of error vectors that transform measured results into corrected results. The error vectors are derived from the measurement system's previous responses to a set of calibration loads.

²The Microsoft *Excel* spreadsheet created as an alternative to the HP 35s programmable calculator program is available for download on the ARRL QEX Web site. Go to www.arrl.org/qexfiles and look for **9x10_Bowman.zip**.

³What are voltage vectors? In RF voltage measurements, vectors are two-dimen-

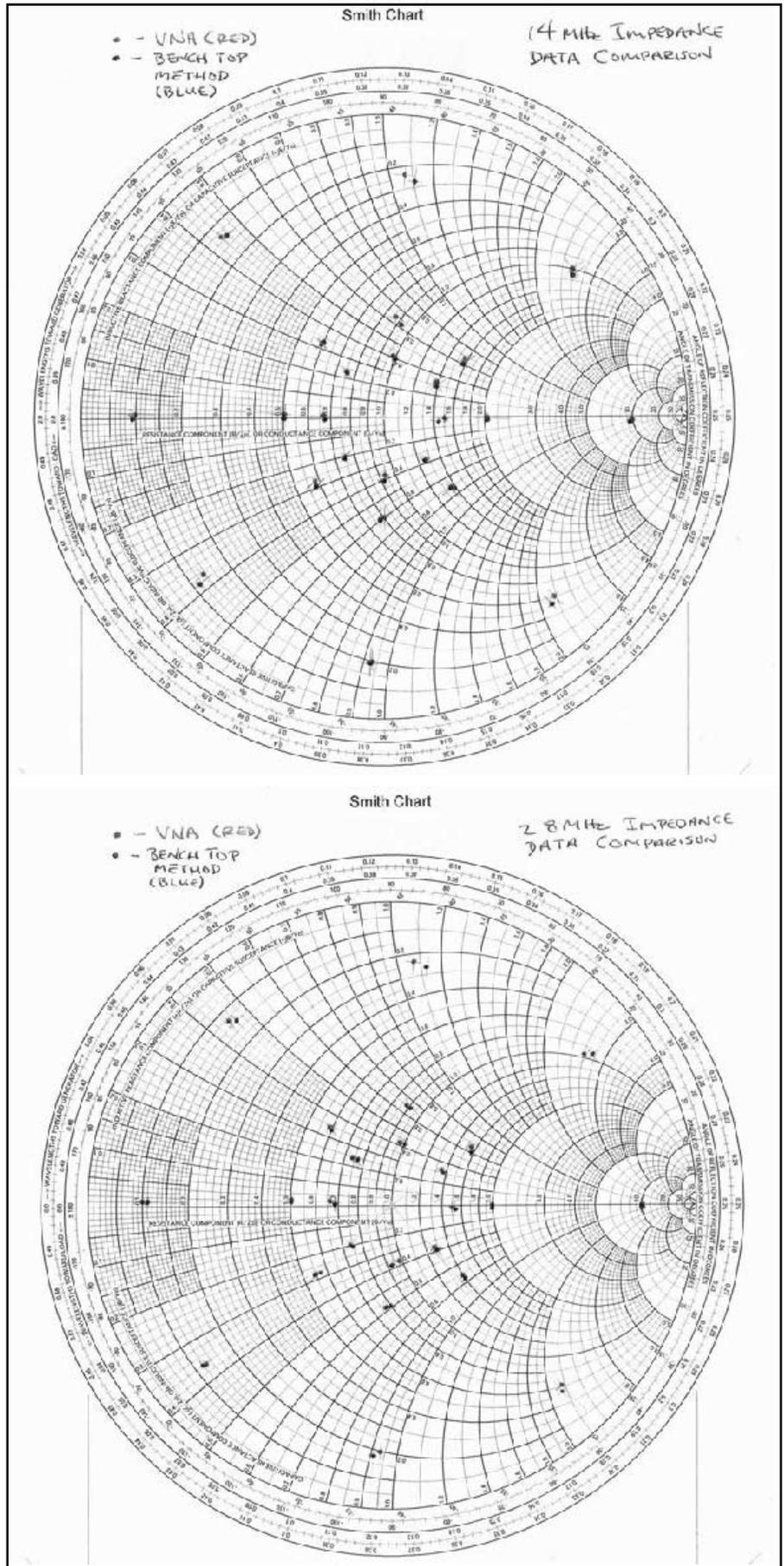


Figure 21 — The plot in Part A shows VNA impedances (black) versus bench-top method impedances (grey) at 14 MHz, and the difference between the same test loads is often less than the width of a pencil lead. The plot in Part B shows VNA impedances (black) versus bench-top method impedances (grey) at 28 MHz, and it shows similar results to the load tests at 14 MHz.

Table 4A

Comparison Test of Complex Impedance Measurements — VNA versus Bench-Top Method

Load	SWR					
	1.5		2.0		10.0	
Test Freq: 28 MHz	VNA	Bench-Top	VNA	Bench-Top	VNA	Bench-Top
Test Power: (0 dBm)	Impedance	Impedance	Impedance	Impedance	Impedance	Impedance
1	33.45∠+0.98°	33.94∠+0.43°	25.20∠+2.50°	25.45∠+1.52°	5.03∠+6.62°	5.54∠+4.48°
2	39.30∠+17.66°	39.96∠+17.32°	33.97∠+29.77°	34.25∠+29.79°	23.21∠+74.12°	24.08∠+73.06°
3	53.14∠+22.26°	53.86∠+22.23°	54.68∠+36.00°	55.64∠+34.77°	54.93∠+77.40°	57.65∠+76.34°
4	69.74∠+13.47°	70.26∠+12.33°	85.34∠+22.97°	85.42∠+21.17°	138.20∠+69.70°	144.30∠+71.35°
5	74.98∠-0.29°	76.73∠-0.65°	100.30∠+0.09°	100.10∠-1.28°	493.60∠-0.01°	500.80∠-2.21°
6	66.15∠-16.25°	66.79∠-16.97°	78.83∠-27.79°	78.54∠-28.24°	112.90∠-73.93°	110.70∠-76.09°
7	52.10∠-21.10°	49.83∠-22.79°	49.95∠-36.27°	48.59∠-37.81°	47.79∠-77.71°	46.58∠-78.46°
8	38.30∠-14.98°	38.18∠-15.70°	31.83∠-25.89°	30.81∠-27.19°	19.29∠-70.49°	19.01∠-71.47°

Table 4B

Percent Error at 28 MHz Between VNA Magnitude and Bench-Top Measurement

	1.5 SWR	2.0 SWR	10.0 SWR
Max Error (%)	4.36	3.20	10.14
Average Error (%)	1.65	1.27	3.83
Standard Deviation (%)	1.17	1.10	2.69

Table 4C

Degrees Error at 28 MHz Between VNA Phase Angle and Bench-Top Method Phase Angle

	1.5 SWR	2.0 SWR	10.0 SWR
Max Error (%)	1.69	1.80	2.20
Average Error (%)	0.69	1.09	1.49
Standard Deviation (%)	0.49	0.55	0.57

sional complex numbers that describe a sinusoidal voltage in terms of magnitude and phase components at a given fixed frequency. Vectors are also used in specifying other complex quantities such as voltage reflection coefficients and impedances. An RF voltage sine wave of a given frequency is a physical quantity with both a magnitude (rms, peak, or peak-to-peak voltage) and a phase angle (degrees). The phase angle is defined by its relative difference from the phase angle of a reference sine wave.

⁴Wes Hayward, W7ZOI, *Introduction to Radio Frequency Design*, ARRL, 1st Edition, 1994, p 156-158.

⁵Wes Hayward, W7ZOI, *Introduction to Radio Frequency Design*, ARRL, 1st Edition, 1994, p 151-153.

⁶Wai-Kai Chen, *The Circuits and Filters Handbook*, CRC Press, 2nd Edition, 2003, p 1197-1199.

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Amateur radio operator Mike Bowman, KG2MG, was first licensed in 1981 as N6EJT while stationed at Edwards AFB in the Mojave Desert. Through Amateur Radio, Mike stayed in touch with his family back east with the help of his brother Rick, KB2YG. Following his tour with the USAF, and with the encouragement and support of his family and his wife Mary Jane, Mike attended RIT in Rochester, New York and graduated in 1987 with a BSEE degree. Although he is an experienced RF engineer, he's still hooked on the can-do attitude and freewheeling spirit of Amateur Radio. No matter what, he always has a great time at the Dayton Hamvention every year with his brother Rick, and friends Skip, K2SR, Leah, K2LAR, Tony, N2LZA, and Jim!



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Using *QuickSmith*: Part 2

Harold provides a description of how to design amplifiers for optimum gain or noise figure using S parameters and QuickSmith.

An Introduction to S Parameters

By using *scattering* or S-parameters, any two-port device can be analyzed and treated as a black box with an input port (1) and an output port (2). By studying the S-parameters much can be learned about the behavior and operation of the two-port device. The device can be an *active* or *passive* component(s) or any combination of the two. The measurements consist of both *magnitude* and *phase angle*. No matter how simple or complex a two-port device may be it can be analyzed using S-parameters.

S₁₁ Forward Reflected

Figure 1 explains the S-parameters that we will be exploring here. At A, the parameter S₁₁ consists of the forward voltage wave and the reflected voltage wave. Remember, S-parameters have both magnitude and phase. If we are to compare the reflected voltage with the forward voltage the phase angle must also be considered.

In Figure 1A the parameter S₁₁ is a measure of the impedance match or mismatch at the input port. The incident signal voltage is applied to the input port (1) and the reflected signal voltage is measured at the

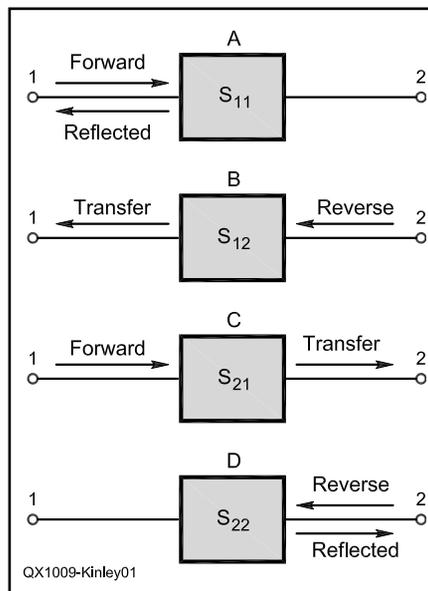


Figure 1 –How to measure the four S parameters. Part A shows the incident and reflected voltage on the input for S₁₁. Part B shows the incident voltage on the output port and the voltage transferred to the input port for S₁₂. Part C shows the incident voltage on the input port with the voltage transferred to the output port for S₂₁. Part D shows the incident and reflected voltage on the output port for S₂₂.

input port (1)—hence, the expression S₁₁. With all S-parameters the magnitude can be expressed as a numerical factor or in decibels. And, the S-parameters may be expressed in *rectangular* or *polar* format. The magnitude and angle represents the polar format. This is the most commonly used expression of S-parameters.

At the input port (1) in Figure 1A the reflected voltage divided by the forward voltage is S₁₁. This is equal to the reflection coefficient, Γ, from zero to one. This can also be expressed in decibels as 20log(Γ).

S₁₂ Reverse Transfer

In Figure 1B the S₁₂ parameter is illustrated. This is a measure of the amount of signal transfer from port 2 to port 1. Typically, port 1 is considered the input port and port 2 the output port. Some circuits are bidirectional, that is, it makes no difference which port is the input or output. The signal transferred between the two ports will be equal in either direction.

However, in the case of an amplifier, with port 1 the input and port 2 the output, the signal transfer from port 1 to port 2 would be very different from the signal transfer from port 2 to port 1. The signal transfer

Table 1

Freq MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	Mag	Angle	Mag	Angle	Mag	Angle	Mag	Angle
400	.5227	-103.4	7.552	112	.0764	48.3	.5405	-44.4
450	.4972	-109.9	6.939	108.7	.0797	47.6	.5068	-45.3
500	.4788	-117	6.353	104.7	.0831	47	.4733	-46.4

BFR92T Transistor V_{CE} = 1.5V I_C=5mA

from port 2 to port 1 would be a measure of the *isolation* of the amplifier. Again, this can be expressed in decibels or as a multiplication factor.

S₂₁ Forward Transfer

S₂₁ is a measure of the transfer of signal from port 1 to port 2. See Figure 1C. If this is an amplifier, the S₂₁ parameter would be a measure of the forward gain of the amplifier. This can be expressed as a multiplication factor or in decibels.

S₂₂ Reverse Reflected

The S₂₂ parameter is a measure of the reflected signal at the output port with the incident signal applied to the output port. See Figure 1D. This figure can be considered a measure of the impedance match or mismatch in the reverse direction. As in the case of the input port (S₁₁), when expressed as a factor from zero to one this is equal to the reflection coefficient, Γ. S₂₂ can also be expressed in decibels as 20log(Γ).

Designing For Maximum Gain

Now, let's look at another use of *QuickSmith* software—designing a small-signal RF amplifier using S-parameters from manufacturers' data sheets. S-parameters provide a means of defining the operation of a two port device—either active or passive. Table 1 lists the S-parameters for a transistor BFR92T. Table 1 shows the S-parameters for three frequencies—400 MHz, 450 MHz and 500 MHz. The S-parameters were not provided for 450 MHz but were interpolated from the parameters given for 400 MHz and 500 MHz. The S-parameters for 450 MHz shown in boldface in Table 1 are the interpolated values. It is important to note that the S-parameters are measured between a 50 Ω source and a 50 Ω load. Furthermore, the S-parameters listed are only valid for the transistor V_{CE} and I_C listed. Using *QuickSmith*, we will use these S-parameters to design a small-signal single-stage RF amplifier.

First, start *QuickSmith* and click on the **Amplifier Design** tab on the menu and then select **S-parameter Design/Analysis**. You will see two Smith charts. The one on the left represents the source plane and the one on the right represents the load plane. From the menu, click on **Enter Parameters** and from the drop-down menu click on **S-parameters**. You will then see a form in which to enter the S-parameters of the device we are using (BFR92T). Click on the **Polar** button and enter the S-parameters for 450 MHz from Table 1. Then, click on **Stability**. The values for *K* and *DELTA* are then computed. If *K* is greater than one and delta is less than one the device is unconditionally stable. See

Figure 2. Since *K* is less than one, we must be careful to avoid input/output impedances that might cause the amplifier to become unstable and break into oscillation. Click on **Circles** and check **Stability Circles**. The stability circles are drawn on the source and load planes as shown in Figure 3. Notice that the stability circles cut across both the source and load planes. It is important that we keep the load and source impedances away from the stability circles. Often, designers choose to use stabilization techniques so that the active device (transistor) is made unconditionally stable. That is beyond the scope of this article.

There are several methods by which the amplifier may be designed. Since the transistor is not unconditionally stable the first step is to determine the maximum stable gain

(MSG). The MSG is determined from the formula below:

$$MSG = 10 \log \left(\frac{S_{21}}{S_{12}} \right) = 10 \log \left(\frac{6.939}{0.0797} \right) \\ = 10 \log (87.064) = 19.4 \text{ dB} \quad [\text{Eq 1}]$$

In the equation above, S₂₁ and S₁₂ are taken from Table 1 for 450 MHz.

In this first example, the amplifier is designed for maximum stable gain. Click on **Circles** and then check **Available gain circles**. Since available gain circles was chosen the input can be any impedance or gamma that falls on the chosen gain circle and will not be matched to the 50 Ω source. The output will be matched to the 50 Ω load. The pop-up form indicates that the maximum gain is 19.4 dB. This is the MSG that was calculated in the equation above. We are designing the amplifier for maximum stable gain; but, in order to keep the design very stable let's shoot for less than that and use a gain figure of approximately 18 dB. You will now see the screen in Figure 4. Increase the gain to 18.1 dB by incrementing the value in the **Ga(dB)** window. At this point, the gain circle passes through the origin (50 Ω point) of the Smith Chart. Click on the **Redraw** button on the menu to remove old circles in order to clean up the display. [Throughout this article the author refers to a blue dot on the various figures. Although QEX is not printed in color, we left the color reference in the text.

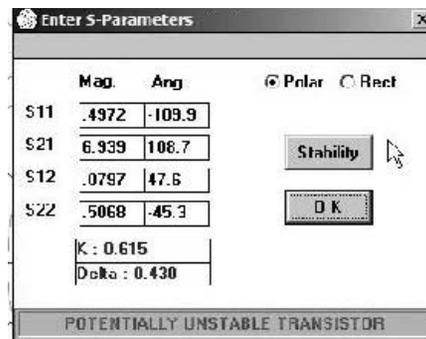


Figure 2 – The S-parameter input dialog. The program shows the transistor is potentially unstable.

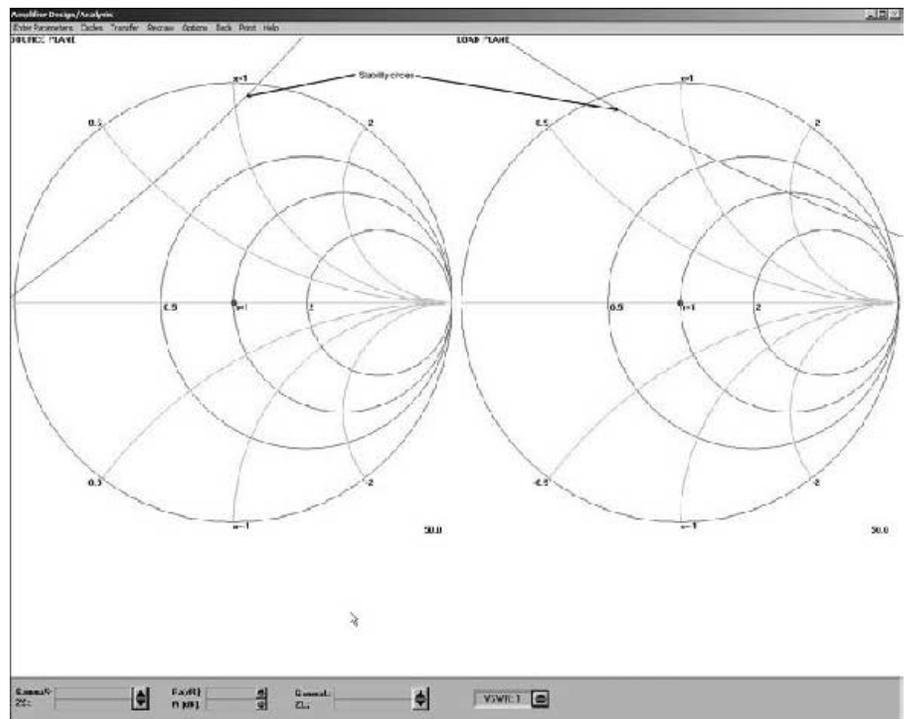


Figure 3 – The source and load planes showing the characteristics of the transistor without matching. The stability circles intersect the planes in the inductive half of each plane and the blue dot is at the center of each plane.

When you are looking at the software on a computer screen, you will be looking for this blue dot. — *Ed.*] Click on the **GammaS** up arrow to “walk” the blue dot around the gain circle to the 50 Ω point on the Smith Chart. See Figure 5. The source impedance (Z_S) or gamma (Γ_S) is indicated on the left chart and the load impedance (Z_L) or gamma (Γ_L) is indicated on the right chart. The source gamma (Γ_S) is 0.008@ -124.125 degrees and the source impedance (Z_S) is 49.541 – j0.668 ohms—practically a pure 50 Ω impedance.

The load gamma (Γ_L) is 0.508 @ 44.8 degrees and the load impedance (Z_L) is 69.065 + j66.599 ohms. It is required that the source and load impedances or gammas be equal to these values to produce the gain of 18.1 dB.

The next step is to design a matching network such that the input of the transistor will “see” a source gamma (Γ_S) of 0.008@ -124.125 degrees or source impedance (Z_S) of 49.541 – j0.668 Ω. Actually, since the source impedance is 50 Ω we don’t have to use an impedance-transforming network between the transistor input and the source—assuming that our source impedance is 50 Ω.

On the menu, click on **Transfer** and then **Load impedance**. A pop-up indicates that the impedance to be transferred is the conjugate of the load impedance shown in Figure 5. Next, click on **OK**. Referring again to the menu, click on **Back**. You will see the screen shown in Figure 6. The Smith chart in the left pane represents the *conjugate* of the load impedance and the right pane provides a schematic design editor by which we can design an impedance network that will transform the 50 ohm load impedance to 69.065 + j66.599 ohms. Since we are designing the amplifier for an operating frequency of 450 MHz go to the **Assign values** tab on the menu and click on **Frequency** and enter 450 MHz. To get there you may have to click on the **wrench** icon on the toolbar first. Now, using the schematic editor set up a pi network with shunt capacitances of 10 pF and a series inductance of 15 nH. Drag and drop a shunt-connected capacitor (C_3) onto the schematic as shown in Figure 7 and set the initial value to 10 pF. Drag and drop a series inductance (L_4) onto the schematic and set the initial value to 15 nH. Next, drag and drop another shunt capacitance (C_5) onto the schematic and set the initial value to 10pF. The values of the individual components of the pi network can be adjusted experimentally to place the blue dot directly over the center of the Smith Chart—the 50 Ω point. To make smaller adjustments to the values of each component the step size can be changed by double clicking on the value of the component. The blue dot is placed on the unity conductance circle by setting the value

of L_4 to 15.1 nH. Adjusting C_5 to 19.9 pF places the blue dot at the center of the Smith chart—the 50 Ω point. The result is shown in Figure 7. Figure 8 shows how the matching network is placed between the 50 Ω load and the transistor output such that looking

from the transistor output toward the load the transistor output “sees” an impedance (Z_L) of 69.065 + j66.599 Ω or a gamma (Γ_L) of 0.508 @ 44.805 degrees. The biasing circuitry is not shown—only the RF circuitry that affects the source/load impedance.

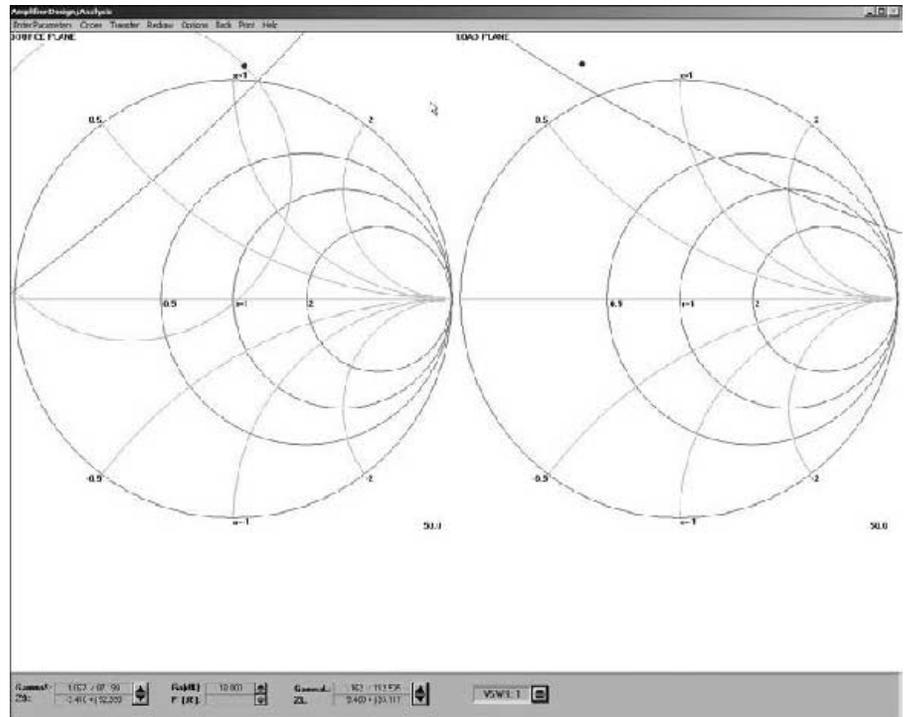


Figure 4 – The source and load planes showing the 18 dB gain circle and the blue dot outside of the stability area for each plane. The gain circle comes very close to the center of the source plane.

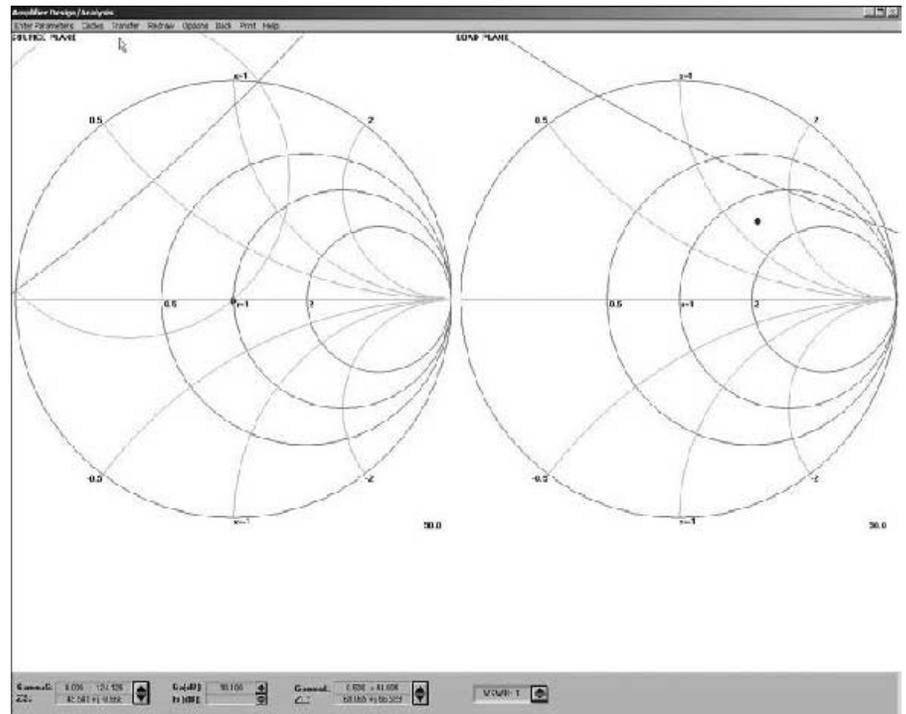


Figure 5 – The source plane showing that the gain circle intersects the center with a gain of 18.1 dB and the blue dot is at 50 Ω.

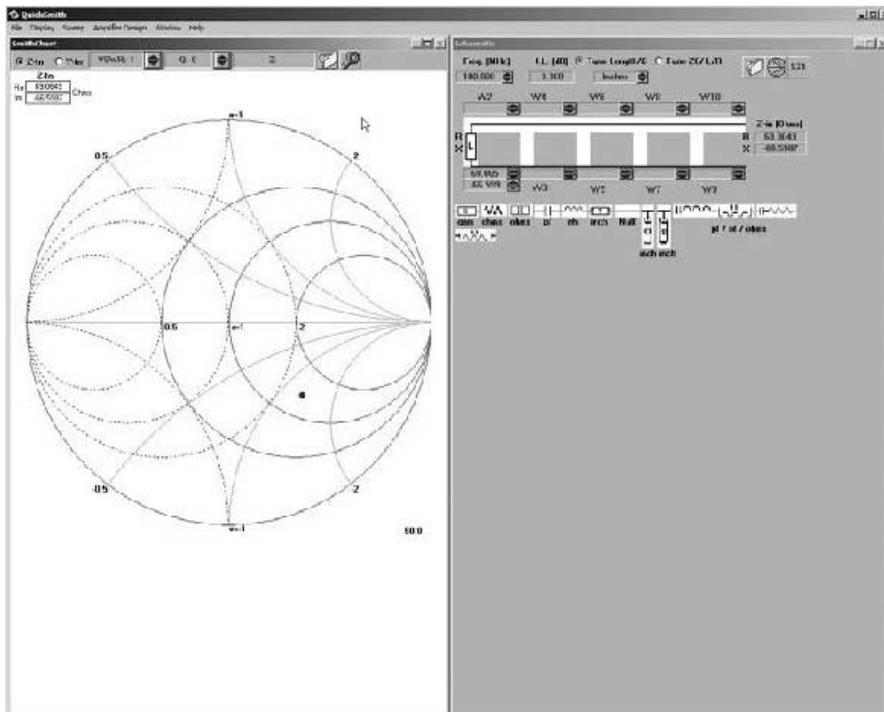


Figure 6 – The schematic editor and load plane windows showing the initial step of designing the output pi network. The blue dot indicates the conjugate of the load impedance. The goal is to move the dot to the center of the Smith Chart.

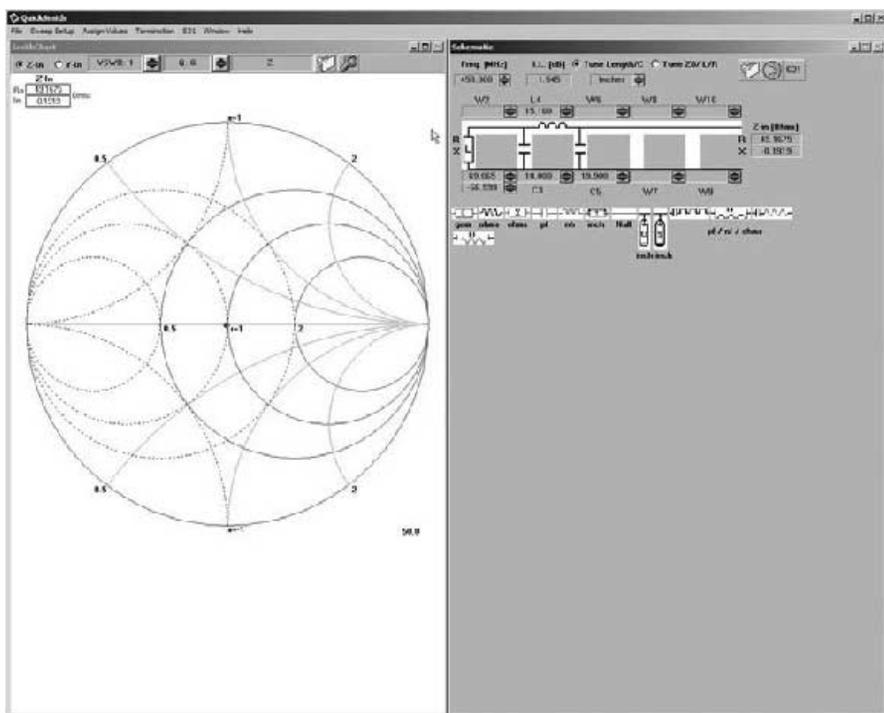


Figure 7 – The schematic editor and load plane after the output pi network is designed. The blue dot has moved to the center of the Smith Chart.

Recall that the maximum stable gain for the previous example was approximately 19.4dB. On the *QuickSmith* menu, click on the *Folders* icon. The gain is set to 18.1dB. Increase the gain by incrementing the value in *Ga(dB)*. Notice that the gain circles transition smoothly until the gain figure hits the maximum stable gain—approximately 19.4dB. At this point the blue dot jumps right into the circle of instability, indicating that the amplifier has broken into oscillation. Reset the gain, *Ga(dB)*, to 18.1dB.

Now, the transistor output has been matched to the 50 Ω load impedance through the matching network designed on the schematic editor. However, the input to the transistor is not matched to the 50 Ω source impedance. In fact, a fairly high SWR exists at the input. Just how high is the input SWR? The formula in Equation 2 is used to calculate the input gamma (Γ_{IN}). This is the reflection coefficient at the input to the active device (transistor).

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{11}\Gamma_L} \quad [\text{Eq 2}]$$

Once we calculate the value of Γ_{IN} we can compute the SWR from the formula in Equation 3.

$$SWR = \frac{1 + |\Gamma_{IN}|}{1 - |\Gamma_{IN}|} \quad [\text{Eq 3}]$$

First, the formula in Equation 2 is executed by substituting the S-parameters from Table 1. The value for Γ_L is found in Figure 5. It is 0.508@44.8°. Remember the rules for performing complex mathematical computations: multiply and divide in polar form, add and subtract in rectangular form. I prefer to use software called *eCalc* which is downloadable from www.ecalc.com. It only costs about \$15 and is quite easy to use. Using *eCalc* you can enter computations in mixed format (polar and rectangular) without having to convert back and forth between polar and rectangular formats to do the computations. Using *eCalc* for the formula in Equation 2 yields a figure of $\Gamma_{IN} = 0.77@-129.9^\circ$. In Equation 3 the *absolute value* of this figure is 0.77 (disregard angle) and yields a SWR figure of 7.7:1.

In the example presented just previously the amplifier could not be designed for maximum gain because the transistor was not unconditionally stable. So the design was limited to the maximum stable gain (MSG). Actually, to be on the safe side, the amplifier in the previous example was designed with a gain that was below the MSG. In cases where the transistor is unconditionally stable the amplifier can be designed for maximum gain without worrying about the amplifier becoming unstable and breaking into oscillation.

Table 2

Freq (MHz)	F_{min} (dB)	Γ_{opt}	$r_r/50 \Omega$
450	1.5	0.28@29°	0.34

BFR92T Transistor $V_{CE} = 1.5V$ $I_C = 5mA$

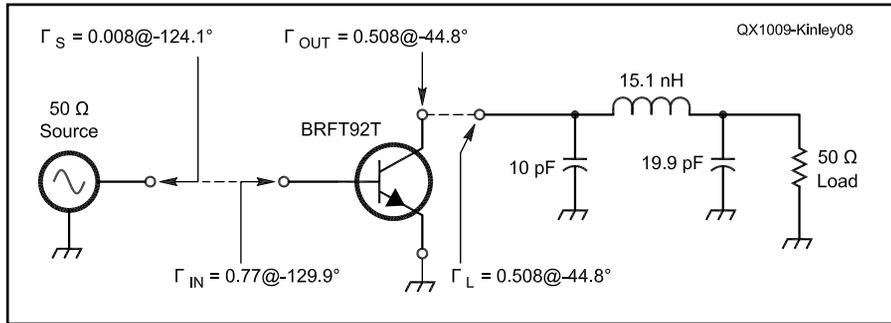


Figure 8 – A simplified schematic of the amplifier showing the transistor and the output pi network.

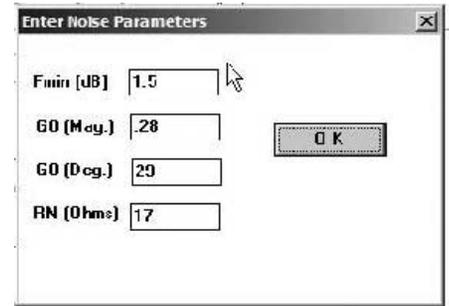


Figure 9 – The Noise Parameter input dialog.

In such cases both the input and the output are *conjugately* matched to the source and load respectively. The procedure of matching the input and output for maximum gain is called *simultaneous conjugate matching*. This simply means that the load impedance is the conjugate of the output impedance and the source impedance is the conjugate of the input impedance. There is a unique *combination* of source and load impedances that, together, produce the maximum gain. This is because the load impedance affects the input impedance and the source impedance affects the output impedance. This, in turn, is caused by the feedback from output to input defined by the S-parameter, S_{12} . If S_{12} is zero then the load impedance does not affect the input impedance and the source impedance does not affect the output impedance. However, in practical devices (transistors) S_{12} is never zero. In the case of simultaneous conjugate matching, the input SWR and output SWR are very good. The magnitude of S_{11} and S_{22} (in the final circuit) would be very low—zero under *ideal* conditions.

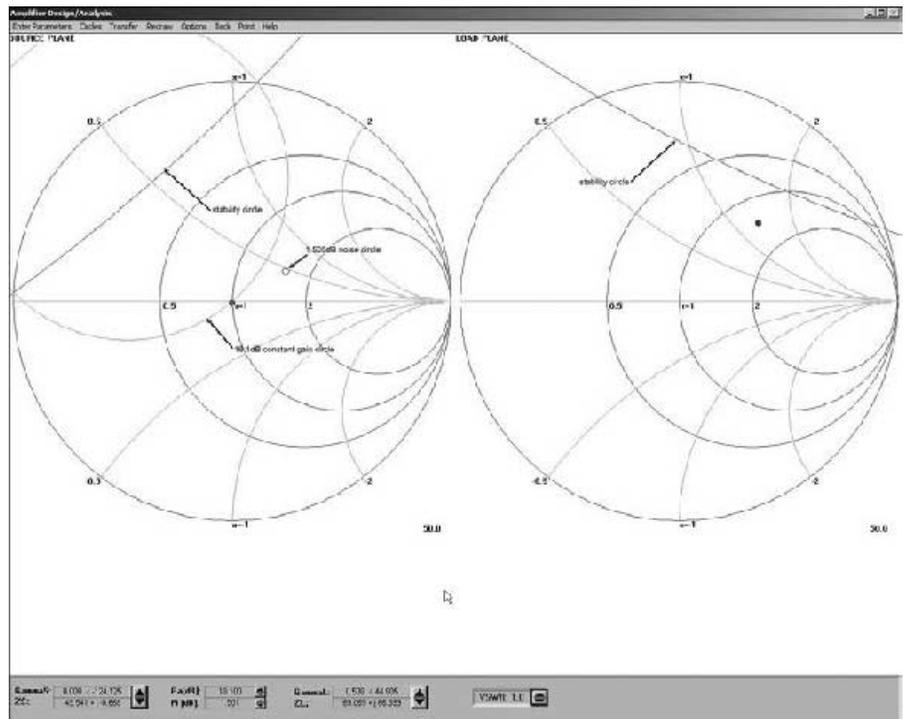


Figure 10 – The source and load planes showing a matched input, matched output, and sub-optimum noise circle.

Designing For Optimum Noise Figure

Now, let's take a look at using the *Noise circles* tool. Click on *Enter parameters > Noise parameters* and enter the figures from Table 2 as shown in Figure 9. Note that the figure shown in Table 2 for r_n is normalized to 1 Ω and must be multiplied by 50 before entering in the table shown in Figure 9. Click on *Circles* on the menu and check *Noise circles* and enter a figure of 1.505. The minimum noise figure according to Figure 9 is 1.5 dB. If 1.5 dB is entered the noise figure on the Smith chart would be a single dot and hardly visible. By entering a noise figure of 1.505 we can see a noise circle on the chart. Your display should look like Figure 10. Notice that the noise circle representing a noise figure of 1.505 dB is very small. The next objective is to reduce the gain of the constant gain circle $Ga(dB)$ so that the gain circle passes through the center of the 1.505 dB noise circle. This occurs at a gain of approxi-

mately 17.4 dB. Click on *Redraw* to clear out old circles. The next objective is to place the blue dot at the center of the noise circle. This is done by reducing Γ_S to “walk” the blue dot around the constant gain circle to the center of the noise circle. See Figure 11.

At the bottom of Figure 11 we can see that in order to make the amplifier operate at a gain of 17.4 dB and a noise figure of 1.505 dB the Γ_S figure must be $0.274@29.463^\circ$ and the Γ_L figure must be $0.409@60.191^\circ$. This will require that an impedance transforming network be placed between the transistor input and the source and between the transistor output and the load. The network placed at the output will match the 50 Ω load to the transistor's output impedance—resulting in a conjugate match. The network placed at the input will not match the 50 Ω source to the transistor's

input impedance but rather will present the proper impedance “seen” by the transistor input looking toward the source. Both networks are designed using *QuickSmith* and are described here.

First, the input network is described. Click on *Transfer > Source Impedance* and click on *OK* on the popup dialog box. Click on *Back* on the menu. Since we already have a low-pass pi network we can manipulate the values of these components in order to place the blue dot at the center of the Smith chart. Increasing the value of L_4 to 16.9 nH places the blue dot on the *unity conductance* circle. Then, reducing the value of C_5 to 13.8 pF “walks” the blue dot around the unity conductance circle to the center of the Smith chart. This gives us the design for the input network as shown in Figure 12.

Next, the output network is designed as

described here. Click on the **Folders** icon on the toolbar to get back to the **Source** and **Load** planes on the Smith charts. Click on **Transfer > Load Impedance** on the menu. Click on **OK** on the popup dialog box. Click on **Back** on the menu. This gets us back to the schematic editor. Reduce the value of L4 to 14.9 nH to place the blue dot onto the unity conductance circle. Then, increase the value of C5 to 17.6 pF to place the blue dot at the center of the Smith chart. The design of the output matching network is shown in Figure 13.

The final design of the RF amplifier is shown in Figure 14. The output of the amplifier is conjugate matched to the 50 Ω load impedance by the low-pass pi network. However, the input is not “matched” to the 50 Ω source impedance. The input impedance transformation network was designed so that, looking from the transistor input toward the source, the transistor input “sees” a Γ_S of $0.274@29.463^\circ$ or a Z_S of $77.292 + j22.481 \Omega$ s as shown in Figure 11. In other words, the 50 Ω source impedance is transformed to $77.292 + j22.481 \Omega$ looking from the transistor input toward the source. This was necessary in order to produce a gain of 17.4 dB at a noise figure of 1.505 dB. An impedance mismatch will occur at the input to the pi network resulting in a significant SWR. In order to determine the SWR at the input to the pi network we have to work a couple of formulas. First, the formula for finding Γ_{IN} is shown in Equation 4 below.

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad [\text{Eq 4}]$$

The S parameters for Equation 4 are found from Table 1 and Γ_L is found from Figure 11 (**GammaL**). Once the figure for Γ_{IN} is calculated the figure is substituted into the formula in Equation 5 to find Γ_{IMN} , the gamma at the input to the matching network.

$$\Gamma_{IMN} = \left| \frac{\Gamma_{IN}^* - \Gamma_S}{1 - \Gamma_S \Gamma_{IN}} \right| \quad [\text{Eq 5}]$$

In Equation 5 the asterisk at Γ_{IN} indicates that this is the complex conjugate of Γ_{IN} . This means that the sign of the angle is changed. The figure for Γ_S is found from Figure 11 (**GammaS**). Using *eCalc* to do the equations, Γ_{IN} was calculated to be $0.755@-120.6^\circ$. The figure for Γ_{IMN} was calculated to be 0.79. Substituting 0.79 into Equation 3 yields a SWR of 8.5:1 at the input.

The input or output SWR is sometimes higher than desired. In such cases some adjustments and tradeoffs (such as noise figure and gain) have to be made in order to achieve a more desirable input/output SWR. Sophisticated (and expensive) design

software can enable the user to achieve these goals without resorting to complicated mathematical computations or trial and error techniques. Although *QuickSmith* doesn't provide these features, as you can see from just the examples illustrated here,

the *QuickSmith* freeware is quite useful and educational. I recommend using this freeware along with studying some good RF textbooks to increase your knowledge of the subject. Several good RF design textbooks are listed in the Bibliography.

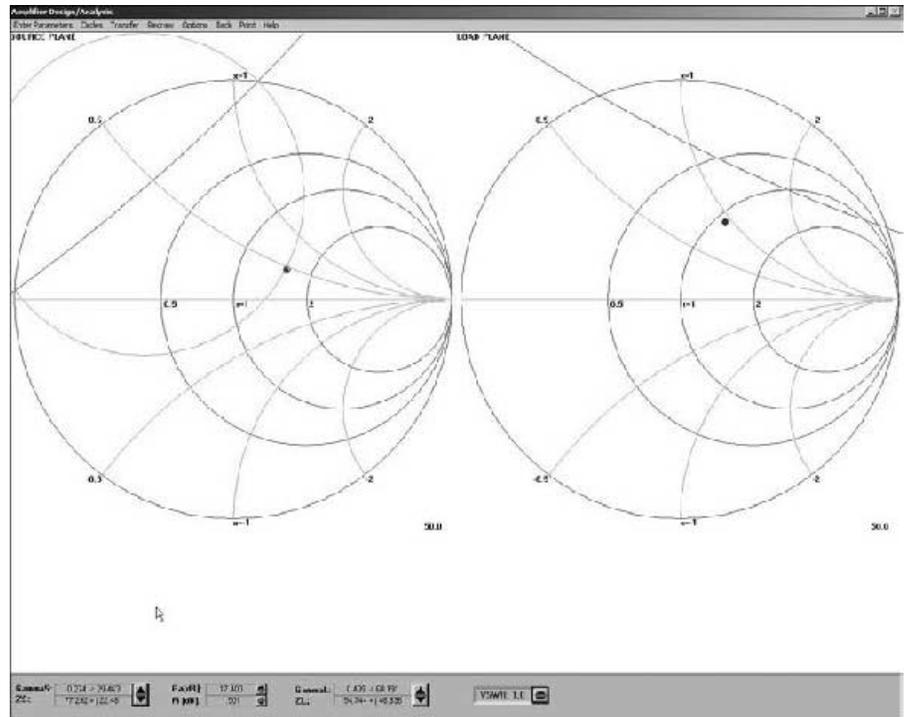


Figure 11 – The gain, $G_a(\text{dB})$, is reduced to 17.4 dB so that the gain circle passes through the center of the noise circle. Then, the blue dot is “walked” to the center of the noise circle by decreasing Γ_{IN} .

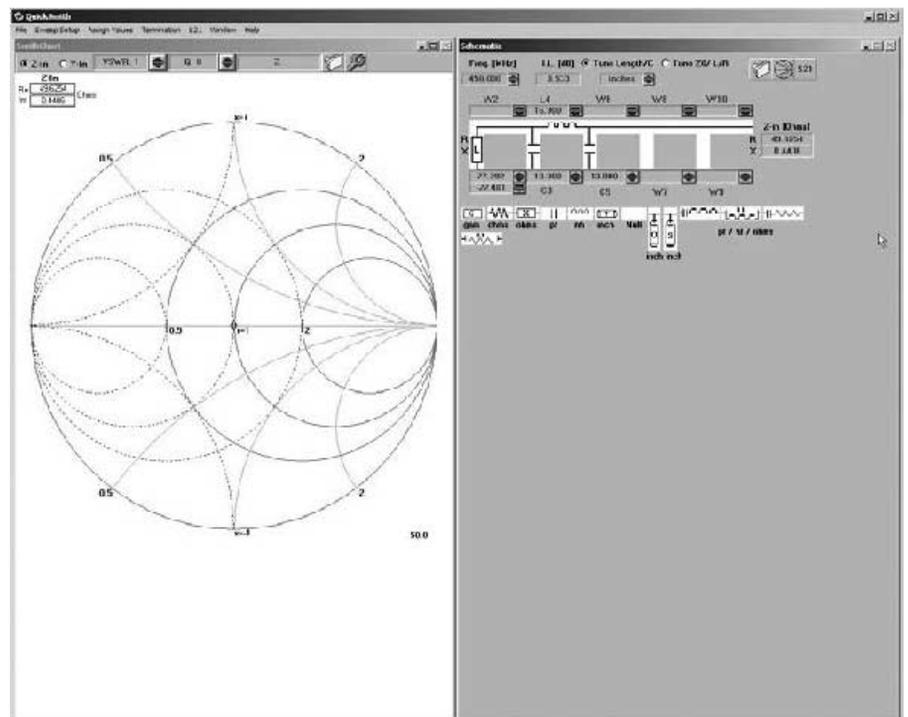


Figure 12 – The design of the input impedance transforming network is shown here.

Harold Kinley, WA4GIB, first studied electronics at a technical school, and is a Certified Electronics Technician. He held a First Class Radiotelephone License, which was later “downgraded” to a General Radiotelephone Certificate. Harold worked in radio and television broadcasting and later in commercial two-way radio. He started as a district radio technician for the South Carolina Forestry Commission, and 31 years later retired as Regional Communications Manager for the same agency. He has always enjoyed field work, installing, maintaining and repairing communication equipment. Harold completed the NRI Complete Communications Course with high honors, studied a CIE electronics course and an MTI training course as well as much independent study for which there were no certificates or degrees — just the knowledge acquired. An ARRL Member, Harold was first licensed as a Novice in 1962 and upgraded Conditional (General) in 1963. He finally upgraded to Extra class in 1998. Harold first began writing for publication in 1976 for the NRI Journal, and later had many articles published in Popular Electronics, Electronic Servicing & Technology, EMC Technology and started a column called “Technically Speaking” for Mobile Radio Technology in the early 90s. Harold has written three books, The PLL Synthesizer Cookbook, Standard Radio Communications Manual and The Radiomans’s Manual of RF Devices, Principles & Practices. He recently revised and expanded the last title and renamed it The RF Desk Reference for Wireless Communications. That book is only available directly from the author. See www.haroldkinley.com for details. Harold has been enjoying retirement since 2002, and still enjoys the wonderful hobby of ham radio.

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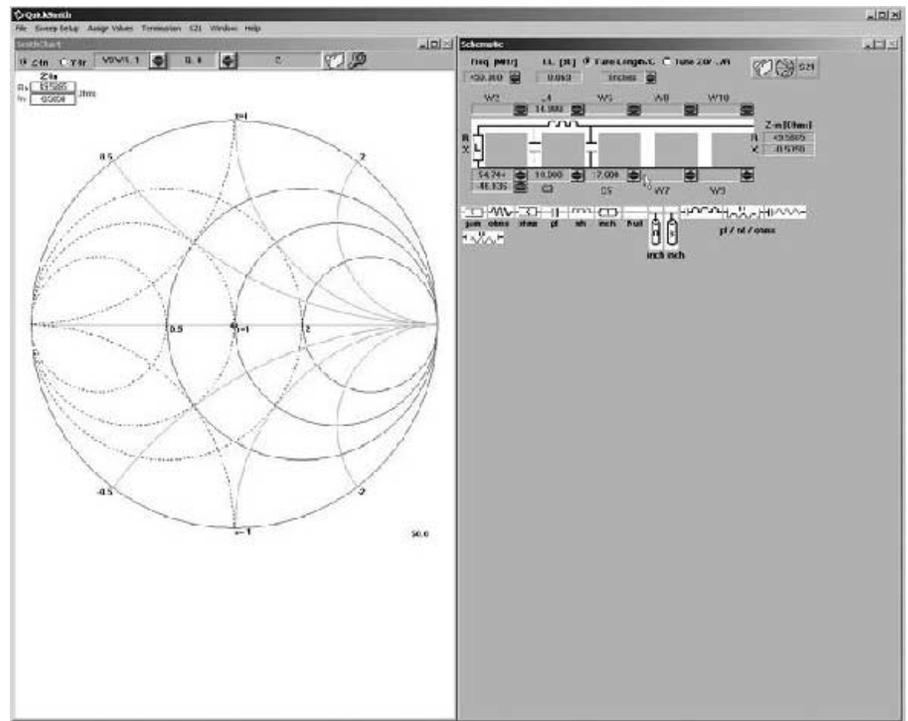


Figure 13 – The schematic editor and load plane showing the output pi network to match the output of the transistor.

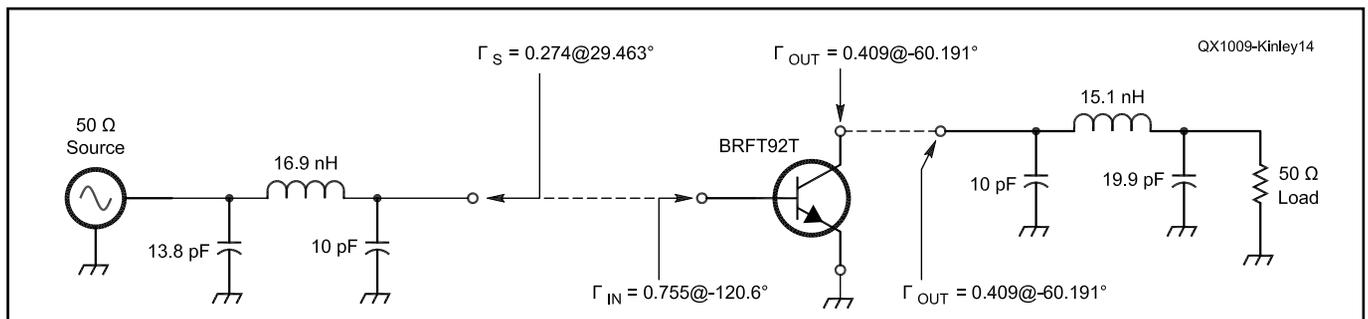


Figure 14 – The final schematic showing only the matching networks and the RF characteristics of the transistor. The bias circuitry is omitted.

QEX

Synthesizing an Audio AGC Circuit

Learn the steps involved with developing an AGC circuit suitable for your next receiver project.

While experimenting with my Ultra-RX1 ultrasonic receiver, to receive CW at 40 kHz, I found the volume deafening. The receiver was designed to hear bat and insect “conversations,” which are generated at a much lower sound pressure level (SPL). The TR40 CW transmitter I used puts out a pressure wave 20 dB above that. To cure this problem, I designed an automatic gain control (AGC) circuit and incorporated that into the receiver. It then occurred to me that this simple yet elegant circuit might be useful in minimalist Amateur Radio receivers such as direct conversion QRP projects. This article presents my thinking in working through the design, and presents a stand-alone AGC circuit with a bill of materials.

The goal of adding AGC to a receiver system or audio circuit is to limit the output volume to a tolerable level when the signal becomes larger than an arbitrary reference level. A majority of the circuits you’ll find to accomplish this task place a voltage controlled attenuator in front of a fixed high gain amplifier, or modify the amplifier’s gain, each with a dc voltage derived from the amplifier output. I chose to use the variable attenuator method since I planned to implement the amplifier with a fixed gain operational amplifier (op-amp). The block diagram and desired system response are shown in Figures 1A and 1B.

Choice of Attenuators

There are a number of choices for attenuators: MOSFETs, JFETs, LED-photocell combos, custom ICs, and more. I opted to use a MOSFET, since they are cheap and readily available. Instead of randomly searching for what works on the bench, I

measured the drain-to-source resistance of a 2N7000 N-channel MOSFET to check the range of dc feedback voltages required for the given resistance range. I used a 9 V battery, a 10 kΩ potentiometer across the gate and source and an ohmmeter across the drain and source. The results are graphed in Figure

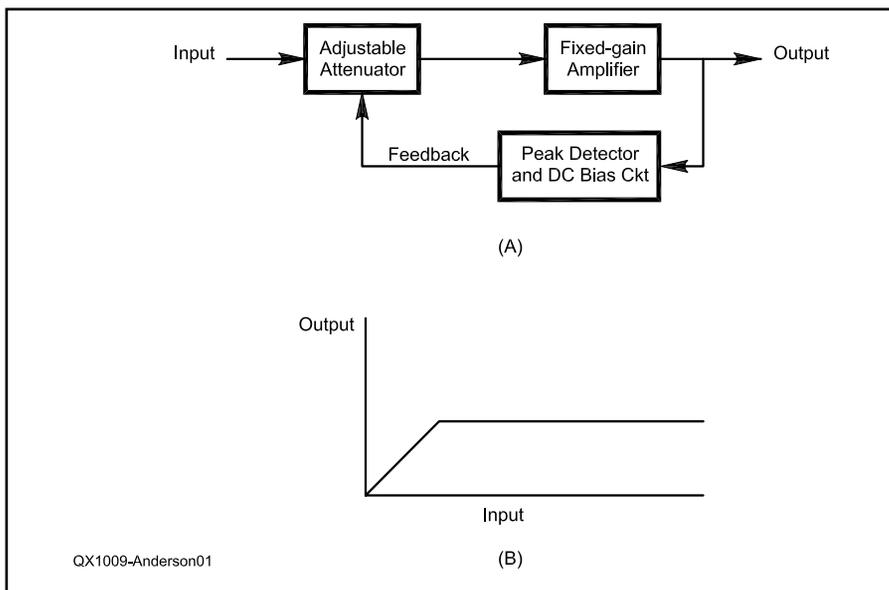


Figure 1 — Part A shows the block diagram of the AGC system and Part B graphs the system response.

Table 1
Gate Voltages Required for a Given Drain-Source Resistance

<i>Vout/Vin, assuming preamp gain of 50</i>							
<i>Vin mvpp</i>	20	40	80	160	320	640	
<i>Vout vpp</i>	1.2	1.2	1.2	1.2	1.2	1.2	
<i>Attenuator</i>	0.5	0.25	0.125	0.0625	0.03125	0.015625	
<i>Rbias</i>	4.70E+04	4.70E+04	4.70E+04	4.70E+04	4.70E+04	4.70E+04	
<i>Rp</i>		15667	6714	3133	1516	746	
<i>Rds</i>		23500	7833	3357	1567	758	
<i>Vgs of FET</i>		2.24	2.35	2.39	2.40	2.40	

2 and tabulated in Table 1.

Note that the resistance of the 2N7000 approaches a minimum with a high gate voltage; and achieves a nominal resistance of 23 k Ω for 2.2 V dc bias. The useful range of resistance is about 80 k Ω to about 500 Ω . *These facts dictate the gate bias voltage for the FET required from the peak detector*, as noted in Table 1. See Sidebar 1 for a derivation of the formulas used for the spreadsheet.

Choices for a DC Control Circuit

There are a number of circuit choices for the peak detector and filter. Perhaps the most common is the op-amp derived peak detec-

tor followed by a passive RC low-pass filter. Figures 3, 4 and 5 present evolving choices from this starting point.

Figure 3A displays a popular textbook version of an op-amp based peak detector.¹ A positive peak detector is constructed using an op-amp with diode and resistor feedback and parallel cap and resistor to ground as the load. When the + input of U1 exceeds the - input, the op-amp output goes high, causing D1 to conduct, charge C2 and lock the - input voltage to the same level as the + input. When the + input then drops below that of the - input,

¹Notes appear on page 27.

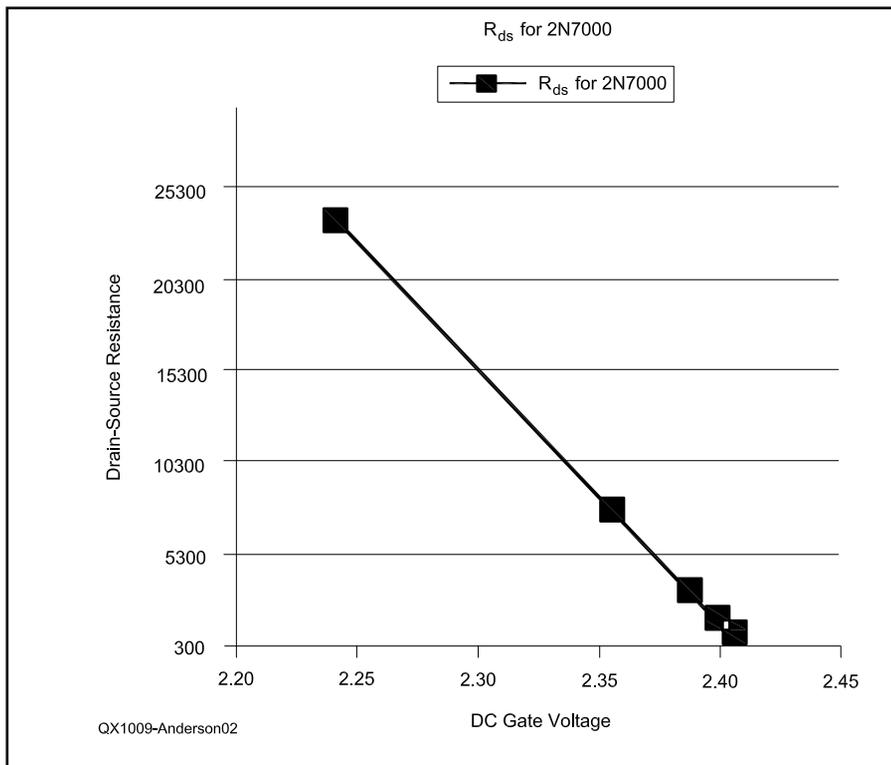


Figure 2 — A graph of the Drain-to-Source Resistance of the 2N7000 FET.

Table 2

Bill of Material

Qty	Designation	Item	Mouser #
1	Q2	2N7000 MOSFET	511-2N7000
1	U1	4580 op-amp, 8-PIN DIP	NJM4580DD
1	Q1	PN2907 PNP TRANSISTOR	512-2N7000
2	R1, R7	47k RESISTOR	291-47K-RC
2	R2, R3	100k	291-100K-RC
1	R4	10K	291-10K-RC
1	R5	470K	291-470K-RC
1	R8	18K	291-18K-RC
5	C1-C5	10 UFD	140-HTRL50V10
1	C6	22 PF	140-500N5-220J-RC

the cathode side of the diode (labeled V_{Bias}) retains the voltage of C2 for a bit. In effect, V_{Bias} reports the peak value of the input signal plus the bias of the (single-supply) op-amp. Figure 3B graphs a typical response.

This feedback circuit worked in *Spice* simulation and when wired on the bench to control the gain of an op-amp amplifier with a resistor and 2N7000 input attenuator.² It does, however, add a second op-amp for the detector, and the bias must be adjusted below the turn-off threshold of the FET.

This later problem can be addressed by isolating the output bias from the peak detector bias, using a comparator and a reference or adding a transistor. The transistor is cheaper and is demonstrated in Figure 4. The PNP transistor acts as a diode, as in Figure 3A, while the collector allows the output bias to float. The trick here is to tie the load through a capacitor C2 to V_{CC} . Thus when the + input of the peak detector is at a larger enough minimum peak, the transistor conducts, supplying current spikes to adjust the FET bias. Once the + input of the peak detector goes high, the transistor is off, C2 recharges and the bias to the FET gate heads to ground.

While looking at this circuit with a minimalist mentality, I surmised that without any bias at the emitter of the PNP (grounding it), an ac-coupled voltage of $1.2 V_{pp}$ inserted at the base of the PNP transistor would maintain the same output bias. At each peak of the base signal, the transistor would conduct, thus providing a current spike to raise the voltage across the bias resistor. Hence, I could remove the op-amp peak detector and capacitor attached to the emitter, resulting in a total AGC system of one fixed-gain op-amp amplifier with simplified feedback circuitry, as displayed in Figure 5A. This circuit worked in *Spice* simulation and was verified on the bench.

The Final Circuit

Figure 6 displays the full AGC circuit: a fixed-gain op-amp and the control circuit of Figure 5 combined. Let's walk through it. The signal source and an optional input low-pass filter are represented at the left by V1, C7, R9 and C8. The attenuator, a simple voltage divider, is constructed using resistor R1 and an N-channel MOSFET, Q2. The linear operational preamplifier starts at C1 and produces an output at pin 1 of U1 connected to C4 and a load. The load could be a pot for volume adjustment. U1, pin1, also feeds the dc control circuit via C3, wherein the circuit flows right-to-left to denote it provides "feedback" to control the variable resistance of Q2 (the FET).

U1 and the passive components around it comprise the fixed gain amplifier. It's the tra-

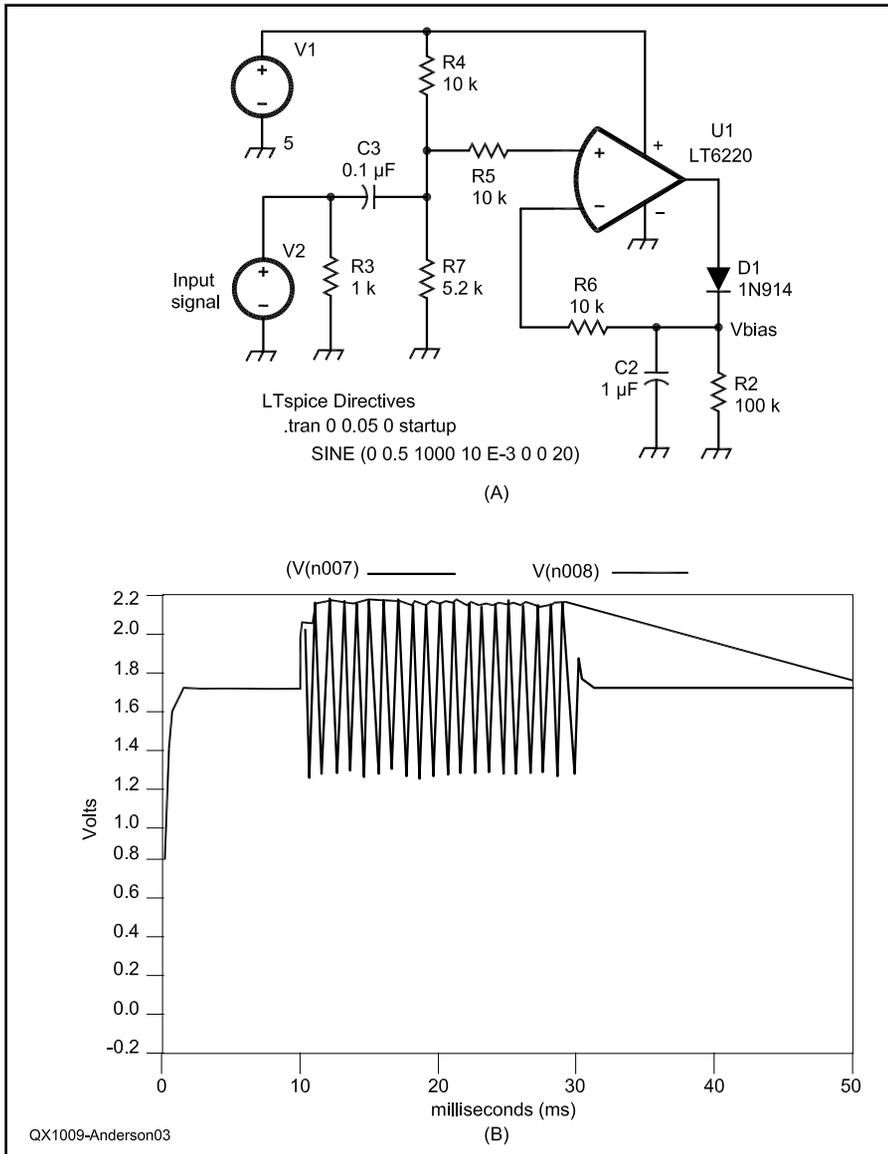


Figure 3 — Part A shows the Spice model circuit for a single-supply op-amp peak detector. Part B graphs the peak detector response.

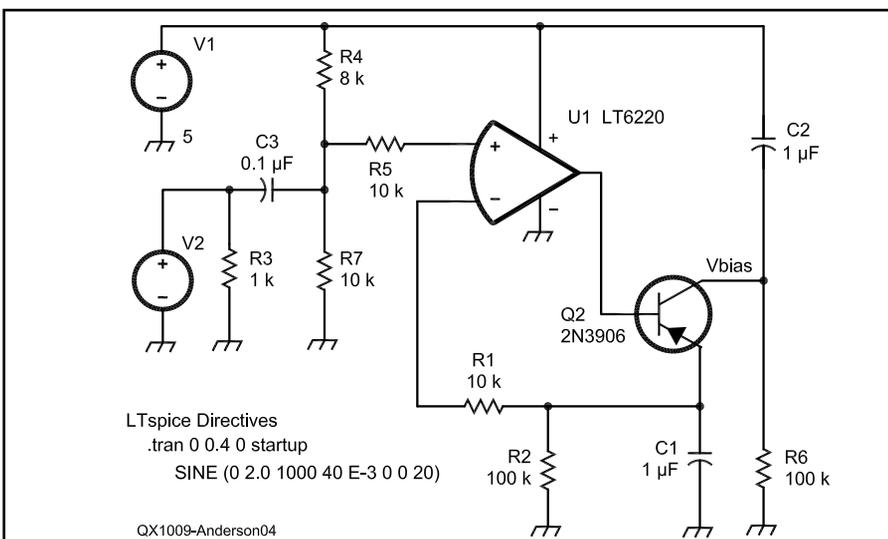


Figure 4 — This Spice model circuit is a peak detector with a floating output bias.

ditional single-supply configuration, biased by R2 and R3. C2 can be reduced to limit potential low frequency distortion below 300 Hz. The gain is set by feedback resistors R4 and R5. Open loop (no AGC) mid-frequency gain is the ratio of R5/R4 plus 1, or 48. C6 across R5 limits the high frequency gain a bit, but is usually optional. Most dual op-amp 8-pin ICs will work. I've tried the LMC662 and high speed NJM4580.

The control circuit shown at the bottom right consists of R6, Q1, R7, C5, and the FET. On power up — and with no signal input to or output from U1 — the voltage across C5 is charged (after a bit) to V_{CC} (+5 V dc), thus leaving the voltage on the gate of the FET at ground. With this gate voltage, the resistance of the FET from drain to source is several meg-ohms, basically turning off the AGC. During this time Q1 is off, too.

When a signal arrives and the output from U1 exceeds $1.2 V_{PP}$, Q1 begins to conduct when the negative peak of the ac signal at the base reaches 0.6 V, thus pulling charge away from C5 and raising the gate voltage. With a steady input signal (from V1) above $\sim 20 mV_{PP}$, the output of the op-amp preamp will be limited to about $1.2 V_{PP}$. As the output signal attempts to grow with a larger input signal, the voltage at the gate of the FET is increased, thereby offsetting the increase. The circuit holds the output signal fairly constant as the input increases over a range of better than 40 dB. A step attenuator (ref 3) fed by a signal generator with a 1 kHz to 10 kHz sine wave can be used to demonstrate the nearly constant output and increased gate voltage with an increase in input signal.³

I incorporated the circuit into the Ultra-RX2 ultrasonic receiver circuit board, shown at Figure 7. The AGC components are in the top left corner. If you try to compare the circuit schematic of Figure 6 too carefully with the board in the photo, you may find that the component designators don't match.

Since there is plenty of gain, you might consider adding this AGC circuit with pre-amp to a QRP direct conversion receiver or to a shortwave crystal radio tuner to achieve a steady volume during the reception of strong signals.

Phil Anderson, WØXI, was first licensed as a teenager in 1953 as KNØHSB. He graduated from the University of Kansas in 1963 with a BSEE, and then earned an MSEE from Syracuse University in 1967. He added a DocEng degree from the University of Kansas in 1971. He was an engineer at IBM in Poughkeepsie, NY between 1963 and 1969. Phil founded Kantronics in 1971, and retired in 2002. He founded the Xtal Set Society in 1991, and is still playing with crystal sets!

In 1969 Phil took (and passed) the Novice

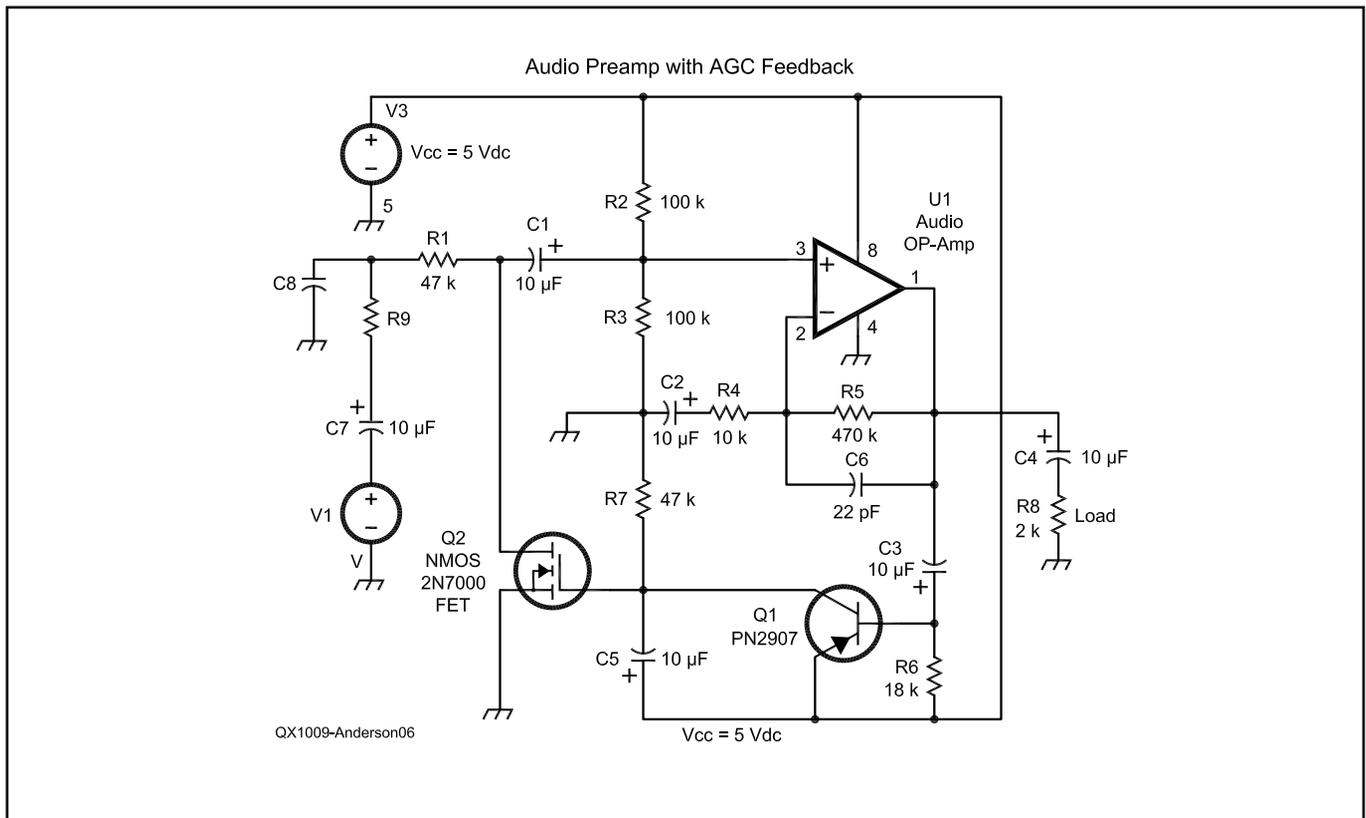
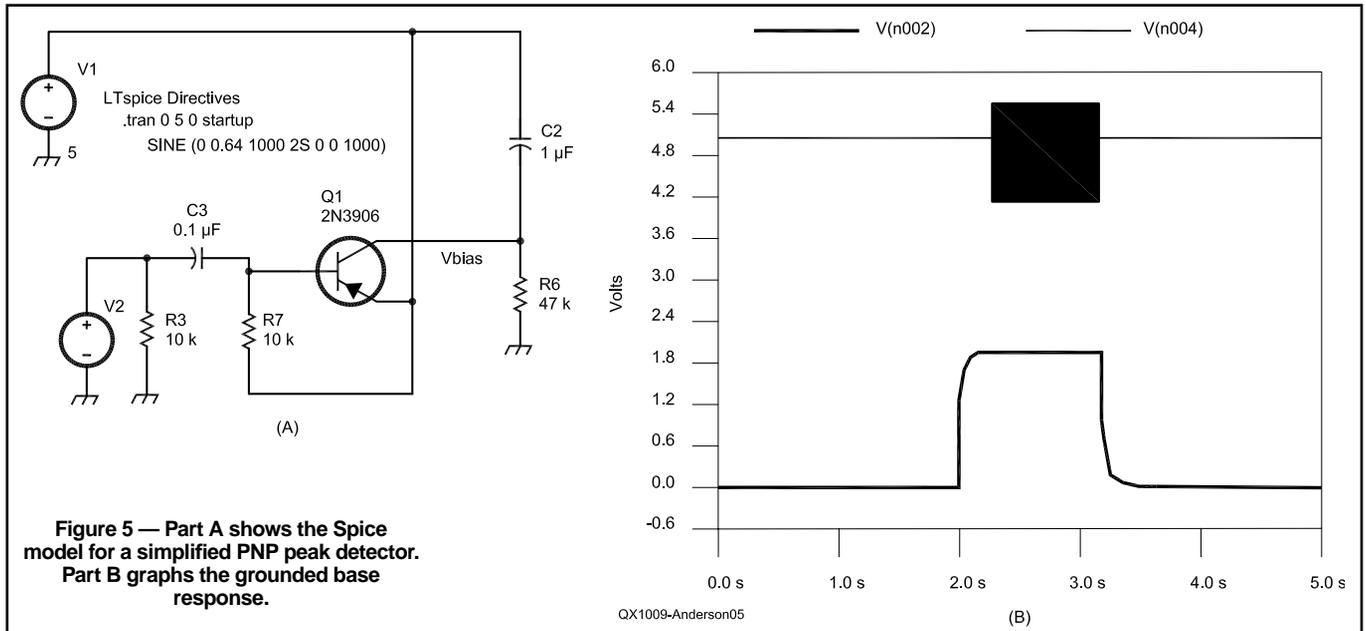




Figure 7 — The AGC circuit is incorporated into the circuit board for the Ultra-RX2 ultrasonic receiver. The AGC circuit is in the top left corner of the circuit board. Note that the component designators on the board may not match the designators on the schematic of Figure 6.

through Amateur Extra Class license exams in one sitting at the FCC Field Office in Kansas City. He is co-inventor of the GTOR communications protocol and co-designer of the Kantronics KPC-2, KPC-3, KPC-4, KPC-9612, KAM, KAM-XL and several pager controllers as well as 144, 220 and 440 MHz RF amplifiers. His current technical interests include ultrasonics, QRP, powerless devices, mm waves and radio astronomy. Phil is also a proud grandfather!

Notes

¹An op-amp Peak Detector from any op-amp circuits text, such as Howard Berlin, *Design of OP-AMP Circuits*, H. W. Sams & Co, Inc. 1977, p 113.

²LTspice, a downloadable program from Linear Technology, used to draw and simulate circuits. See www.linear.com/designtools/software/ltspice.jsp.

³The Step-Attenuator. Its use is described in "The Trap Coil Q Measurement Method Revisited," downloadable on this page: <https://www.midnightscience.com/article-index.html>.

⁴A Simple Regression calculator can be found at www.people.hofstra.edu/Stefan_Waner/realWorld/regression.html.

Attenuator Calculations

Referring to Figure 6, the attenuator is configured as a voltage divider, with R1 as the input and the resistance of the FET and bias resistors R2 and R3 in parallel as the output. Hence, the attenuation can be written as:

$$\alpha = \frac{R_{FET} \parallel R_2 \parallel R_3}{R_1 + R_{FET} \parallel R_2 \parallel R_3} \quad [\text{Eq A1}]$$

Using a curve fitting calculator such as the one found at Note 4, a first order estimate of the FET resistance can be written as:

$$R_{FET} = mX + b = -139 \text{ k}\Omega \times V_{Bias} + 335 \text{ k}\Omega \quad [\text{Eq A2}]$$

With $V_{Bias} = 2.24 \text{ V}$, then $R_{FET} = 23.64 \text{ k}\Omega$

At this operating point, with an R_{Bias} of $50 \text{ k}\Omega$, the attenuation, α , for Figure 6 is estimated as:

$$\alpha = \frac{50 \text{ k}\Omega \parallel 23.64 \text{ k}\Omega}{47 \text{ k}\Omega + 50 \text{ k}\Omega \parallel 23.64 \text{ k}\Omega} \approx 0.25$$



WB2EZG Five-Band Trap Dipole

An inspiration from 1955 yields a new design for 2010.

Can a wire antenna using only two basic traps work well over the traditional 80-10 meter amateur bands? Yes, it can, and this entirely new design, inspired by Buchanan's classic W3DZZ dipole and various succeeding configurations^{1,2} addresses the various drawbacks of the original antenna. Specifically, it ...

- Offers broad response — at least 200 kHz at 80, 20 and 10 meters and a practical bandwidth of 100 kHz on 40 and 15 meters (3:1 SWR or better, 75 Ω feed)

- Lifts the resonant frequency of the traps (more correctly, "loading elements"), usually at 7 MHz for this class of antenna, out of the band to cut power losses and trap rating requirements

- Does away with special trap arrangements and configurations, matching sections and "add-on" compensating elements

- Minimizes the time for in-the-field pruning

In answering the long-standing question of how well a no-frills two-trap dipole is suited to five-band operation in practical applications, we turn directly to some basic math as opposed to a largely cut-and-try approach. Here we solve a set of transmission-stub equations to quickly approximate antenna length, inductance and capacitance of the loading elements, and the position of the loading elements along the flat top. This antenna is a bit longer than the original two-trap dipole. On the other hand, it's a repeatable design (which is intended for use with transmitters having built-in capability to match to a fairly wide range of loads) that allows users to customize band coverage to a fair degree by simply adjusting the length of the flat top.

The Top-Down Approach

The W3DZZ's signature configuration centers on the 40-meter band; i.e., two traps tuned to 7 MHz or so that are placed at each end of a center-fed wire about 65 feet long with the antenna having a total length of about 110 feet. That antenna is designed to

work as essentially a half-wave dipole on 80 and 40 meters, three-half waves on 20, five-half waves on 15, and seven-half waves on 10. In practice, the W3DZZ can be made to work over two bands without much difficulty and three bands with a bit of cut-and-try. Adjusting the antenna to work on four bands is significantly more difficult, however, and five bands present the ultimate challenge. It's a familiar problem to those experienced

with the 5-band trap dipole and various antenna analysis programs that approximate its overall performance, such as EZNEC. Experimentally and from EZNEC analysis, the stated SWR characteristics for the original 5-band trap design are somewhat optimistic, particularly at the higher frequencies.³

The success of the new design (Figure 1) springs from a top-down approach, i.e., focused on the highest frequency of opera-

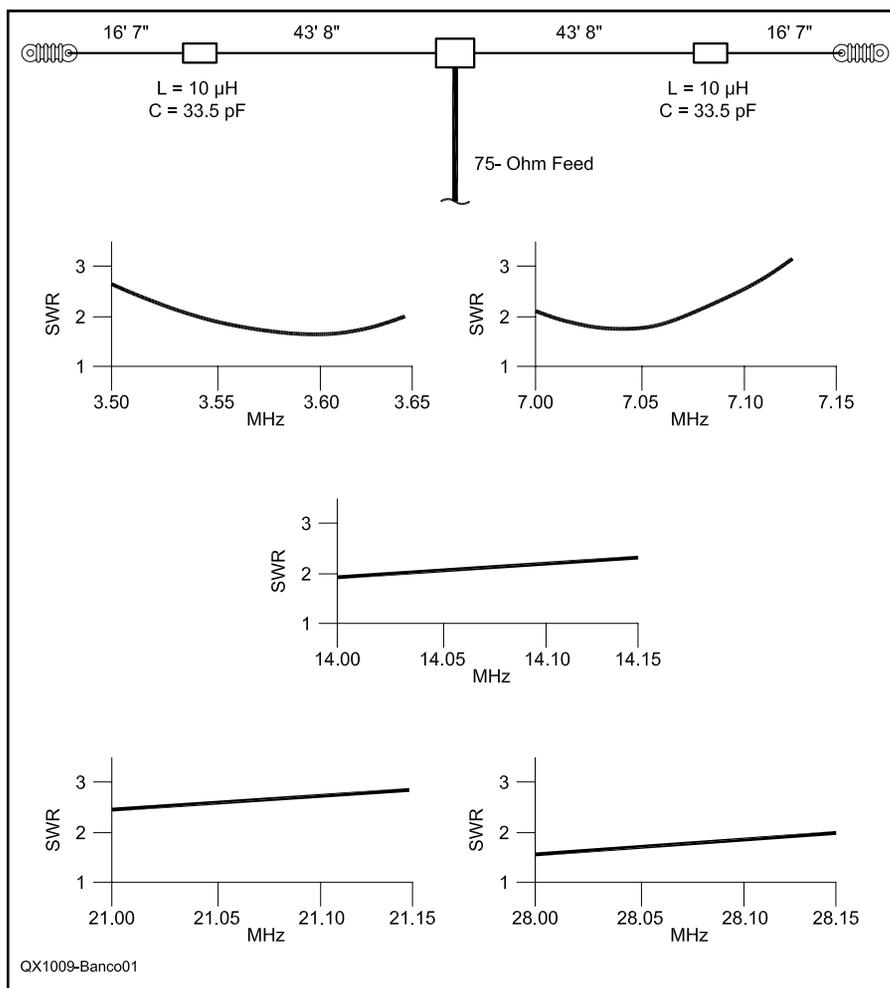


Figure 1 — Configuration and SWR curves for one solution of the WB2EZG five-band dipole at 28 feet, as tweaked for the CW bands. SWR measured at the transmitter end of an 85-foot section of RG-6 coax (Commscope F677TSVV).

¹Notes appear on page 31.

tion. The antenna has a physical length that's resonant at the highest frequency of operation (28 MHz). That's a bit more than 120 feet. Indeed, operation at 28 MHz in a traditional two-trap design isn't otherwise easily secured with a shorter antenna, given the fixed placement and component values of the L and C elements.

Moreover, the values of L and C used in a traditional trap-dipole have little effect on antenna response at 10 meters. Not surprisingly, the math confirms our practical experience and tells us the length of the antenna should be essentially 7/2-waves at 28 MHz. The new antenna's comparative band-to-band response, versus that of many previous trap designs, is relatively insensitive to small changes in antenna length and the exact placement of the loading elements — issues that usually create insurmountable tuning difficulties in a traditional trap dipole as the designer struggles to redress the resonance requirements for each band simultaneously. The main operating tradeoff with the new antenna is a bit less bandwidth on 40 meters.

Developing the “Harmonic” Equations

Let's see what our basic math says. The current-distribution along an antenna's flat top has the same general characteristic as a transmission line with standing waves. The impedance distribution for both is much the same, too. In essence, we view the flat top as an approximate extension of a transmission line.

Thus, we model the antenna as a shorted section of transmission line extending from the antenna's feed point to the traps (we consider the relatively low-impedance feed point as the “shorted” end), and as an open stub that extends from the traps to the antenna's end insulators. From this analysis we determine the values of L and C per trap that, when placed as lumped circuit elements at a point where the stubs converge, provide the proper reactance to ideally resonate the wire ($X = 0$) at each of five spot frequencies.

Each of the antenna's parallel LC networks has extremely high inductive reactance immediately to the low side of its resonant frequency, and the reactance falls off exponentially thereafter. Similarly, the LC networks provide high capacitive reactance immediately to the high side of resonance, and reactance falls off exponentially as frequency increases. The impedance of the ideal LC network is:

$$Z_1 = \frac{-jX_c jX_L}{j(X_L - X_c)} = \frac{-j2\pi fL}{4\pi^2 f^2 LC - 1}$$

Now the impedance along the antenna's flat top, which we, again, view as a transmission line, is:

$$Z_2 = c_w j(\tan \theta_1 - \cot \theta_2)$$

where $c_w = 138 \log 4d/h$ represents the characteristic (resistive) impedance of a single wire over earth; d is the diameter of the wire; h (in the same units as d) is its height above ground, and θ_1 and θ_2 is the line length in electrical degrees (alternatively, expressed in radians). Thus, the reactance of a shorted line section extending from the feed point to the trap is $c_w j \tan \theta_1 = c_w j \tan (2\pi l_1/\lambda)$, where the sign of the reactance changes as l_1 goes through every quarter-wavelength point. Similarly, $-c_w j \cot \theta_2 = -c_w j \cot (2\pi l_2/\lambda)$ is the reactance of an open stub section extending from trap to end insulator. Now $l_1 + l_2$ is the length of one side of the dipole; and λ is the wavelength of operation.

For a given frequency and placement of loading element Z_1 on the flat top, we expect $Z_1 + Z_2 = 0$ in order to cancel the reactive component of impedance along the wire. Combining and rearranging the equations for Z_1 and Z_2 , we get:

$$j2\pi fL = (4\pi^2 f^2 LC - 1) c_w j(\tan \theta_1 - \cot \theta_2)$$

or

$$\left(2\pi fC - \frac{1}{2\pi fL} \right) c_w (\tan \theta_1 - \cot \theta_2) = 1$$

Solving the Equation Set

For a fixed-length section of line measuring $l_1 + l_2$, electrical lengths θ_1 and θ_2 ideally vary directly as an integer multiple of the frequency of operation. As a result, θ_1 and θ_2 are basically twice their values at 7 MHz as at 3.5 MHz, four times their values at 14 MHz, six times at 21 MHz and eight times at 28 MHz. Thus we expand the equation above to the following five-band equation set to determine L , C , θ_1 , and θ_2 :

$$(k_1 C - k_2/L) c_w (\tan \theta_1 - \cot \theta_2) = 1$$

$$(k_3 C - k_4/L) c_w (\tan 2\theta_1 - \cot 2\theta_2) = 1$$

$$(k_5 C - k_6/L) c_w (\tan 4\theta_1 - \cot 4\theta_2) = 1$$

$$(k_7 C - k_8/L) c_w (\tan 6\theta_1 - \cot 6\theta_2) = 1$$

$$(k_9 C - k_{10}/L) c_w (\tan 8\theta_1 - \cot 8\theta_2) = 1$$

...where $k_m = 2\pi f_m (10^\circ)$ and $f_1 = 3.5$, $f_3 = 7$, $f_5 = 14$, $f_7 = 21$, and $f_9 = 28$ MHz (for $m = 1, 3, 5, 7, 9$); and $k_n = 1/2\pi f_n (10^\circ)$ for $n = 2, 4, 6, 8, 10$, and $m = 1, 3, 5, 7$ and 9 , respectively.

We have four unknowns (L , C , θ_1 , θ_2) in five nonlinear equations, which implies one redundant equation, assuming the set has a solution. To more rigorously examine the system solution, we add a “pseudo unknown,” E , to establish an equation set having five unknowns in five equations.

For simplicity, we introduce E into the first equation — the equation having the sim-

plest form (i.e., basic single-angle tangent and cotangent functions, where E is likely to have the least complicating effect). Thus the new term to the right of the equal sign in the first equation becomes $(1 + E)$. Ideally, we expect $E = 0$.

Next, we set the limits of our search to a practical antenna length. It's the shortest length that's likely to yield a viable design. We expect the length to be somewhat greater than 110 feet (the original length of the W3DZZ trap dipole). At the other end, we limit the maximum flat top length to less than a half wave at 3.5 MHz (approximately 135 feet) for minimizing the antenna's physical size. Thus the maximum allowable value of $(l_1 + l_2)/\lambda$ is equal to 0.25 (i.e., the maximum value for $l_1 + l_2$ is one-half of 135 feet = 0.25 wavelength at 3.5 MHz). We thus set the search for L and C for a maximum limiting length of $\theta_1 + \theta_2 = 1.57$ radians (i.e., $\theta_1 + \theta_2 = 2\pi (0.25) = 90 \text{ degrees} = 1.57 \text{ radians}$).

The harmonic nature of the trigonometric equation set initially suggests we can solve it by hand, making use of multiple-angle substitution techniques. But it's a time-consuming task too tedious for most mathematicians. Thus we turn to numerical computation software, in this case *Systems of Nonlinear Equations v.1* (the vendor is Numerical Mathematics) for the answer.

Results

The output of the 5-by-5 analysis, for four values of c_w and consistent with finding the lowest value of $(\theta_1 + \theta_2)$ in the interval $1.28 < (\theta_1 + \theta_2) < 1.57$ (where 1.28 radians corresponds to a physical antenna length of ~110/2 feet for the W3DZZ antenna), is shown in Table 1. The cut-and-try solutions provided by *EZNEC*, each using the initial parameters provided by the 5-by-5 analyses, fairly confirm the solution delivered by the numerical software (the first *EZNEC* solution is suited to large-diameter wire and “tape measure” designs; the others are optimized for 12-14 gauge wire). *EZNEC*'s calculation of SWR at the feed point across each band is consistent with the actual SWR measured at the input of the transmission line (which as expected will be slightly lower in most cases). It's also consistent with the results provided by W9CF's transmission-line calculator.⁴ Here in Table 1 l_1 and l_2 are the trap positions expressed as a percentage from one end of the total flat top length, and h_{opt} is the approximate height above ground (feet) that will provide the aforementioned response over five bands. Note the percentage difference in the results of the 5-by-5 analyses, versus *EZNEC*, is a function of c_w .

The numerical software computes $E = 0.63$ for the quasi-unknown variable. Thus there is no exact solution to our original equa-

Table 1

Results of the five-by-five equation set analysis and EZNEC, which are in fairly good agreement for the values and positioning of the LC loading elements, suggest a much more flexible design than the traditional trap dipole.

5-by-5 Analysis				EZNEC				
$L(H)$	$C(pF)$	c_w	l_{tot}	$L(H)$	$C(pF)$	$l_1, l_2 (%)$	l_{tot}	h_{opt}
9.8	37	450	118.1	8.9	40	13.0, 87.0	122.0	35
11.7	31	535	118.1	10.8	34	14.4, 85.6	121.1	30
12.6	29	575	118.1	10.2	35	13.8, 86.2	121.6	35
13.1	27	600	118.1	10.8	34	13.3, 86.7	121.7	35

tion set. But the result for E bears little significance in the final analysis. That is, many of the 4-by-4 equation sets for this antenna converge towards the same numbers for L , C , θ_1 , and θ_2 provided by a rigorous 5-by-5 test.

As expected, the computed values for L and C are a function of c_w . However, the calculated lengths l_1 and l_2 essentially remain the same (θ_1 and θ_2 are 0.993, and 0.381 radians, respectively) over the c_w range. But we do not consider c_w a practical design variable as it relates to the actual impedance of a flat top over ground, and instead look upon L and C over the range of c_w as a fairly small collection of values that we can apply to secure fairly good (i.e., perhaps less than fully optimized) response for five-band operation. In that context, the SWR at the *feed point* in a less than fully optimized design can exceed 3:1 at 15 meters—but it's of scant consequence when it comes to performance over your favorite 100 kHz band segment.

Disregarding 10 meters, there's a nearly linear relationship between the required reactance provided by the loading elements on a given band, versus the difference between the antenna's multiwave resonant length required for that band and the actual wire length. Such a response suggests we can customize band-to-band coverage both gradually and monotonically (although not linearly) simply by adjusting the physical length of the antenna, and this is indeed the case. The ability to tune is not unique to a multiband trap design (especially where we employ loading elements, versus "traps"), and has been demonstrated previously.⁵

Practical Installation

Figure 1, a design for the CW bands, shows one solution for the new 5-band dipole, this one using components on hand to demonstrate the design's flexibility. Antenna pruning for your particular installation should require no more than a few iterations. Place the antenna (#14 bare wire, solid copper) between two supports such that the dipole's center is at least 15 feet above ground. Then resonate the flat top to the lower end of 28 MHz. Use components within the range of values indicated in Table 1 (in this case, an inductance of 10 μH and an

air variable capacitor for each trap, and insert them between 13 and 14 percent from each end of the ~121-foot flat top). Install suitable insulators at these points for wire support and to allow adjustment of wire lengths as well as for easy attachment and removal of the traps in the pruning process. The LC components are housed in a pop-open plastic enclosure measuring approximately 1.75-by-2.5-by-5 inches for protection from the weather.

Adjust the trap capacitance and wire lengths as required (take care to ensure symmetry on each side of the dipole) for the lowest SWR on each band. A choke balun should be installed at the feed point. Slip twelve F-50B toroid cores (Palomar Engineers) over your 75- Ω feed line before making measurements. Apply heat shrink tubing to keep the cores in place. This antenna is fed by RG-6 cable (Commscope F677TSVV).

Your adjustment of wire dimensions and C for a given inductance will be approaching the sweet spot once you secure a monotonic increase, or decrease in the optimum frequency on all bands by cutting wire from, or adding to, the length of the outer portion of

the antenna's flat top. You may find it more effective to cut or add from both the inner and outer sections of the flat top. For best results, maintain each "trap" at from 13 to 14 percent from each end of the flat top.

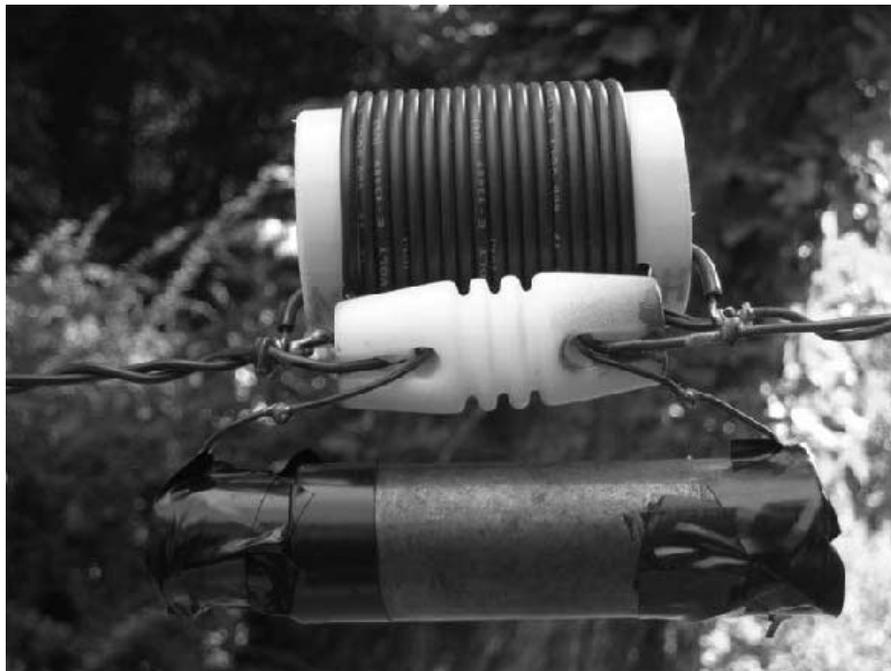
Performance

This antenna has performed well over several seasons and fairly harsh environmental conditions with no basic changes in trap characteristics. Fixed-value transmitting mica capacitors or your homebrew alternative might serve better than the typical close-spaced, transmitting air variable to maintain antenna characteristics and allow high-power operation as well. Fixed-value transmitting ceramic caps, if used, might best be suited to moderate climates where there's no great swings in seasonal temperatures or environmental conditions. Transmitter loading is extremely smooth on 80 through 10. Given the right conditions, you'll be able to hear and work DX on all bands with this antenna using relatively low power (100 W), even in the occasional pileup.



One of the original traps used with this antenna. It is comprised of a 10 μH B&W miniductor coil and a Johnson 158-5-23 air variable capacitor set to 33.5 pF.

A more robust trap made in the true Amateur Radio spirit – using whatever was on hand! The 2-inch diameter coil is constructed from 16-gauge insulated wire to provide about 10.8 μH . The capacitor consists of two sections of copper tubing, a 3/4-inch diameter section placed within a 1-inch diameter section and adjusted to yield a capacitance of about 31.3 pF.



Acknowledgement

Thanks are due Scott Leyshon, WA2EQF, who devised and installed an “on-the-fly” test system for quickly tweaking antenna parameters.

Notes

¹Buchanan, W3DZZ, “The Multimatch Antenna System,” QST, Mar 1955, pp 22-23, 130.

²The ARRL Antenna Book, ARRL Publications, 19th edition, pp 7-7 to 7-13.

³The ARRL Antenna Book, ARRL Publications, 19th edition, p 7-10.

⁴See <http://fermi.la.asu.edu/w9cf/tran/>

⁵Johns, W3JIP, “Dual-Frequency Antenna Traps,” QST, Nov 1983, pp 27-30.

Vincent Biancomano, with experience in electrical engineering and meteorology, started out at Bell Laboratories in the late 1960s. His first technical article for QST was in 1972 on the subject of speech recognition. Biancomano has served at every editorial level for more than 30 years in the electronics trade journal business for Electronics, Electronic Design, EE Times, Energy Efficiency & Technology, Fiberoptic Product News, and various IEEE magazines. He's a member of IEEE, the American Meteorological Society and the National Weather Association.

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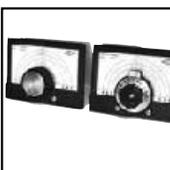
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A Simple and Effective RF Power Reference

How to harmonize the readings of all the power meters in a homebrewer's ham shack.

Everything started when, several years ago, I bought my first HP432A power meter. After a while I suspected that the bolometer was not right, so I bought a second bolometer, and then a third bolometer with waveguide flange (a good bargain). Then I bought a second HP 432 (another good bargain, I can't resist!). I built two power meters with the AD8307, and then an AD8362 power meter. My last purchase was a spectrum analyzer together with a set of some diode detectors of various brands.

Everything was fine, but all of them indicated measured power with a little bit of a difference. Initially this was within my measurement limits, but later on it became disturbing. Where was the true value? I needed a standard reference, not so much for spotting 0.01dBm, but to have a common reference and at least always have the same error. I thought to buy a power meter (HP435) to use only the calibrator, but it seemed to be using "a gun to kill a fly". And, besides NIST, who can guarantee that an instrument

fifteen years old is still calibrated?

I found a paper by Paul Wade, W1GHZ, for a little RF power reference based on a 50 MHz TTL quartz oscillator. It is a good idea indeed.¹ It gave me some good hints, but still looked a bit too simplistic: amplitude was just controlled by two back to back diodes. I started thinking of a feedback circuit comparing the RF output to a stabilized reference. To do this I considered controlling

¹Notes appear on page 34.

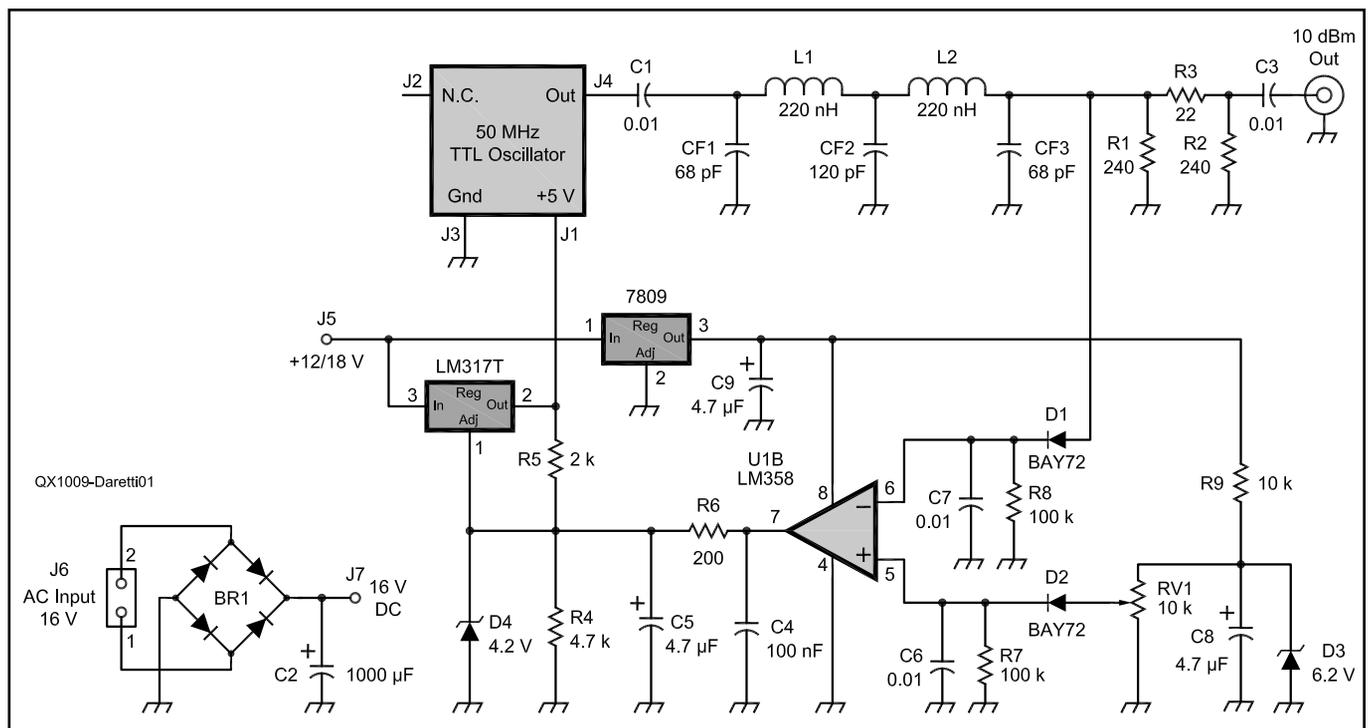


Figure 1 — Schematic diagram.

the output with a variable PIN diode attenuator driven by the feedback loop. However, a PIN diode for 50 MHz was not in my drawers (today it is more a “trunk” than a drawer).

So I changed my mind, and got the idea to control oscillator amplitude (i.e. power) by controlling the power supply. I started designing a detector to control the adjustable output of a LM317 to drive the oscillator power. I had some 50 MHz TTL oscillators recovered from scrap PC boards and started testing. Output was a bit less than the V_{CC} (around 5 V) and the waveform was about square, becoming more sinusoidal once loaded to 50 Ω . Suitable supply was between 4.2V to over 6V.

The surprise comes from output impedance measurement: it was everything from 25 to 200 Ω . The measurement method I used is to measure V_{out} (on open) and V_{out} (on 50 Ω). The ratio (V_{out} open / V_{out} on 50 Ω) = 2 suggests R_{out} = 50 Ω . There is nothing wrong with a different output impedance except that the following low pass filter should be designed with proper input and output impedance. That suggested to me to avoid this critical parameter.

The following low pass filter is quite important in order to have as pure a sine wave as possible. In fact in the presence of harmonics and non sinusoidal waveforms, the concept of “power” becomes more complex. The filter, designed with *ELSIE*, is a Chebyshev Low Pass 5th order with capacitive input.² *ELSIE* has also calculated the two air inductors, as 5 mm diameter, 10 mm long, 9 turns.

Right after the filter is the detector for the feedback loop. It is a straightforward design, and the output connects to the inverting input of an LM358 op amp supplied by a 7809 9V regulator. The non-inverting input is fed by an identical diode supplied by stabilized DC. The reason for that is so that the two diodes are exposed to the same thermal stress and deviations. In that way the two diodes track each other. The type of diode is not critical, but they must be the same type number. It is even better if they are a matched pair. The DC supplied to the non-inverting diode is stabilized by a 6.2 V zener diode. The associated variable resistor is used to trim power output. A 3.6 dB pi attenuator follows the filter to terminate the filter and isolate it from load variances. The output provides a stable 10 dBm signal.

How the Design Works

First we select a suitable V_{CC} for the oscillator. I selected 4.7V as a good compromise. I thought it was a higher probability to increase rather than reduce power (so we increase V_{CC} rather than reduce it). With this V_{CC} , the power output was 13.6 dBm right after the filter. Consequently I designed the attenuator

for 3.6 dB which gives a set of resistors of 240, 22 and 240 Ω and gave an output of 10 dBm. The output can be trimmed with the variable trimmer if necessary.

The output from the LM 358 goes to the “Adjust” pin of the LM 317. There is a RC low pass filter between the LM358 and LM317 which is mandatory as without it the closed loop tends to oscillate heavily. The “Adjust” pin voltage is set with two resistors to 4.2 V with no feedback signal. There is also a 4.7 V Zener diode protecting the LM317 in case of a short circuit in the output causing the feedback signal to jump up to 9 V destroying the oscillator (it has happened to me!).

I built the circuit on a PCB with SMD components. It could just as easily have been

a through-hole design, though. Figure 1 is the schematic of the circuit. Figure 2 shows a picture of the bottom of the completed board inside of the metal enclosure. It is important to pick a well shielded box to assure a clean output signal. Figure 3 shows the completed system with the cover in place and Figure 4 shows a spectrum plot of the output.

Figure 5 shows the bottom copper. Figure 6 shows the top silk screen and PCB pattern.

Building and Testing

I started the project by first putting the oscillator in place on a socket (taken in and out often for testing). Then I measured the output impedance as previously described. Replacing it for any reason is easy because of

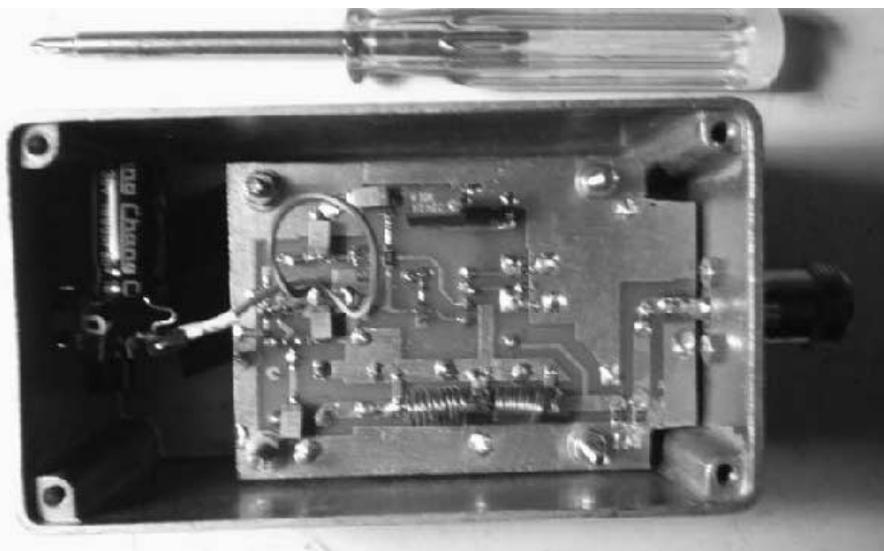


Figure 2 — Inside the box. You can see the two inductors and the variable pot. The oscillator is on the other (component) side.

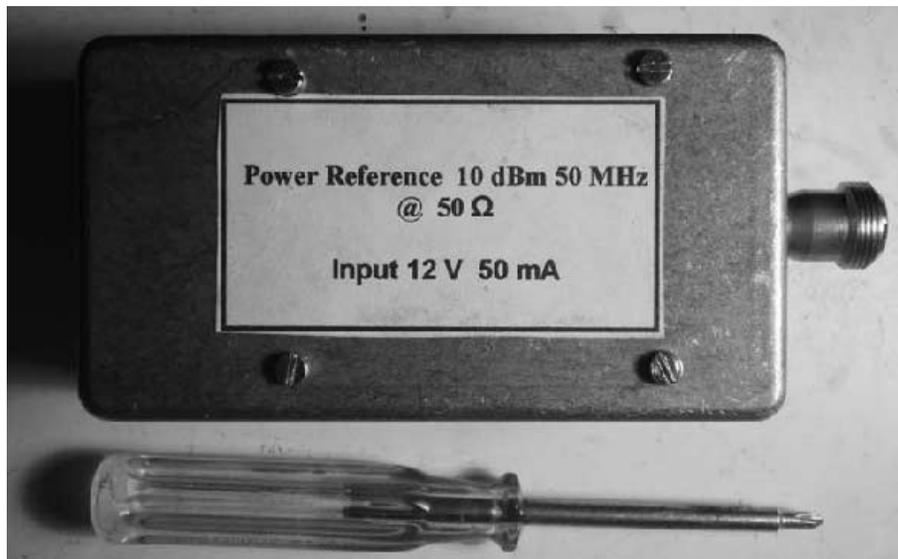


Figure 3 — The completed system.

the socket. Then I made the 50 MHz filter. By squeezing and pulling a bit on the inductors I optimized the output, with the output temporarily connected to a 50 Ω resistor. With a 50 Ω load and V_{CC} at 4.7V, I measured the power output as precisely as I could. I had to invent the most precise method available to my tools to measure power. The key was a friend's loan of a digital oscilloscope with the ability to measure V_{RMS} with four digits at 50 MHz.

So, in that configuration (open feedback loop, filter connected to 50 Ω) I measured 1.07 V_{RMS} at 50 MHz out of the filter. That is 13.6 dBm so the attenuator was designed for 3.6 dB. If you have access to more reliable methods, the trimmer allows you to accurately set the output power.

I closed the loop by soldering the last components in place and set the trimmer to have 4.7V at the oscillator V_{CC} . It was exciting to check the loop with my finger touching the PCB track right before the attenuator and see the oscillator V_{CC} jump up because of my finger absorption. The output level remained stable.

Now, finally, I have a tool to calibrate all of my power measurement systems or at least set them all with the same error!

A Warning on Use

This little instrument is designed to deliver 10 dBm to a 50 Ω load only. That is enough in most cases. Adding more attenuation to reduce power will reduce any impedance mismatch at the filter output and control point. If you connect it to a different load (such as 75 Ω) it will not deliver 10 dBm! [A 75 Ω load will yield a reading that is 1.5 dB high. A minimum loss attenuator for 50/75 Ω matching will add 5.7 dB loss, but yield an exact reading.—Ed.]

Notes

¹Paul Wade, W1GHZ, Web site: www.w1ghz.org/.

²Jim Tonne, Tonesoftware ELSIE filter design program: www.tonesoftware.com/. ELSIE is also included on the CD that is included with the 2010 ARRL Handbook.

Andrea Daretti, IZ2OUK, holds an MSE from the University of Rome, Italy. He worked for 30 years for HP, first in the Medical Product Group, and later in the Computer Group in the US, Germany and Italy. After HP he became an IT consultant for Public Administration in Italy for several years. Once retired he could spend his time on his hobbies: electronics and open air activity. Being an active homebrewer, his interest is recently biased toward radio astronomy and micro-waves.

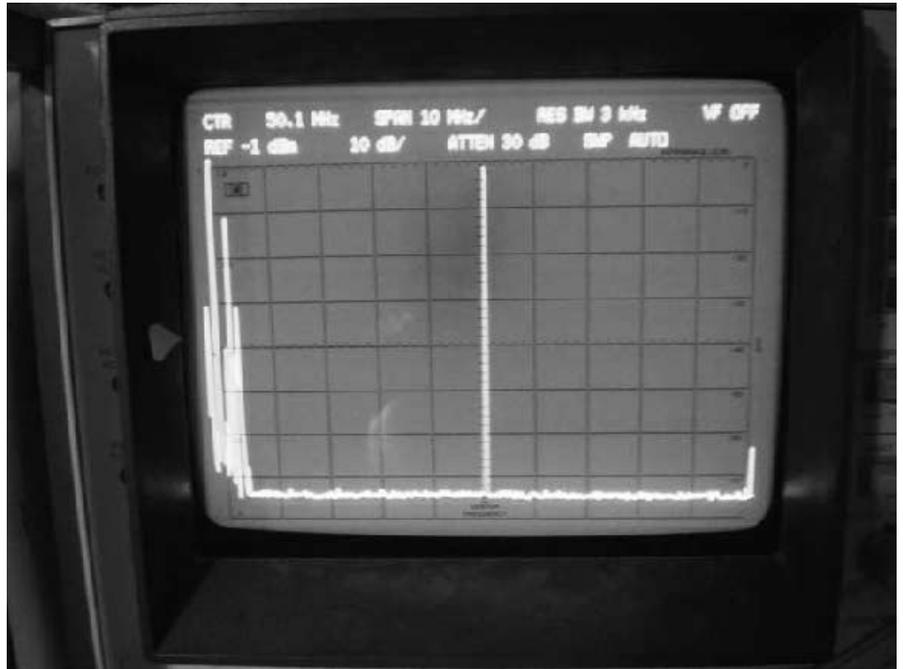
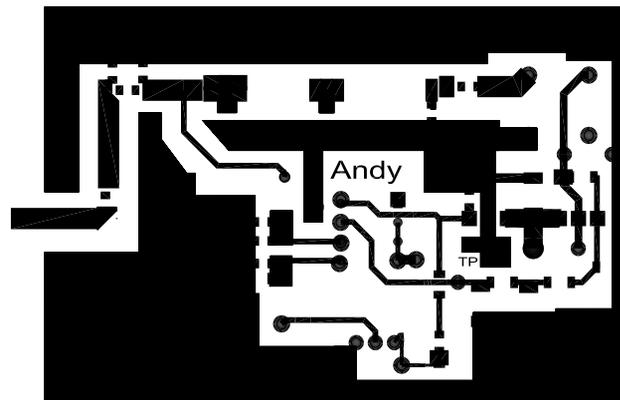
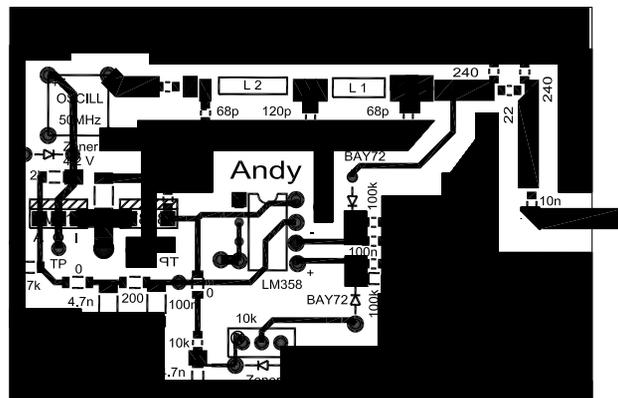


Figure 4 — Measured output of the filter. The good result is because the output is a very good sinusoid with 50 Ω load.



QX1009-Daretti05

Figure 5 — Board layout.



QX1009-Daretti06

Figure 6 — Component placement.



A New Tune for the Loop

Here's an interesting approach to ferrite rod variable-inductance tuning for low power transmitting loops.

Effective multiband antennas don't come any smaller than the magnetic loop. Building one at home makes an attractive project, but the tuning arrangements and metalwork can be challenging. This loop is designed for low-power (QRP) transceivers. It offers a new approach and is straightforward to make.

The schematic for a typical conventional magnetic loop is shown in Figure 1(A). A loop less than $1/4$ th wavelength in circumference is fed with a gamma match. It is tuned at the high voltage end of the circuit with a capacitor that should ideally be of the vacuum variable type. A reduction drive is often fitted, as the Q is extremely high. You need an extension spindle if the capacitor has to be adjusted by hand, both for safety and to avoid affecting the resonance of the loop. All this can make for a cumbersome and physically fragile assembly, unsuitable for portable operation.

If we could alter the resonance of the loop by varying its inductance, then instead of a variable capacitor we could use a preset or even a fixed type. The loop shown in Figure 1(B), does exactly that. It is tuned by moving a ferrite rod within a small two-turn coil in continuity with the loop at the feed point. The capacitor is a fixed one, chosen for the frequency range required, avoiding the need for any manual adjustment at the high voltage part of the circuit. The photograph (Figure 2) shows homemade capacitors that permit multi-band operation from 3.5 up to 24MHz.

This system also allows a simple way of coupling the loop to a $50\ \Omega$ coax feed line. The traditional gamma match has a sliding contact from the coax inner core that is moved outwards from the zero potential until a match is obtained. In the present case this is unnecessary. A match can be achieved by connecting the coax braid to the center of the two-turn coil (the zero-potential point), and the center conductor to an end of the

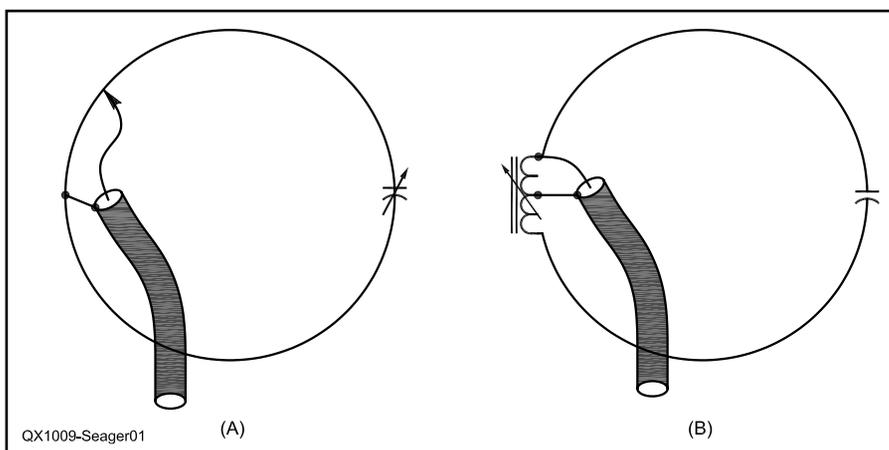
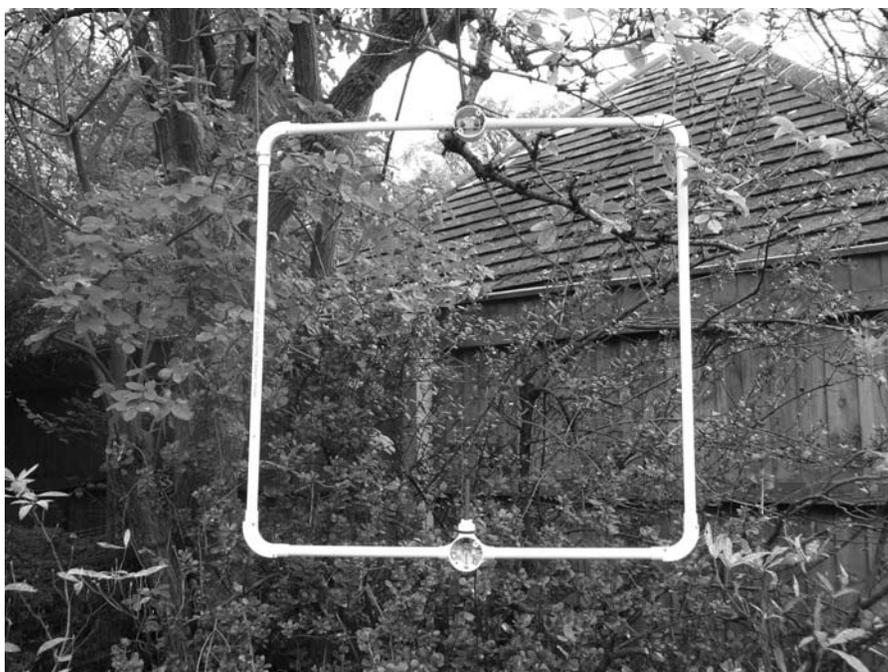


Figure 1 — Figure 1A shows a typical magnetic loop with a gamma match and a variable capacitor. At B we have a variable inductance loop with a fixed capacitor.

coil where it joins a main element of the loop.

This could be seen as an autotransformer or as a gamma match with part of the coil taking the place of the usual sector of loop circumference. If preferred, the loop can also be fed by way of an inductive coupling. It will be found that only two turns are needed for this matching transformer. Both coupling systems can be built in if each is brought out to a separate coax connector.

Putting it Together

I chose to make the elements out of thin copper tapes. These are very light but need support and so I built the loop out of PVC conduit. Any other form of loop would be suitable including the traditional solid copper tube, but the PVC T box connector shown in Figure 3 is easy to work with and the whole structure is light and generally escapes injury even if dropped.

A ferrite rod of the type used in old AM portable receivers is fitted into a cup made from a rubber cable protector, or the plastic from a clip cover with a 2 inch (50 mm) long $\frac{3}{16}$ inch (3.5 mm) diameter bolt threaded through and secured with a nut. If it is not firm, a drop of super glue helps. The end of the bolt passes through a 3.5 mm jack socket that grips it quite well. The rod can be steadied at the open end of the T box with a suitably modified cap from a hand wash bottle. A two turn $\frac{3}{4}$ inch (2 cm) diameter coil is connected between the two elements of the loop. The midpoint of this coil was the ground point for the gamma match. In the photograph a wire can just be seen connecting this point to the outer (braid) connector of the coax socket. As this is a low-power antenna I used phono sockets, but others may prefer to use a lower loss type. The connection to the center conductor of the coax was soldered to a loop element where it is joined to the coil. (Either end will do).

The second coil is a simple coupling coil. Because the ferrite rod passes through this first (increasing the inductance as it goes) only two turns are required. The elements for the magnetic loop were two double lengths of approximately $1\frac{1}{4}$ inch (3 cm) wide copper "slug tape" obtained from a garden center. Due to the skin effect for radio-frequency current flow they should together be roughly equivalent to a tube $\frac{3}{4}$ inches (1.9 cm) in diameter. In one version I also added lengths of coaxial cable with the center conductor and braid soldered together at the ends to further increase the effective diameter and reduce the conductive resistance. I have made a square loop using conduit elbows at the corners and a (more or less) circular one in which I bent the PVC.¹

The square loop was made from $\frac{3}{4}$ -inch (2 mm) conduit with 33-inch (84 cm) sides joined with PVC inspection bends – curved sections of PVC with removable covers. The circular loop was of 1 inch (2.5 cm)

conduit, with a diameter of $3\frac{1}{2}$ inches (1 meter). In both loops the fixed capacitor was mounted between two brass terminals in a PVC "through box" (Figure 4) exactly opposite the T box housing the ferrite tuning

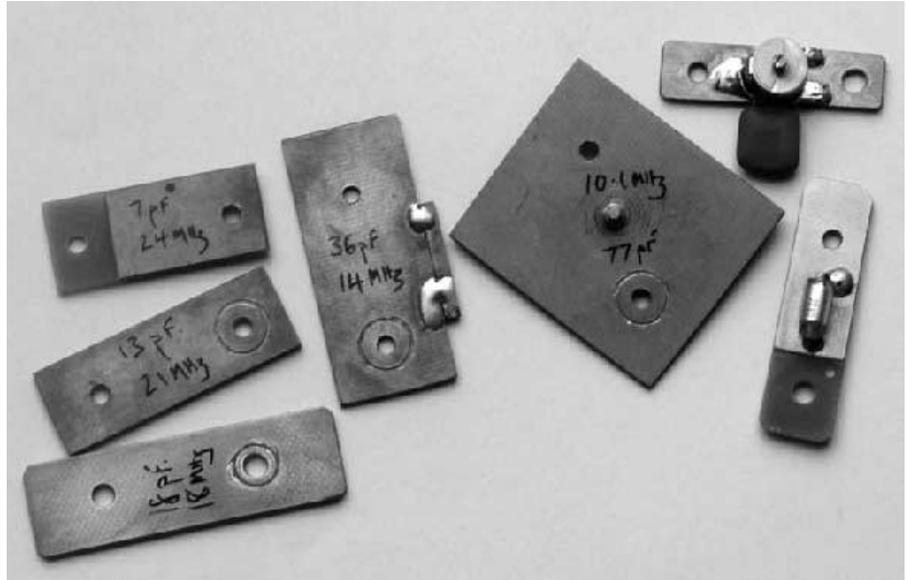


Figure 2 — A variety of homemade and other capacitors to allow multi-band operation.



Figure 3 — PVC T box showing the adjustable ferrite rod and the coil in series with loop elements. The coil on right is an inductive coupling

¹Notes appear on page 37.

assembly. All joints were secured with PVC cement on completion.

In this budget loop the only extravagance was in purchasing the copper tape and the use of silver solder, both justified by the need to minimize losses. Some of the capacitors can be custom made entirely at home from double sided fiberglass copper board. The value needed for each band was found by substituting a large variable capacitor across the element terminals. The capacitance was noted at each required resonant point, using a low power signal source and a directional power meter. Capacitors were then fashioned as shown (Figure 2). Copper board is readily cut to size if you measure the capacitance per area for the thickness you are using. If you go too far you can always solder a few pF back on the edge! On the lower bands a combination of capacitors and preset trimmers will be needed to achieve about 150 pF for 7 MHz and 680 pF for 3.5 MHz. Be aware, though, that voltages in small loops are high and inadequate capacitor insulation may arc over.

With an appropriate fixed capacitor in place, the inductive tuning arrangement gave full coverage of the CW end of each band. Separate capacitors were needed for the upper (SSB) sections on 14 MHz and below.

Setting Up

Other than the fact that tuning is done with the ferrite rod instead of a variable capacitor, the procedure for setting up the antenna is the same as with a conventional loop. The feeder can be any length of 50 Ω coax. To keep weight down in what can be a useful portable antenna I use 12 feet (4 m) of RG-174. The antenna is kept within easy reach of the operator so it seems sensible to restrict power output to 5 W or so. At this level I have noticed no warming effect on the ferrite rod.

The coax lead is coupled via a bidirectional power meter to the transceiver and with power at a minimum the ferrite rod is rotated until a dip is seen on the meter. It will be found that if the jack socket spring contact is slightly crimped the bolt will track with almost micrometer precision and keep its position well. It is always possible to get a 1:1 match to a 50 Ω output, if not with the preferred gamma match, then with the inductive coupler.

Results

Subjective impressions are that this loop operates in much the same league as other magnetic loops. As with all loops it needs to be retuned when its height above ground or proximity to other objects is altered. Tuning is extremely smooth, with no hand capacitance effect even when touching the ferrite rod. The fun of making contacts with small

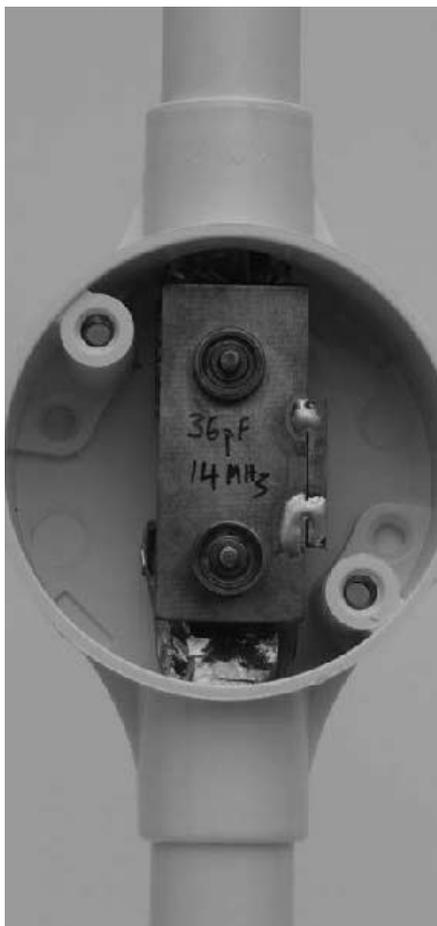


Figure 4 — A capacitor (for the CW end of 20 meters) mounted in the PVC “through box.”

antennas and low power is well worth the effort.

Magnetic loops have been around long enough to find a firm place in the antenna handbooks. Is it time to try a new “tune?”

John Seager, G0UCP, is a retired hospital pediatrician. He has enjoyed a lifelong interest in radio from crystal sets to Software Defined Radio. John's present interests are QRP operating, small portable antennas and learning Chinese.

Notes

¹Bending PVC is quite easy, but not without hazard, so I cannot recommend the method I used which involved inserting a plug in the lower end and then pouring in slightly cooled boiled water. As soon as the tube was full I inserted a cork in the top end and then, wearing gloves, laid the tube on a flat surface and rapidly bent it to the shape required. There was every chance of a serious scald. A tendency for the plugs to pop out during the procedure also makes it unsuitable as an indoor activity! Recently I have used flexible polyethylene pipe instead.

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Definition and Misuse of Return Loss

2009 IEEE. Reprinted with permission, from Vol. 51, No 2. (April 2009) issue of the IEEE Antennas and Propagation Magazine, page 166-167

As Editor-in-Chief of the Transactions, I have noticed over the past year or so that the occasional incorrect use of the term return loss has now grown into a flood of misuse. Perhaps over 30% of all antenna papers submitted to the Transactions in the past twelve months have used return loss incorrectly. The reason for this is uncertain. To remind everyone of the correct terminology, I review the definition of return loss, briefly outline the history of the term and give some examples of current misuse.

Return loss is a measure of the effectiveness of power delivery from a transmission line to a load such as an antenna. If the power incident on the antenna-under-test (AUT) is P_{in} and the power reflected back to the source is P_{ref} , the degree of mismatch between the incident and reflected power in the travelling waves is given by the ratio P_{in}/P_{ref} . The higher this power ratio is, the better the load and line are matched. Expressed in dB, return loss is defined as:

$$RL = 10 \log_{10} \left(\frac{P_{in}}{P_{ref}} \right) \text{ dB} \quad [\text{Eq 1}]$$

which is a *positive* quantity if $P_{ref} < P_{in}$. Stated another way, *RL* is the difference in dB between the power sent towards the AUT and the power reflected. It is a positive, non-dissipative term representing the reduction in amplitude of the reflected wave in comparison with the incident one. This is the situation for a passive AUT. A negative return loss is possible with active devices.¹

Expressing the power in terms of voltage (or equivalently as field strength) in a transmission line or waveguide (assuming a passive AUT), then Equation 1 becomes:

$$RL = 10 \log_{10} \left| \frac{1}{\rho^2} \right| \text{ dB} \quad [\text{Eq 2}]$$

$$RL = -20 \log_{10} |\rho| \text{ dB} \quad [\text{Eq 3}]$$

where ρ is the complex reflection coefficient at the input of the AUT. That is, return loss is the negative of the reflection coefficient, expressed in decibels. In terms of the voltage-standing-wave-ratio (VSWR) this is:

$$RL = 20 \log_{10} \left| \frac{VSWR + 1}{VSWR - 1} \right| \text{ dB} \quad [\text{Eq 4}]$$

$$RL = (40 \log_{10} e) \operatorname{ar} \tanh^{-1} \left| \frac{1}{VSWR} \right| \text{ dB} \quad [\text{Eq 5}]$$

To reinforce the above description, I quote verbatim from the definition of return loss in the *IEEE Standard Dictionary of Electrical and Electronic Terms*.² There are two parts; both are applicable to antennas, cables or waveguides. Return loss:

“(1) (data transmission) (A) At a discontinuity in a transmission system the difference between the power incident upon the discontinuity. (B) The ratio in decibels of the power incident upon the discontinuity to the power reflected from the discontinuity. Note: This ratio is also the square of the reciprocal to the magnitude of the reflection coefficient. (C) More broadly, the return loss is a measure of the dissimilarity between two impedances, being equal to the number of decibels that corresponds to the scalar value of the reciprocal of the reflection coefficient, and hence being expressed by the following formula:

$$20 \log_{10} \left| \frac{Z_1 + Z_2}{Z_1 - Z_2} \right| \text{ decibel}$$

where Z_1 and Z_2 = the two impedances. (2) (or gain) (waveguide). The ratio of incident to reflected power at a reference plane of a network.”

This definition accords with current usage of return loss in modern day text books, such as *Foundations for Microwave Engineering* by R. E. Collin³ or *Microwave Engineering* by D. M. Pozar.⁴ Return loss is a convenient way of characterizing mismatch especially when the reflection is small.

The origin of the definition of return loss is somewhat hazy, although its use in microwaves and antennas appears related to the adoption of the Smith chart. The original paper on the circular transmission line chart, now universally known as the Smith chart, was first published by P. H. Smith of Bell Telephone Laboratories in 1939.⁵ This chart was continually improved through to the late 1960s. It was not until 1949 that the chart first had nomographs of return loss and reflection coefficient at the foot of the chart that are shown today. In the 1940s a similar quantity, a power ratio in decibels was used, which was related to the logarithm of the VSWR.^{6, 7, 8} A few papers on microwaves in the 1950s by Bell Labs staff used return loss.⁹ Most relevant textbooks prior to 1960, however, did not mention it.

Considerably earlier, workers in transmission systems (principally telephone) in the 1930s used return loss as given in the definition (1)(C) above. Research at Bell Labs provided guidelines for the control of “echo” and “singing” on all types of circuits. The reflected signal set up oscillations on the telephone line, and this led to an audible whistle if the return loss was too low. Within the band, “singing return loss” is the lowest return loss at any frequency that this occurs. The objective was to achieve an average return loss of about 11 dB as a compromise

¹Notes appear on page 39.

between sending and receiving in the telephone network.¹⁰

My own experience in the late 1960s and early 1970s was that we preferred VSWR to describe reflections in transmission lines, waveguide and antennas. Return loss was only quoted when the VSWR was close to 1 (often VSWR<1.1, or in other words, RL ~26 dB). This occurred with components for satellite communications or radioastronomy. Nowadays the requirements on reflection coefficient for wireless often specify a 10 dB return loss bandwidth and VSWR provides insufficient discrimination to verify accuracy of simulations, measurements or establish lower reflection levels within the band.

Turning to present-day usage, return loss is now the most common term used to describe reflection and mismatch. Frequently, however, this term is confused with reflection coefficient that has been expressed in dB. The logarithm is taken of the magnitude of the reflection coefficient but this is incorrectly referred to as return loss; the result is still reflection coefficient albeit in decibels. The difference between the two is a minus sign as shown in Equation 3.

Many recent microwave and antenna papers and several well known books carelessly use return loss. I won't name any for fear of embarrassing the authors. Suffice to

say it is common-place to see plots captioned and labeled return loss when in fact they are really describing reflection coefficient. I have even had some reviewers asking authors to change the correct form to the incorrect one — change a positive sign to a negative one even though the authors labeled the plot correctly as return loss! Some authors are inconsistent in the use of terminology (including myself). On one hand they correctly show reflection coefficient but in the text or captions refer to return loss.

In considering the problem of misuse of return loss, I wondered initially if a standard textbook or a software package employed the incorrect definition; I found little evidence for this conjecture. Having become aware of a burgeoning problem, I introduced a reminder in the decision letter to authors of Transactions papers to check their usage of return loss before submission of the final manuscript. This reminder has had only a minor effect, however, as the practice has continued and even increased. Now, where possible, authors are reminded prior to acceptance. More broadly and beyond return loss, correct use of technical terms is vital for promoting consistency and avoiding misunderstanding. Through our publications, and the Transactions in particular, the Antennas and Propagation Society strives for the best

possible publications and, therefore, it is vital that authors aim for accuracy and consistency. Next time you submit a paper, please carefully check your usage of return loss and reflection coefficient; misuse of these terms may delay publication of your paper.

Notes

- ¹D. M. Pozar, *Microwave engineering*, Addison-Wesley, New York, 1990, p 633f.
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- ⁶The present definition of decibel was not adopted until 1929 (See Note 7).
- ⁷K. S. Johnson, "Note — Decibel tables," *Bell System Technical Journal*, Vol. XXV, No. 1, 1946, p 158.
- ⁸C. G. Montgomery, R. H. Dicke and E. M. Purcell, *Principles of Microwave Circuits*, McGraw-Hill, 1948, p 62.
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Hardware Update

I discovered two major mistakes in the initial version of the combination ADC-DAC board. The first is that the DAC-08 requires a current source for V_{REF} rather than a voltage. (I would say the pin should be named I_{REF} instead.) The second comes from the design of the DAC-08, which is so old that it uses the old IBM standard of starting bit counting at one rather than zero, and with bit one as the MSB. The consequence is that our bits are backwards. I have new boards out for fabrication. Figure 1 shows the new schematic. R3 and R4 provide the current source for the DAC-08, and the pins for the DAC-08 are renamed and connected correctly. I also added an optional second DAC so we can do interesting things like binaural audio or $I-Q$ RF generation.

A Real Software Adventure

This installment will walk you through the process I followed to get the first project up and running. Software rarely goes as planned and this was no different. We will walk through getting the intended program built and go through its initial test. Then we will move to using the *Linux* tools to build and test the code using the *Linux* debugger.

I ran into a problem that could affect you. I had installed the 2008 release of the *Windows* hosted GCC tool chain. For some reason, *Norton Virus Scan* believed that some of the intermediate portions of the compiler were a virus and it deleted the executable files. There is a new release on the Blackfin Koop Web site. The file you want is **blackfin-toolchain-win32-2009R1.1.exe**. This appears to be a more stable release and also includes a very nice IDE (Integrated Development Environment) that understands how to connect to the Stamp to do *Windows* based debugging using GDB. So far *Norton* likes this version.

You may be somewhat disorganized, like me, and have misplaced your CD that came with the Stamp. Both of my distribution CDs have disappeared during two office moves. You can download the CD image (in ISO format). You will need CD burner software to create a new CD. The file was difficult to find because it is in the hardware section along with the schematic files. This URL will get you to the image under the "software" label: blackfin.uclinux.org/gf/project/stamp/frs/.

All of the files for the programs in this issue are available on the *QEX* Web site.¹

The Initial Test

Once I got the hardware sorted out using the "peek and poke" method with the uBoot program, it was time to test the corrected hardware. I wrote the program in Listing 1 (The *C* Programming Sidebar gives a short tutorial in *C* programming) to test that the DAC was working correctly using a full speed program. "Full speed" is relative; my program writes the same value to the port 8 times in order to slow the sample rate down enough to stay within the ability of the DAC. Each write to the port only takes about 20 ns. I originally wrote a program that generated a triangle wave and used an oscilloscope to verify that the data lines individually looked correct. It gave confusing results, so I switched to a sawtooth generator. This works well with one channel of the scope hooked to Port G bit 7 (PPI connector pin 13). You get a very nice square wave on the data pin. As you look at each lower bit with the other scope channel, the frequency doubles.

I paid "real money" to buy *Procomm Plus* (Symantec) for a terminal emulator program, since *Hyperterm*, as shipped in *Windows XP* is broken. I discovered that Kermit on the Stamp does not talk to Kermit in *Procomm* correctly. Transfers appear to complete properly, but uBoot declares

that the loaded image (using the loadb command) is not a valid ELF image. I used Kermit within *Hyperterm* and was able to get a proper image loaded. Since my software was confirmed as working, I switched to using Y-modem protocol

Listing 1

```
int main(void)
{
    int    temp, i;

    // Initialize the timer hardware
    init_hardware();
    while(1)
    {
        for (i=0; i < 256; i++)
        {
            *pPORTGIO = i;
            *pPORTGIO = i;
        }
    }
}
```

Listing 2

```
void init_hardware(void)
{
    int temp;

    // Set up Port G for the 8 bit DAC08 interface.
    // Interface uses bottom 8 bits as GPIO
    // Note that the Port G MUX does not need to be modified
    temp = *pPORTG_FER;
    temp &= 0xFF00;
    *pPORTG_FER = temp;
    temp = *pPORTGIO_DIR;
    temp |= 0x00FF;
    *pPORTGIO_DIR = temp;

    // Set up Port F for the AD7476 SPI interface.
    // Interface uses SPI_SEL1, MISO, MOSI, SCLK, and SS
    // Note that the Port F MUX does not need to be modified
    temp = *pPORTF_FER;
    temp |= 0x7c00;
    *pPORTF_FER = temp;
    // set the SPI_FLAG register to use SSEL1
    *pSPI_FLG = 2;
    //set the SPI baud rate to a small value
    *pSPI_BAUD = 1024;
    // enable the SPI
    *pSPI_CTL = 0x552C;
}
```

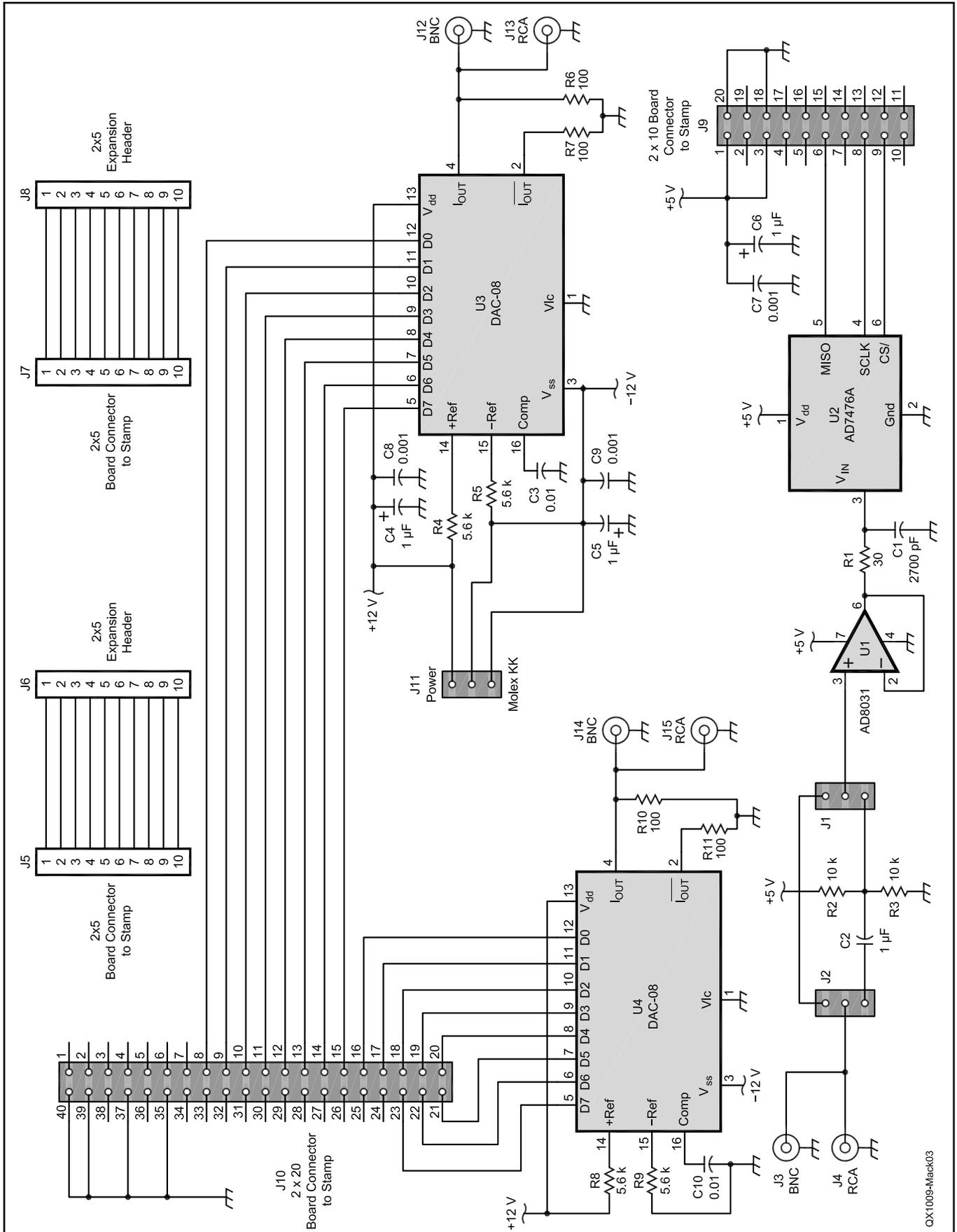


Figure 1 — This schematic diagram shows the corrected ADC and DAC circuits, with connections to the Blackfin BF537 Stamp evaluation board.

from *Procomm* and successfully loaded the image.

Listing 2 shows the hardware set-up function. We need to set up the SPI system, connect the SPI to its port pins, and set up Port G as a GPIO (general purpose I/O) 8 bit output port. This function is in the file named *Initialization.c*, which will be a part of all of our programs that use the combination I/O board.

Listing 3 shows the next hardware test program. The system isn't useful unless we can do both input and output from the system, so we need to be able to read in data, process it, and send the processed data back to the real world. This program reads a sample from the ADC at the rate set by the SPI baud rate at line 36 of *Initialization.c*. The first version of the test program set *SPI_BAUD* to 1024 to ensure that I was running the system at a slow speed for testing. The sample rate is approximately 3 kHz. Figure 2 shows a triangle input waveform from a function generator and the output waveform from the DAC. The next step was to reduce the *SPI_BAUD* value until I reached a sample rate of 1 MSample/s (that could also be stated as 1 μ s/Sample). *SPI_BAUD* is 3 for this program to yield 1 MSample/s.

Figure 3 is the output of the DAC with *SPI_BAUD* set to 3 and using an input sine wave at 900 kHz. This shows the alias effect that occurs with under sampling.

The program uses the trick of writing the same IO port multiple times to kill time. The AD7476A requires a minimum of 50 ns for the chip select pin to be high before the next conversion. We write to the port 6 times to ensure that 50 ns has elapsed. The next trick is the while loop, which counts up to 65535 waiting for the SPI conversion to be complete. Depending on how things initialize, the SPI may hang and not complete a conversion. This loop forces an abort of the SPI cycle and moves to the next cycle. Once you get the SPI functioning, it continues correctly. The last step takes the 12 bit value from the ADC and divides it by 16 using a right bit shift by 4 bits. That changes the data from a 12 bit word to an 8 bit word for the DAC. Writing the DAC requires just one line to write the 8 bit data value to the 8 bit GPIO port.

We are ready, now, to do some real DSP work.

Software Framework

The system I have put together is a two task foreground/background system. There are two "tasks" that operate in the system. The foreground contains the initialization, calculations, and controls that do not need to be synchronized to a particular time. The background is where the input/output work gets done. We want the reads of the ADC and output to the DAC to occur at precise times and with minimal jitter from sample to sample.

Fortunately, the "blink" example pro-

gram provides us with the basics for the foreground/background system. Timer 0 is set up to create a periodic interrupt that we will use to set the sample rate. The interrupt service routine (ISR) for the timer encapsulates the background task. The background task will write the DAC first so that the output samples have minimal jitter (to ensure a clean transmit signal when transmitting). The ADC is read second

and should have minimal jitter since it is always started immediately after the DAC is written. Notice that there are 5 lines of code between setting and clearing the chip select pin for the ADC. That ensures a 50 ns minimum pulse width for the ADC.

There are four buffers that are used for communication between the foreground and the background. The first two buffers hold data from the ADC for the filtering and

Listing 3

```
int main(void)
{
    int    temp, i;

    // Initialize the timer hardware
    init_hardware();
    while(1)
    {
        // start the conversion
        *pSPI_FLG = 0x202;
        // wait for conversion complete
        i = 0;
        while ((*pSPI_STAT & 0x20) == 0)
        {
            i++;
            if (i == 65535)
                break;
        }

        temp = *pSPI_RDBR;
        temp >>= 4;

        *pPORTGIO = temp;
    }
    return 0;
}
```

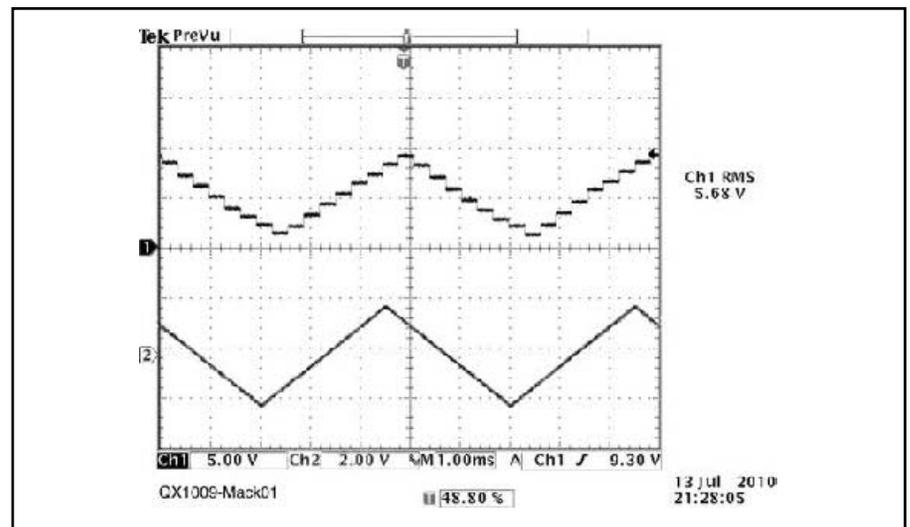


Figure 2 — The lower trace shows a triangle wave input signal from a signal generator, while the upper trace is the DAC output waveform. In program Listing 3, *SPI_BAUD* is set to 1024, for a sample rate of 3 kHz.

demodulation processes. The background fills a buffer and then sends a message to the foreground to consume the data in the buffer. The background then fills the second buffer while the foreground is processing the first buffer. This process continues forever. The second two buffers hold DAC data from the foreground to the background. This portion is likewise double buffered. The system could also have been implemented with queues (a software version of a hardware FIFO), but the system would have required mutual exclusion around the accesses to the input and output positions for the queues.

The function "main()" starts the system and initializes the hardware resources. The last section is the foreground task and is contained in an infinite loop. The "while (1) { ... }" construct is the infinite loop of the foreground. The foreground task must process all of the input samples, all of the output samples and do all of the signal processing for each sample faster than the fastest sample rate in the background. There must be at least some small amount of unused CPU power in order for the system to work. The foreground task is where that unused CPU time is consumed.

Listings 4 and 5 show the foreground and background tasks respectively.

Creating DSP Programs in Linux

I reached a point in debugging the bare metal application where I wasn't certain I could make progress without stepping through the code. I stopped and created a *Linux* application in the hopes that *Linux* does not protect the IO space from programs. *Linux* does, in fact, protect the IO port registers from user access and causes your program to terminate. The process of getting a real program to work under *Linux* is useful, however, for when we want to do work with device drivers and real debugging.

I copied the files for my "test_io" program into a new directory and set up the Makefile to call the *Linux* uClibc portion of the tool chain. Once I got a set of header files with the hardware addresses, the program compiled easily to a *Linux* executable file. Look at the files on the *QEX* Web site for the details.

Debugging In Linux

Debugging is fairly straightforward. You will need to be able to connect your PC and the Stamp board to your local network. The standard debugger for *Linux* systems is "gdb" and has a command line interface. It is very similar to debugging in *BASIC* or using the "debug" command in a *Windows* command window. The new release of the tool chain has the *Eclipse* environment that provides a connection between a *Windows* environment and GDB and looks similar to *Visual DSP* or *Microsoft Visual C++*.

You can launch *Eclipse* by opening *Windows Explorer* and navigating to the *Eclipse* directory in your tool chain. Just

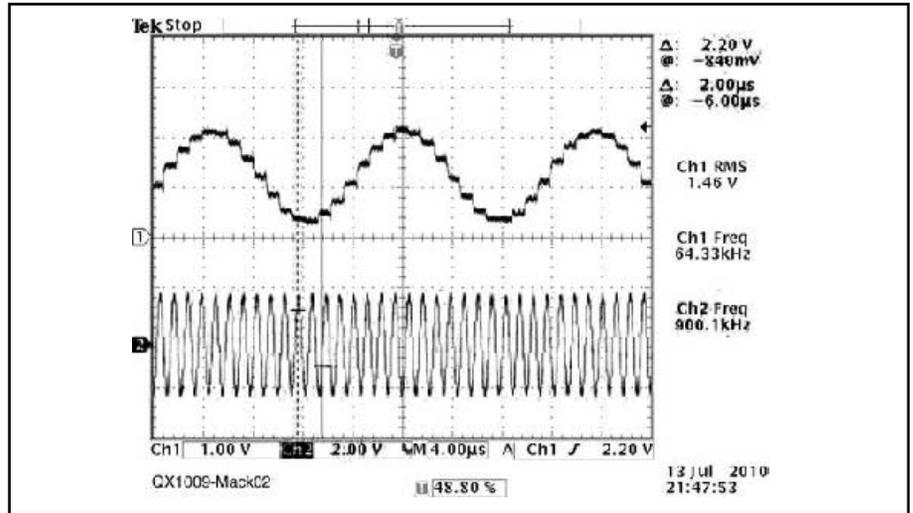


Figure 3 — The lower trace shows a 900 kHz sine wave input signal and the upper trace shows the DAC output waveform, with SPI_BAUD set to 3. This shows the alias effect that occurs with under sampling.

Listing 4

```
static int filling_buffer_A;
static int reading_buffer_A;
int buffer_a_full, buffer_b_full, DAC_buffer_a_empty, DAC_
buffer_b_empty;

//-----//
// Function: main

//
//-----//
int main(void)
{
    int temp, i;

    // Initialize the timer hardware and the ports
    init_hardware();
    // Attach the timer interrupt to the interrupt service
    // routine
    init_isr();
    while(1)
    {
        // Wait for a full ADC buffer
        if (buffer_a_full)
        {
            sdr_receive(BUFFER_A);
            buffer_a_full = FALSE;
        }
        if (buffer_b_full)
        {
            sdr_receive(BUFFER_B);
            buffer_b_full = FALSE;
        }
        // Wait for an empty DAC buffer
        if (DAC_buffer_a_empty)
        {
            sdr_transmit(BUFFER_A);
            DAC_buffer_a_empty = FALSE;
        }
        if (DAC_buffer_b_empty)
        {
            sdr_transmit(BUFFER_B);
            DAC_buffer_b_empty = FALSE;
        }
    }
    return 0;
}
```

Listing 5

```
char next_DAC_value;
static int filling_buffer_A;
static int ADC_buffer_entry;
static int reading_buffer_A;
static int DAC_buffer_entry;
//-----//
// Function: Timer0_ISR
//
// Parameters: None
//
// Return: None
//
// Description: This ISR is executed every time Timer0
// expires.
//-----//

void Timer0_ISR (void)
{
int temp;

// terminate the last ADC conversion
*pSPI_FLG = 0x202;
// confirm interrupt handling, reset the status register
*pTIMER_STATUS = 0x0001;
temp = *pSPI_RDBR;
*pPORTGIO = next_DAC_value;
// start the next ADC conversion
*pSPI_FLG = 0x002;
// store the ADC value
if (filling_buffer_A)
{
ADC_buffer_a[ADC_buffer_entry] = temp;
ADC_buffer_entry ++;
if (ADC_buffer_entry > ADC_BUFFER_SIZE)
{
ADC_buffer_entry = 0;
filling_buffer_A = FALSE;
buffer_a_full = TRUE;
}
}
else
{
ADC_buffer_b[ADC_buffer_entry] = temp;
ADC_buffer_entry ++;
if (ADC_buffer_entry > ADC_BUFFER_SIZE)
{
ADC_buffer_entry = 0;
filling_buffer_A = TRUE;
buffer_b_full = TRUE;
}
}
// read the DAC value
if (reading_buffer_A)
{
next_DAC_value = DAC_buffer_a[ADC_buffer_entry];
DAC_buffer_entry ++;
if (DAC_buffer_entry > DAC_BUFFER_SIZE)
{
DAC_buffer_entry = 0;
reading_buffer_A = FALSE;
DAC_buffer_a_empty = TRUE;
}
}
else
{
next_DAC_value = DAC_buffer_b[ADC_buffer_entry];
DAC_buffer_entry ++;
if (DAC_buffer_entry > DAC_BUFFER_SIZE)
{
DAC_buffer_entry = 0;
reading_buffer_A = TRUE;
DAC_buffer_b_empty = TRUE;
}
}
}
}
```

double click on “eclipse.exe” to start it. Follow the directions at docs.blackfin.uclinux.org/doku.php?id=toolchain:eclipse#debugging_using_eclipse to get *Eclipse* set up to do debugging. There are very few steps involved, and the documentation is very well written. My examples use Port 3456 for the *Eclipse* setup as the connection between the Stamp and the PC. A port is just a number that network software uses as another type of address. This is an address in addition to the IP addresses for the computers. I picked 3456 because it was in an example and it is not likely to be used by other software on a network.

The first step in debugging is to connect your PC to the Stamp serial port and boot *Linux* on the Stamp. You obtain an IP address from your router by typing “dhcpcd &” on the console. The next command, “ftpd -D”, starts the FTP server so we can transfer our files to the Stamp. Type “ifconfig” to get your IP address so you can communicate with the Stamp. We’ll use my IP address (192.168.1.108) for our examples.

Now we move back to the PC. In your command window, change to the directory for the program to debug (c:\analog_devices\test_io in this case). Type “ftp 192.168.1.108”. The program will ask you to log in. The user name is “root” and the password is “uClinux”. It is important to do the command “binary” next, to ensure that the file is transferred as a program rather than text. Type “put test_io” to move the program to the Stamp. Typing “quit” exits the FTP program.

Now we go back to the Stamp and type “ls” to ensure that the test_io program got loaded. When FTP puts a file on the Stamp, it is an ordinary file. We need to tell *Linux* that test_io is a program that can be executed. Type “chmod 777 test_io”. Typing “ls” will show test_io in a different color (if you have a color terminal emulator) to indicate it is now executable.

The combination of *Eclipse* and GDB requires a client/server type connection. The client is *Eclipse* running on the PC and the server is a program called gdbserver that runs on the Stamp. This is the place where you need that port number. Type “gdbserver localhost:3456 test_io”. The server will start and wait for you to start the *Eclipse* debugger by clicking on the “Run->Debug Configurations...” menu. Clicking the “Debug” button on the dialog will launch the debugger and stop with the program ready to debug. At that point you run the debugger just as you would any other *Windows* based debugger. One important thing to remember is that the *Eclipse* authors decided to use different “F” key values from most of the rest of the world. F5 and F6 step through code, while most debuggers use F10 and F11. As you step through the program you will see the messages on the console from the gdbserver. If you step to the point in my program where I attempt to write the Port

G register, you will see the program terminate because *Linux* forbids your program to access those registers. We will use the debugger and device drivers to debug our logic in an upcoming installment.

Notes

¹The program files listed in this column are available for download on the ARRL QEX Web site. Go to www.arrl.org/qexfiles and look for the file **9x10_Mack_SDR.zip**.

C Programming Sidebar

It is likely that you have programmed in BASIC or FORTRAN or some other rudimentary language. You just start programming by writing lines of commands in BASIC. Modern versions do not even require line numbers for statements. C is a more modern language and is similar to the languages *Delphi*, *Pascal*, and *Ada*. All of these languages use the concept that all code is contained inside of functions or procedures. All C programs are required to have at least one function whose name is "main". The keyword "int" in front of main() in Listing 1 indicates that it will return a number to the operating system. The compiler requires that it have that data type or you will get a compile error. Likewise, the "return 0;" statement returns the number zero to the operating system and is required. The purpose is for your program to use that "return" statement to let the operating system know if your program encountered an error. The data type in the parentheses "(void)" tells the compiler that we will not be passing any information to the function "main".

In BASIC you can access a location with a simple PEEK or POKE command, like so:

```
Temp = PEEK(UART_DATA)
```

to read the UART data register or

```
POKE(UART_BAUD, 57600)
```

to write to the UART baud rate register. You can do exactly the same operations in C, but the syntax is more complicated. The first step is to create a variable that will hold the address we want to POKE into. In Listing 1, that variable is "pPORTGIO". In the init_hardware function, we write the line:

```
pPORTGIO = 0xFFC03204;
```

That tells the C compiler that we want to manipulate the address FFC03204, which is the Port G data register. The line in Listing 1:

```
*pPORTGIO = i;
```

tells the compiler to create the instructions to take the value stored in the variable "i" and store it in the address contained in the variable pPORTGIO. That asterisk tells the compiler to store a value at a particular memory address. We call the variable pPORTGIO a pointer variable because it points to a particular memory address. The "p" in the name helps us remember that it is a pointer type variable. We will use pointer variables extensively to access the various IO ports on the Stamp. To PEEK at a value, we simply reverse the syntax:

```
temp = *pSPI_DATA;
```

This lets us read from the SPI data register and store the data into the variable "temp".



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3CX800A7	4CX250R	YC-130	5867A
3CX1200A7	4CX350A	YU-106	5868
3CX1200Z7	4CX350F	YU-108	6146B
3CX1200Z7	4CX400A	YU-148	7092
3CX1500A7	4CX800A	YU-157	3-500ZG
3CX2500A3	4CX1000A	572B	4-400A
3CX2500F3	4CX1500A	807	M328/TH328
3CX3000A7	4CX1500B	810	M338/TH338
3CX6000A7	4CX3000A	811A	M347/TH347
3CX10000A7	4CX3500A	812A	M382

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Reader's Page

Bill Moneysmith, W4NFR, shared these photos of his recently completed GS-35B triode HF amplifier. It operates on 160 through 10 meters and uses the LDG Z-11Pro II tuner on the input. Bill drives it with his Kenwood TS-870S transceiver.

The amp features a Russian GS-35B triode, a Dayton blower for cooling, a Multronics 22.5 μ H variable Edgewound inductor, 10-1000 pF vacuum variable capacitors for loading and tuning and Giga-vac vacuum RF relays. The chassis is entirely homebrew attached

to a standard 10.5 x 19.0 x .125-inch front panel. It has a variable bias inside with a small pot to the side of chassis for adjustment. The overall size was chosen to fit inside a Hammond Manufacturing cabinet that Bill picked up at FAIR Radio in Lima, Ohio.

The images show the amplifier in various stages of construction (clockwise from upper left), culminating in the finished product displaying 1500 W output on a Bird wattmeter. It's an engineering work of art!



QEX

Upcoming Conferences

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The ARRL and TAPR Digital Communications Conference is an international forum for radio amateurs to meet, publish their work, and present new ideas and techniques. Presenters and attendees will have the opportunity to exchange ideas and learn about recent hardware and software advances, theories, experimental results, and practical applications.

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For more information go to www.tapr.org.

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Microwave Update (MUD), the nation's most popular, amateur radio-focused microwave and millimeter wave experimentation technical conference will be held at the Sheraton Cerritos Hotel from October 21 through 24, 2010.

Each year, the MUD attracts attendees from all over the world to discuss the latest technical developments and operating achievements in amateur experimentation on the 1,000MHz and up frequencies.

This year's event is hosted by the San Bernardino Microwave Society (SBMS). MUD is a technical conference and includes presentations by leading microwave radio experimenters and a banquet as well as a vendor area where exotic microwave RF components can be bought and sold. Several commercial equipment manufacturers are scheduled to appear, to demonstrate their latest offerings. In addition, noise figure and antenna gain test sessions for up to 47GHz are being planned.

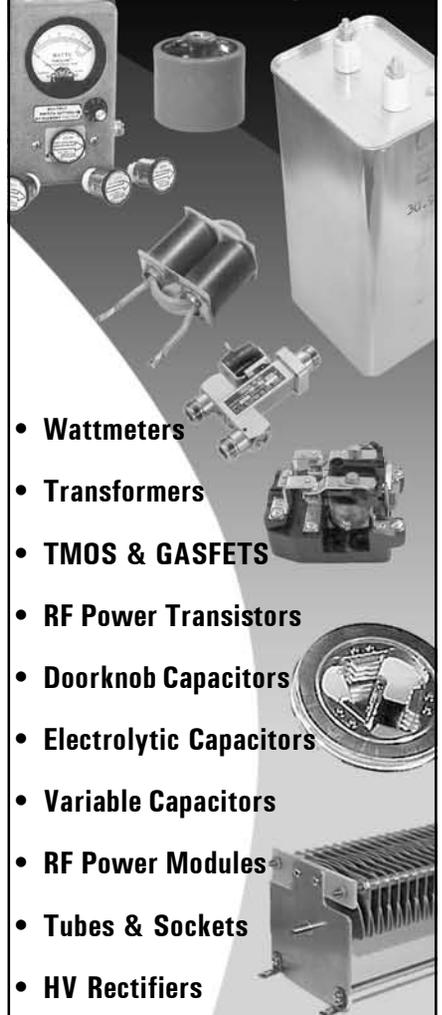
Participants are encouraged to register for the conference and reserve hotel rooms as early as possible. When making hotel reservations, make sure to mention the Microwave Update to qualify for your special rate.

The town of Cerritos offers a number of excellent activities for sight-seeing, and the Southern California Fall weather is another bonus. Participants are encouraged to make this a family affair. We will have Ladies Activities in and around the hotel, and there are many local attractions such as Medieval Times®, Knott's Berry Farm®, Disneyland® and the Queen Mary (W6RO) nearby.

More details, including a registration form, can be found on the Microwave Update website, at www.microwaveupdate.org

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October 8-10, 2010

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AMSAT announces the 2010 Space Symposium and Annual Meeting will be held on Friday, October 8 through Sunday, October 10. This year we have selected the Chicago/Elk Grove Holiday Inn which is near O'Hare Airport for the event. This is the same hotel that recently has hosted the Central States VHF Conference, TAPR and W9DXCC events.

All Amateur Radio Operators interested in space communications are invited to participate in the Symposium offerings including: Space Symposium with Amateur Satellite Presentations; Operating Techniques, News, & Plans from the Amateur Satellite World; Board of Directors Meeting open to AMSAT members; Meet Board Members and Officers; Annual General Membership Meeting; Annual Banquet—Keynote Speaker and Door Prizes; President's Club Reception; Area Coordinator's Breakfast.

The Chicago/Elk Grove Holiday Inn is located at 1000 Busse Road, Elk Grove, IL (near O'Hare Airport with free hourly shuttles). The Hotel booking code for the Elk Grove Village Holiday Inn is AMS for the AMSAT convention. The \$79 per-night room rate will apply for those using this group code.

At the conclusion of the Symposium activities you are invited to participate in a tour of the Tevatron at the Fermi National Accelerator Laboratory at Noon on Sunday. Plans include a tour of the multi-megawatt RF portions of the particle accelerator as well as a tour of the new Super Conducting RF Test Facility.

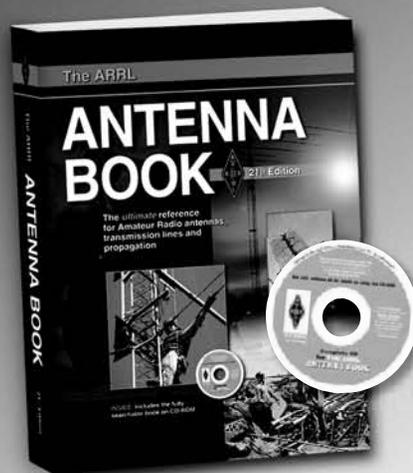
Check www.amsat.org for more news as it becomes available.

Next Issue in QEX

Ron Skelton, W6WO, discusses the role of baluns in general, but more importantly, explains a critical figure of merit in balun design: CMRR, otherwise known as Common Mode Rejection Ratio. The CMRR of a balun is defined in professional literature as the ratio of wanted to unwanted transmitted power. Ron applies this definition to amateur baluns and shows how to go about measuring it accurately.

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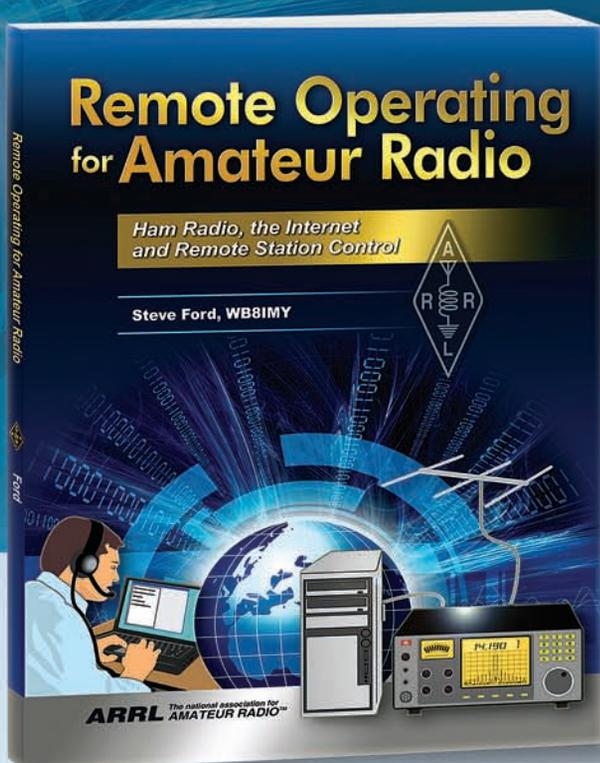
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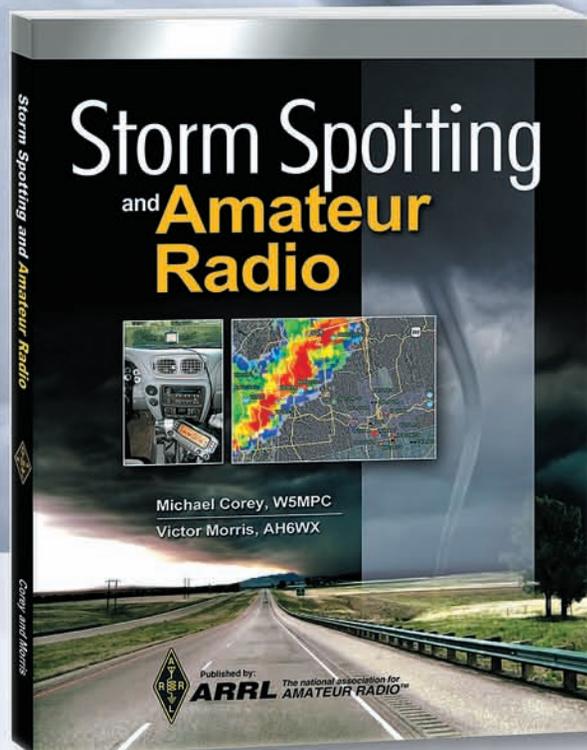
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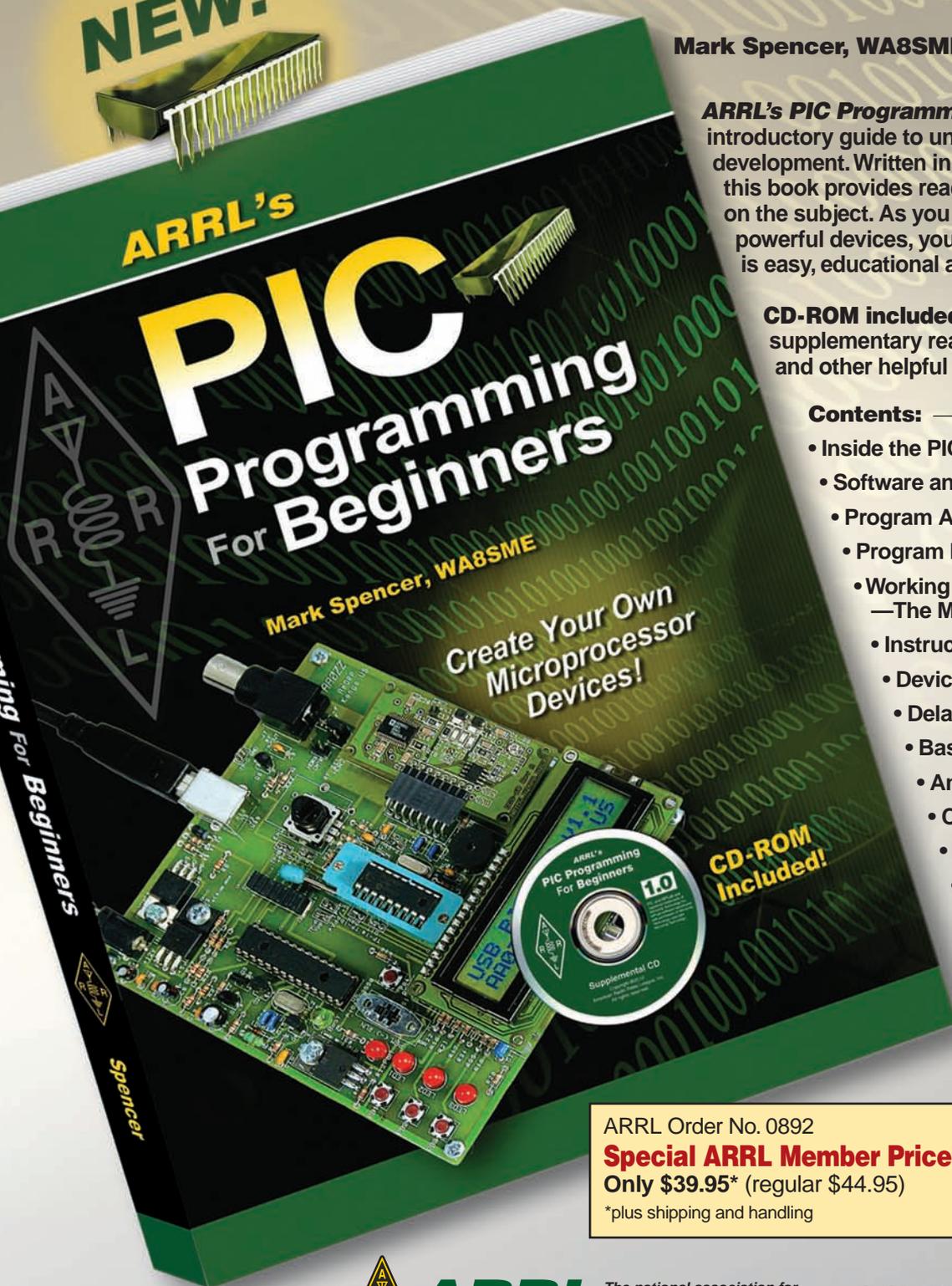
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