QEX

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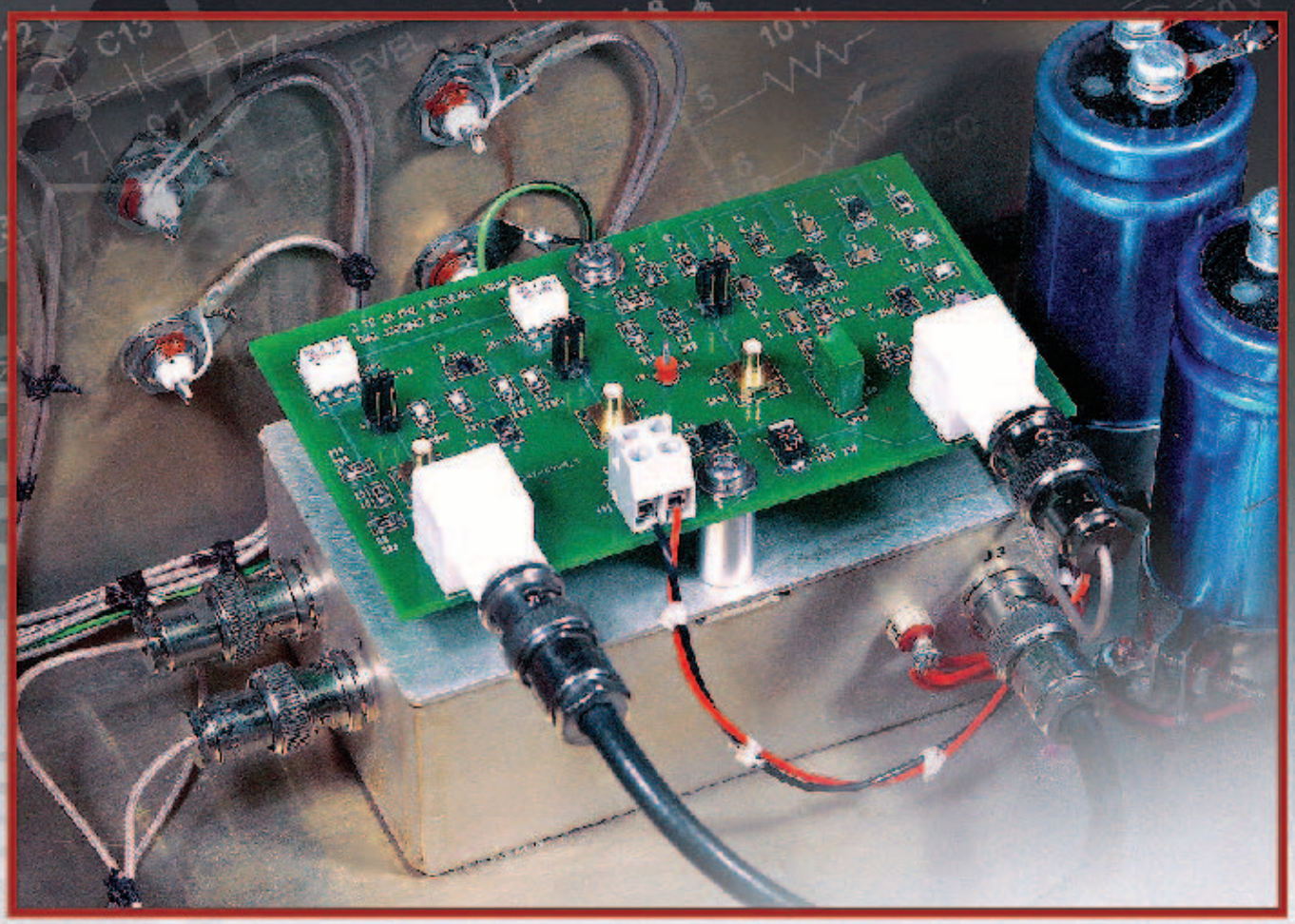

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About the Cover

Much of the test equipment made during the last couple of decades requires 10 MHz external frequency references. But what if all you have is an older 5 MHz frequency standard, a common device back in the day? Rather than purchase a new standard John Roos, K6IQL, created a solution in the form of a quadrature driven mixer frequency doubler and output amplifier. John's design converts a 5 MHz standard to 10 MHz and does so with exceptionally low spurious levels. Read about it in this issue!

In This Issue

Features

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The American Radio Relay League

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The purpose of *QEX* is to:

1) provide a medium for the exchange of ideas and information among Amateur Radio experimenters,

2) document advanced technical work in the Amateur Radio field, and

3) support efforts to advance the state of the Amateur Radio art.

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Larry Wolfgang, WR1B

Empirical Outlook

Becoming a *QEX* Reader

Many of you noticed that in the January/February 2011 issue of *QEX*, the end of the article by Roger Paskvan, WAØIUJ, "An All Purpose High Gain Antenna for 2400 MHz" was missing. A last-second error in preparing the file to send to our printer resulted in that problem, and we sincerely apologize for the confusion and inconvenience it caused you. Shortly after discovering that the last page of the article was missing, I posted the complete article to the "This Month in *QEX*" section of the ARRL website: **www.arrl.org/this-month-in-qex**. For those who did not find the article posted there we have printed the missing page in this issue. See page 47. In addition, I have posted a new photo for Figure 1 and new graphs for Figures 2, 3 and 4 to the *QEX* files web page: **www.arrl.org/qexfiles**. The new photo and graphs have higher resolution than those printed in *QEX*, but otherwise do not present any different information.

I have spent the past 6 months on a medical leave from my responsibilities at ARRL Headquarters. In my absence, Publications Manager Steve Ford, WB8IMY, and *QEX* columnist and technical proofreader, Ray Mack, W5IFS, have been filling in for me. You have probably noticed that Ray's "SDR: Simplified" column last appeared in the Sep/Oct 2010 issue. Ray had that column just about completed before I went to Virginia for the Boy Scout National Jamboree last July. Since then, he has been too busy editing articles for publication, and was unable to find time to write another column. I hope that will change shortly.

While at the Jamboree, I became ill, and was hospitalized with a cellulitis infection of my leg. I have now nearly recovered from that infection, as well as surgery and a skin graft that resulted from it. During my absence, Steve and Ray have completed one and edited four more issues of *QEX*, along with also carrying out their normal full time responsibilities. My "Thank you" seems totally inadequate!

Now I have a confession to make to you. Prior to my illness, I had not been a *QEX* reader. That is, not in the same sense that you enjoy *QEX* in the comfort of your home.

You are probably wondering how I could have missed the pleasure of really *reading* this great magazine as you read it, as it is meant to be read, for so long. From the time *QEX* was first published, I would pick up a copy at ARRL HQ, and occasionally read an article or two. Frequently an article would look interesting, and I would skim through it, but I did not read any issue cover to cover! After becoming a *QEX* assistant editor, and later Managing Editor and then Editor, I still picked up a copy and paged through, but almost never read anything in the finished, bound magazine. (Of course by the time the magazine is printed, I have read every manuscript several times as I edited them, and read several versions of page layouts as we prepared the magazine to go to the printer.)

While on medical leave, I really started to look forward to each issue arriving in the mail. Perhaps this gives me a better perspective for how you feel as you await the arrival of each issue in your mailbox. I would quickly grab my copy and examine the cover, and then open it to the table of contents to see the list of articles inside. Each article seemed to demand to be read first! Although I had read all of the manuscripts as we reviewed submitted articles, that is not at all the same as reading the finished product printed in the magazine.

I had helped select the articles for the Sep/Oct issue, but did not edit any of the articles. I always enjoy Phil Anderson's articles and "Synthesizing an Audio AGC Circuit" was no exception. I wondered how the "WB2EZG Five-Band Trap Dipole" turned out, and was anxious to read that article. Andrew Daretti's "Simple and Effective Power Reference" article sure was interesting.

Horst Steder's "High-Frequency Ladder Filters with Third Overtone Crystals" was a fascinating read, as was Dave Bowker's "RF Phase Meter." Ron Skelton presented some very interesting information about "HF Balun Performance." I may need to consider adding a vector network analyzer to my stock of test equipment.

James Ahlstrom's "All Digital Transceiver for HF" is a tremendous project. Few of us are likely to duplicate his efforts, but there is so much to learn in that article! I will probably never absorb everything, but it is definitely worth reading several times. Sivan Toledo's "Driverless Ethernet Sound Card" presents me with another learning opportunity. While I am not active on 2400 MHz, any project that involves hardware and plumbing construction techniques holds my interest. I imagine I am more likely to be able to complete such a project than one involving magnifiers, tweezers and a needle-point soldering iron. In spite of that missing page, Roger Paskvan's article looks like something I could build.

This issue includes another solid line-up of articles that I am anxious to read. In fact, I've already started reading this issue, because I received the page layout PDF files to review before the issue went to press. Happy reading.

John E. Post, KA5GSQ

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On Determining Loop Gain through Circuit Simulation

Loop gain is a fundamental parameter for electronic circuits that employ either positive or negative feedback. This article discusses how to determine loop gain through circuit simulation.

Amplifiers employing positive or negative feedback are fundamental building blocks in electronic circuits. Negative feedback is employed to linearize amplifiers in order to reduce distortion of the input signal and improve amplifier bandwidth. Conversely, applying sufficient positive feedback to an amplifier results in an oscillator because an output signal occurs when no input signal is present.[1]

Figure 1 depicts a block diagram for a simple amplifier with positive feedback. The gain of the amplifier is A while the gain (or loss) of the feedback network is K. The input and output voltages of the overall circuit are v_i and v_o respectively, while the voltage at the output of the feedback network is v_f. Again referring to Figure 1, the output voltage is obtained from the amplified sum of the input and feedback voltages, or

$$v_o = A(v_i + v_f) \qquad \text{Eq. 1}$$

while the voltage at the output of the feedback network is found from

$$v_f = Kv_o \qquad \text{Eq. 2}$$

Combining Equations 1 and 2 in order to eliminate the feedback voltage term allows the voltage at the output of the amplifier to be expressed in terms of the input voltage as

$$v_o = \frac{A}{1 - A \bullet K} v_i = \frac{1}{K} \bullet \frac{1}{\frac{1}{A \bullet K} - 1} v_i \qquad \text{Eq. 3}$$

In Equation 3 the term AK is referred to as the loop gain T.

In order for the positive feedback amplifier to sustain oscillations the Barkhausen criteria requires that the magnitude of T is equal to unity at a frequency where the phase of T is equal to 0 degrees or radians (or some integer multiple of 360° or 2π radians). In order for oscillations to *start* the loop gain must be greater than unity at a frequency where the phase is 0 degrees or radians (or some integer multiple of 360° or 2π radians).[2] Thus, the loop gain provides critical information concerning whether an electronic circuit will actually function as an oscillator.

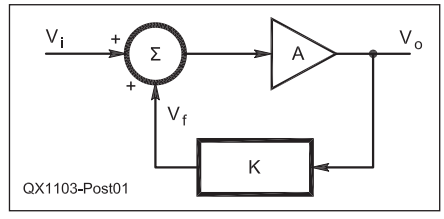

Figure 1 — Block diagram of positive feedback amplifier depicting input voltage v_i, output voltage v_o, and feedback voltage v_f.

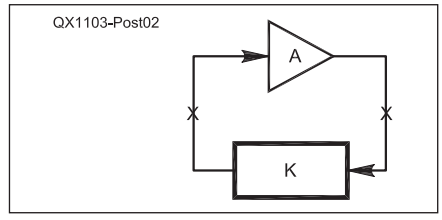

Figure 2 — Positive feedback amplifier redrawn to emphasize the feedback loop. Each "X" indicates locations where it is possible to break open the loop in order to determine loop gain.

In order to develop a method to determine the loop gain, consider Figure 2, which is redrawn to emphasize the feedback portion of the loop from Figure 1. If the loop is opened at either "X" and a test voltage v_{test} is applied to the side of the loop that leads to the amplifier input, what voltage $v_{measure}$ is measured at the other side of the loop opening? Obviously $v_{measure} = AKv_{test}$ so that the loop voltage gain is $v_{measure}/v_{test} = AK = T$.

Figure 3 shows a circuit model of the positive feedback amplifier, Figure 2. As shown in the figure the circuit consists of a dependent source, in this case a voltage controlled current source that represents an ideal transconductance amplifier and an impedance Z_f that represents the load of the feedback net-

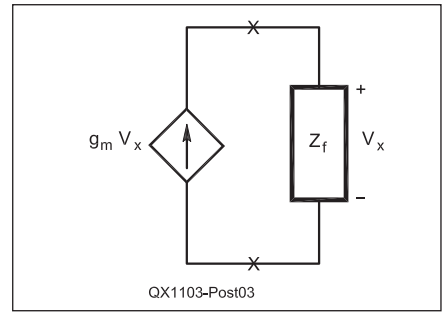

Figure 3 — Alternative model of a positive feedback amplifier consisting of a dependent current source with current $g_m v_x$ in parallel with a feedback impedance Z_f. Each "X" indicates locations where it is possible to break open the loop in order to determine loop gain.

[1]Notes appear on page 7.

work on the controlled source. In general it is possible to define either a loop voltage gain T_v or a loop current gain T_i. The procedure for determining either one is the same—the loop is opened, a test voltage (current) is applied and a response voltage (current) is determined and then their ratio is obtained. But now a second load impedance Z_f is connected across the source in order to maintain the same load impedance on the source with the loop open as with the loop closed. This is shown in the two circuits shown in Figure 4. For the circuit on the left side of the figure applying a test voltage of v_x results in a voltage of v_y and the loop voltage gain is $T_v = v_y/v_x = g_m v_x Z_f/v_x = g_m Z_f$. For the circuit on the right side of the figure applying a test current of i_x results in a current of i_y and the loop current gain is $T_i = i_y/i_x = g_m(v_x/Z_f) = g_m Z_f$. In this simple example $T_v = T_i = g_m Z_f = T$ which is the overall loop gain, but this result holds only if the output impedance of the dependent source is ignored as we shall see.

Although the technique of opening the loop appears simple in theory there are a number of factors that complicate its application to a practical circuit. For example opening the loop may remove the dc bias current for the active device so that it no longer functions. Another problem is precisely duplicating the value of the load impedance that appears in parallel with the dependent source once the loop is broken.

An Experimental Method for Determining the Loop Gain

In 1975 R.D. Middlebrook proposed a method to overcome these limitations for negative feedback amplifiers.[3] Middlebrook applied this method to measure the loop gain of negative feedback amplifiers. It is also possible to apply the method to determine the loop gain of negative feedback amplifiers through circuit simulation.[4]

In general Middlebrook's method determines the loop voltage gain T_v by inserting an arbitrary voltage source v_z into the loop as shown by the circuit on the right side of Figure 5. Because practical dependent sources contain an internal impedance Z_s this impedance, as well as the load impedance Z_f due to the feedback network, is shown in the circuits in Figure 5.

Because the internal impedance of the voltage source v_z is a short circuit the load impedance seen by the dependent source is unchanged and bias currents are unaffected. All that remains is to obtain the voltages v_x and v_y, through either measurement or circuit simulation, and then determine the loop voltage gain $T_v = v_y/v_x$.

The loop current gain T_i may be obtained by the dual of the previous method as shown in the left side of Figure 5. This time an arbitrary current source i_z is added in parallel with the dependent source and feedback network. Because the internal impedance of the current source is infinite the load impedance seen by the dependent source is unchanged and the bias currents are unaffected. In this case it is necessary to obtain the currents i_x and i_y, through either measurement or circuit simulation, and then determine the loop current gain $T_i = i_y/i_x$.

Next it is necessary to determine the overall loop gain T from the loop voltage gain T_v and loop current gain T_i. This is demonstrated in Appendix 1, which modifies Middlebrook's result for the case of a positive feedback amplifier (oscillator). As shown in Appendix 1, once the loop voltage gain T_v and the loop current gain T_i are obtained the overall loop gain T can be found from

$$T = \frac{T_v T_i - 1}{T_v + T_i - 2} \qquad \text{Eq. A-1}$$

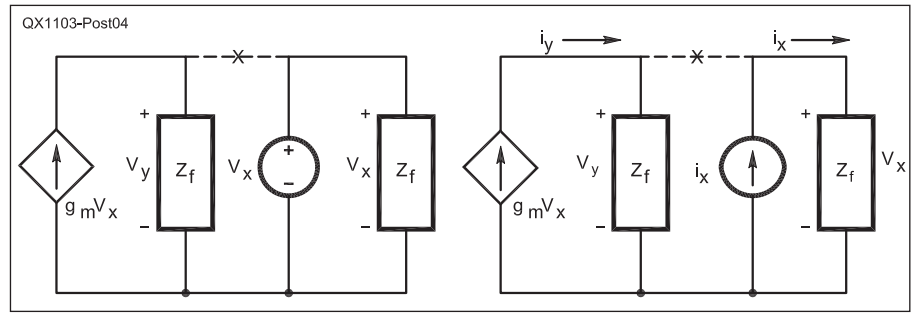

Figure 4 — In order to obtain loop voltage gain break loop at "X", insert a test voltage source, and then determine $T_v = v_y/v_x$ (left circuit). In order to obtain loop current gain break loop at "X", insert a test current source, and then determine $T_i = i_y/i_x$ (right circuit). In each case after the loop is broken it is necessary to insert a replacement feedback impedance Z_f in order to maintain a constant load for the dependent current source.

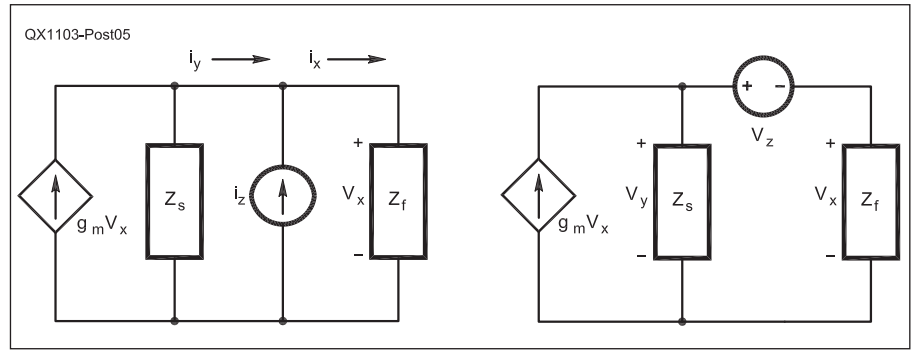

Figure 5 — Determine loop voltage gain by inserting an arbitrary voltage source v_z and then obtaining $T_v = v_y/v_x$ (right circuit). Determining loop current gain by inserting an arbitrary current source i_z and then obtaining $T_i = i_y/i_x$ (left circuit).

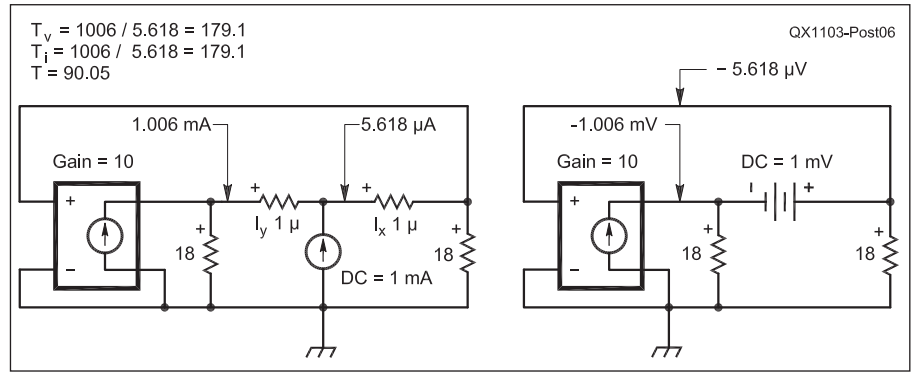

Figure 6 — Circuit simulation to determine loop voltage and current gain for the circuits shown in Figure 5 for the case of $Z_s = R_s = 18\ \Omega$ and $Z_f = R_f = 18\ \Omega$.

For large values of T_v and T_i Equation A-1 can be approximated as

$$T \cong \frac{T_v T_i}{T_v + T_i}$$

which demonstrates that, like the formula for two parallel resistors, the overall loop gain T will be smaller than the smallest of either the loop current gain T_i or the loop voltage gain T_v.

The balance of this article will demonstrate how to apply Equation A-1 through circuit simulation in the case of dc, audio, and radio frequency positive feedback amplifiers.

Example: Determining the Loop Gain for DC Circuits

Because Equation A-1 was derived by applying general circuit laws, it applies equally to either time varying (ac) or constant (dc) voltages. Thus before applying the method to determine the loop gain of an oscillator it is instructive to review several dc simulations to demonstrate that Equation A-1 is correct, as well as illustrate the method of obtaining the loop gain T through simulation.

Figure 6 presents a circuit simulation of a positive feedback amplifier. In this case $R_s = R_f = 18\ \Omega$ so the load and feedback resistances are equal and the theoretical loop gain is $T = g_m R_{eq} = 10S(18\Omega \| 18\Omega) = 90$ V/V. The function of the two 1 μΩ resistors is to sense the currents i_x and i_y without perturbing the results. As shown in the figure in the case of equal load and feedback resistance $T_v = T_i = 179.1$. Applying Equation A-1 with these values yields $T = 90.05$ V/V, so excellent agreement is obtained between the simulated and theoretical values of the overall loop gain T. Notice that the value of either the test voltage or current source in Figure 6 is immaterial since only the ratio of i_y and i_x or v_y and v_x is of interest rather than the individual values of voltage or current.

Figure 7 presents a circuit simulation for the case of $R_s = 10\ \Omega$ and $R_f = 90\ \Omega$ so the theoretical loop gain is unchanged because $T = g_m R_{eq} = 10S(10\Omega \| 90\Omega) = 90$ V/V. In this case the source resistance is much less than the feedback resistance so the dependent source approximates a voltage source because of its relatively low resistance and the loop voltage gain dominates the overall loop gain T because $T_i = 890.6$ while $T_v = 99.90$. Applying these values to Equation A-1 again results in T = 90.00 V/V, so excellent agreement is once again obtained between the simulated and theoretical values of the loop gain and since $T_v << T_i$, $T \cong T_v$.

Figure 8 presents a circuit simulation for the converse of the previous case in that now $R_s = 90\ \Omega$ and $R_f = 10\ \Omega$. In this case the feedback resistance is much less than the source resistance so the dependent source approximates a current source. The theoretical loop gain is unchanged because $T = g_m R_{eq} = 10S(90\Omega \| 10\Omega) = 90$ V/V. The results obtained here are the reverse of the previous results and the loop current gain dominates because $T_v = 890.6$ while $T_i = 99.90$. Applying these values to Equation A-1 once again results in T = 90.00 V/V, so excellent agreement is obtained between the simulated and theoretical values of the loop gain and since $T_i << T_v$, $T \cong T_i$.

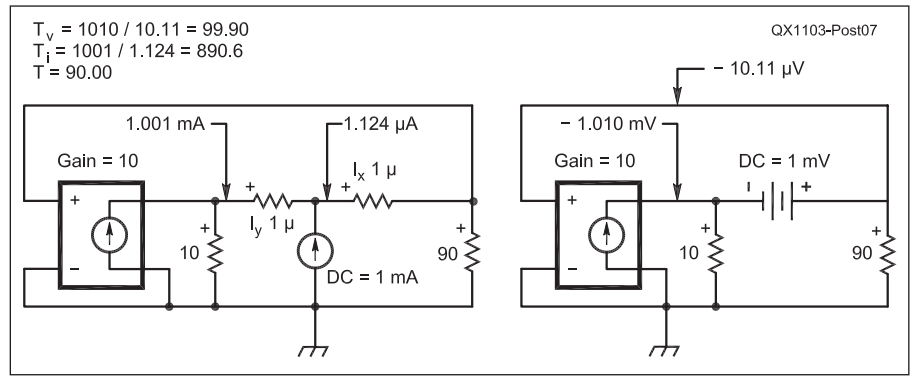

Figure 7 — Circuit simulation to determine loop voltage and current gain for the circuits shown in Figure 5 for the case of $Z_s = R_s = 10\ \Omega$ and $Z_f = R_f = 90\ \Omega$.

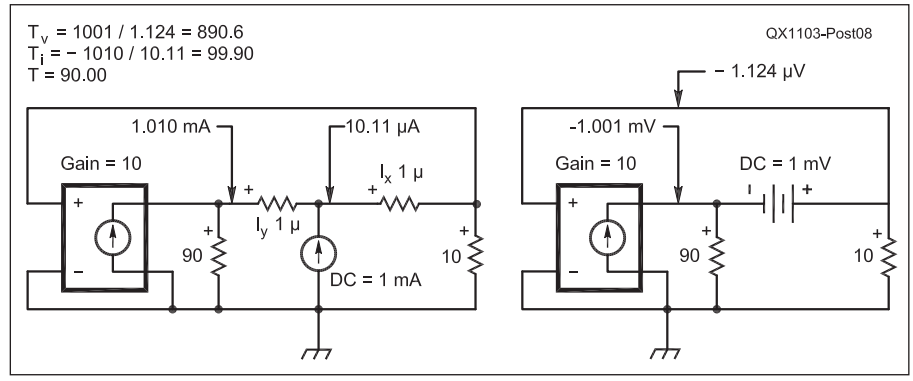

Figure 8 — Circuit simulation to determine loop voltage and current gain for the circuits shown in Figure 5 for the case of $Z_s = R_s = 90\ \Omega$ and $Z_f = R_f = 10\ \Omega$.

Example: Determining the Loop Gain of a Wein-Bridge Oscillator

The results in the previous section are instructive because they point out that if the feedback amplifier can be approximated as either an ideal voltage or current amplifier the overall loop gain T may be obtained from a single circuit simulation. In order to illustrate this concept consider Figure 9 which presents the schematic diagram of an audio frequency Wien-bridge oscillator. Referring to the figure, the oscillator consists of an operational amplifier with two feedback paths. The upper negative feedback path through the 1kΩ and 5kΩ resistors has a gain of 1 + 5k/1k = 6 V/V. This path provides negative shunt feedback to the amplifier output

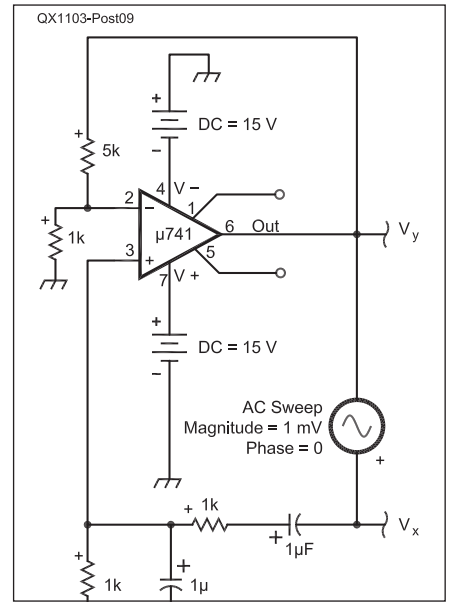

Figure 9 — Circuit simulation to determine the loop voltage gain for the Wein-bridge oscillator. The upper network provides negative feedback and controls the amplifier gain. The lower network provides positive feedback and controls the frequency of oscillation. In this case the loop is broken and an arbitrary voltage source is inserted between the output of the amplifier and the input of the feedback network.

Table 1
Calculated versus simulated results for Colpitts oscillator loop gain and oscillation frequency. The error is obtained from (Calculated-Simulated)/Calculated x 100%.

	Loop Gain (V/V)			*Oscillation Frequency (MHz)*		
C (pF)	*Calculated*	*Simulated*	*% Error*	*Calculated*	*Simulated*	*% Error*
340	1.00	1.06	-6.00%	1.0184	1.0157	0.27%
373	1.07	1.13	-5.61%	1.0160	1.0135	0.25%
426	1.17	1.22	-4.27%	1.0124	1.0102	0.22%
470	1.24	1.28	-3.23%	1.0097	1.0076	0.21%
556	1.34	1.38	-2.99%	1.0049	1.003	0.19%
800	1.50	1.52	-1.33%	0.9929	0.9913	0.16%

which reduces the amplifier output resistance by the factor of 1 + *AK* so the circuit very closely approximates an ideal voltage amplifier.[1]

The lower positive feedback path through the *RC* network controls the frequency of oscillation. In the special case where the two resistors are of equal value and the two capacitors are of equal value it is possible to show that the oscillation frequency is

$$f_o = \frac{1}{2\pi RC}$$

while the gain of the lower feedback network is 1/3 V/V[5]. Thus for the circuit in Figure 9, the oscillation frequency is

$$f_o = \frac{1}{2\pi \cdot 10^3 \cdot 10^{-6}} = 159.15 \text{ Hz}$$

and the loop gain is

$$6 \cdot \frac{1}{3} = 2 \text{ V/V}.$$

Figure 10 shows the phase in degrees (top) and magnitude in V/V (bottom) of $T_v = v_y/v_x$, where v_y and v_x were obtained by conducting an ac sweep between the frequencies of 155 Hz and 165 Hz of the circuit shown in Figure 9. The cursor in the top plot in Figure 10 is positioned to show that the phase is 0º at f_o = 158.92 Hz while the bottom plot shows the loop voltage gain T_v = 1.999 V/V at that same frequency. A separate simulation (not shown) reveals that the loop current gain is T_i = 44.175 kA/A at the same frequency so the circuit is an almost perfect voltage amplifier as claimed previously. Thus $T_v << T_i$, so $T \cong T_v$ = 1.999 V/V. In this case the theoretical and simulated loop gain and resonant frequency differ from each other by no more than a few tenths of a percent in either case. These results further confirm the utility of this method to determine oscillator loop gain through simulation.

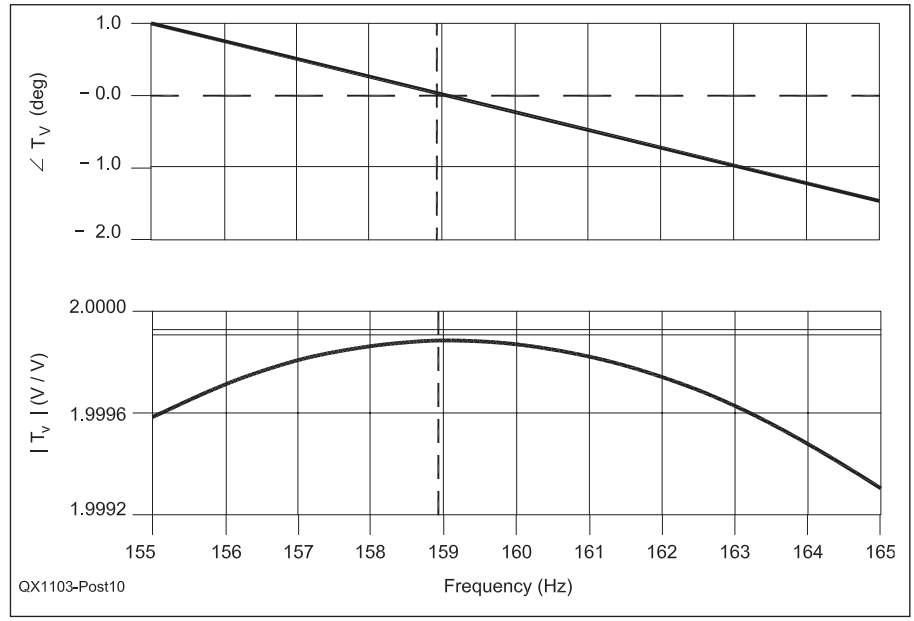

Figure 10 — Loop gain phase (top) and magnitude (bottom). The loop voltage gain T_v = 1.9999 V/V and T_y = 0° at 158.92 Hz.

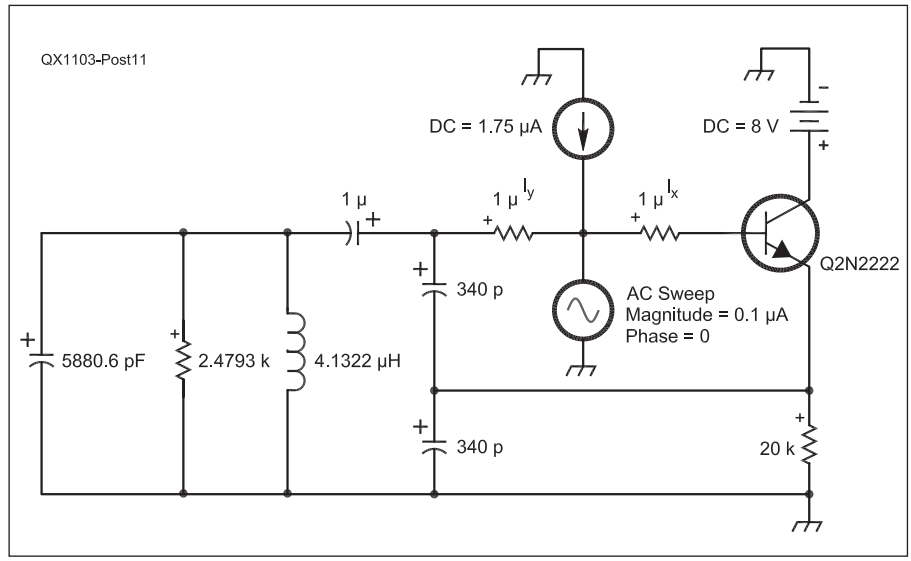

Figure 11 — Circuit simulation to obtain the loop current gain T_i of the Colpitts oscillator. In this case an arbitrary current source is connected between the input of the amplifier and the output of the feedback network.

Example: Determining the Loop Gain of a Colpitts Oscillator

As an example of a more general and sophisticated application of this method

consider the SA/NE 602 IC Colpitts oscillator circuit that appeared in the March/April 2010 issue. In Appendix 1 of that article I argued that the impedance looking into the base of the transistor was so high that it could be approximated as an open circuit. For this reason it was possible to open the loop at the base of the transistor and ignore the loading effect of the base of the transistor on the feedback network, which simplifies the analysis of the oscillator circuit. The method presented here of determining loop gain through circuit simulation provides a means for verifying that assumption and validating the results presented in that article.

Figures 11 and 12 depict the schematic diagram of the Colpitts oscillator shown in Figure 2 of the previous article using the component values for the MF band oscillator shown in Table 1 of the previous article. The 2N2222 transistor is not the device used internally in the SA/NE 602 IC, but it is satisfactory for the purpose of conducting a circuit simulation to determine the loop gain in the MF band. The 1.75 μA current source was chosen to set the emitter current to 0.25 mA in order to provide the proper bias for the transistor. For the circuit in Figure 11 an ac sweep was conducted to obtain the loop current gain $T_i = i_y/i_x$ while for the circuit in Figure 12 an ac sweep was conducted to obtain the loop voltage gain $T_v = v_y/v_x$. Then the overall loop gain T was obtained through application of Equation A-1 and the phase and magnitude of T plotted as shown in the top and bottom plots respectively in Figure 13.

It is possible to examine the plots in Figure 13 in order to determine the resonant frequency f_o and the loop gain T at that frequency in the same way as was done for the loop gain results that were obtained from the Wein-bridge oscillator. These results are shown in Table 1 which compares the values of loop gain and oscillation frequency obtained through circuit simulation for the six values of the voltage boosting capacitor C with those presented in Table 3 of the previous article. As shown in the table the error between the calculated and simulated results for the loop gain are in error by no more than a few percent while the error between the calculated and simulated results for the oscillation frequency are in error by no more than a few tenths of a percent.

These results validate the assumptions detailed in the March/April 2010 article and confirm the accuracy of the formulas that were derived in Appendix 1 of that article.

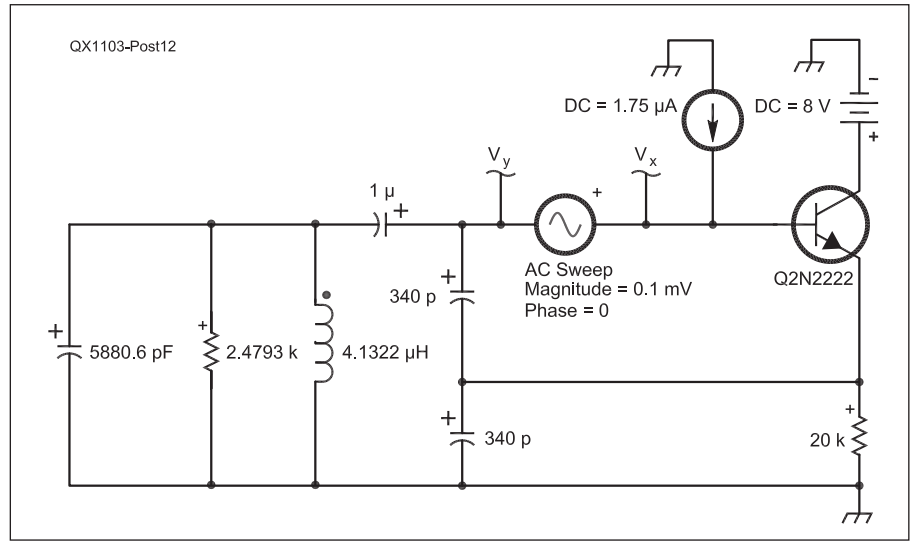

Figure 12 — Circuit simulation to obtain the loop voltage gain T_v of the Colpitts oscillator. In this case the loop is broken between the input of the amplifier and the output of the feedback network and an arbitrary voltage source is inserted in the loop.

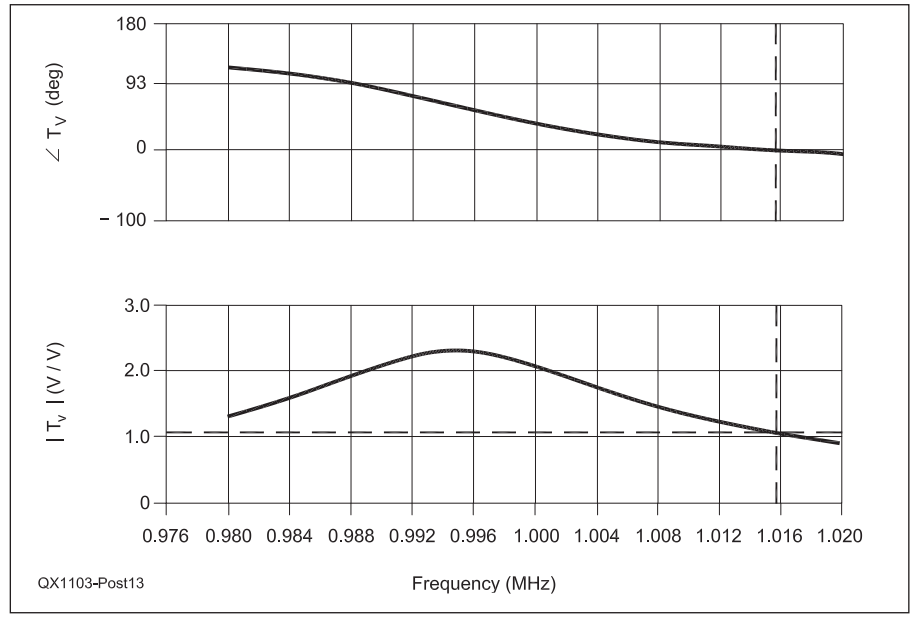

Figure 13 — Plot of Colpitts oscillator loop gain found by applying Equation A-1 to obtain the phase (top) and magnitude (bottom) of the loop gain T.

Conclusion

This article demonstrates that it is possible to apply circuit simulation techniques in order to determine the loop gain for feedback amplifiers that apply positive feedback. These results are useful to either investigate a feedback amplifier's performance or to confirm analytical results. This method was applied to determine the loop gain through simulation of dc, audio, and radio frequency circuits. In each case the error between theoretical predictions and the results obtained from simulations are no worse than a few percent.

John E. Post is an assistant professor of electrical and computer engineering with Embry-Riddle Aeronautical University in Prescott, AZ. He holds an Amateur Extra class license, KA5GSQ, and has BS, MS, and PhD degrees in electrical engineering.

Notes

[1]Comer, David J., *Modern Electronic Circuit Design,* Addison-Wesley, Reading, Massachusetts, 1976.
[2]Young, Paul H., *Electronic Communication Techniques*, 5th Edition, Pearson Prentice Hall, Upper Saddle River, New Jersey, 2004.
[3]Middlebrook, R.D., "Measurement of Loop Gain in Feedback Systems", *International Journal of Electronics*, vol. 38, no. 4, pp. 485–512, 1975.
[4]Tuinenga, Paul W., *SPICE: A Guide to Circuit Simulation and Analysis Using PSpice,* Prentice-Hall, Inc. Englewood Cliffs, New Jersey, 1988.
[5]Alexander, Charles K. and Sadiku, Matthew N.O., *Fundamentals of Electric Circuits,* 4th Edition, McGraw Hill, Boston, Massachusetts, 2009.

Appendix 1

Referring to the circuit on the right side of Figure 5, summing currents entering the bottom node gives

$$-g_{\mathrm{m}}v_{\mathrm{x}}+\frac{v_{\mathrm{y}}}{Z_{\mathrm{s}}}+\frac{v_{\mathrm{x}}}{Z_{\mathrm{f}}}=0. \qquad \textbf{Eq. A-2}$$

Then, rearranging Equation A-2 and solving for the loop voltage gain results in

$$T_{\mathrm{v}}=\frac{v_{\mathrm{y}}}{v_{\mathrm{x}}}=g_{\mathrm{m}}Z_{\mathrm{s}}-\frac{Z_{\mathrm{s}}}{Z_{\mathrm{f}}}. \qquad \textbf{Eq. A-3}$$

The overall loop voltage gain is $T=g_{\mathrm{m}}(Z_{\mathrm{s}}||Z_{\mathrm{f}})$. Modifying Equation A-3 to introduce this factor yields

$$T_{\mathrm{v}}=\frac{v_{\mathrm{y}}}{v_{\mathrm{x}}}=\frac{g_{\mathrm{m}}Z_{\mathrm{s}}Z_{\mathrm{f}}(Z_{\mathrm{s}}+Z_{\mathrm{f}})}{Z_{\mathrm{f}}(Z_{\mathrm{s}}+Z_{\mathrm{f}})}-\frac{Z_{\mathrm{s}}}{Z_{\mathrm{f}}}=\mathrm{T}\left(1+\frac{Z_{\mathrm{s}}}{Z_{\mathrm{f}}}\right)-\frac{Z_{\mathrm{s}}}{Z_{\mathrm{f}}}. \qquad \textbf{Eq. A-4}$$

Solving for the impedance ratio Z_s/Z_f gives

$$\frac{Z_{\mathrm{s}}}{Z_{\mathrm{f}}}=\frac{T_{\mathrm{v}}-T}{T-1}. \qquad \textbf{Eq. A-5}$$

Now referring to the circuit on the left side of Figure 5, by equating currents it is possible to express i_y as

$$i_{\mathrm{y}}=g_{\mathrm{m}}v_{\mathrm{x}}-\frac{v_{\mathrm{x}}}{Z_{\mathrm{s}}}. \qquad \textbf{Eq. A-6}$$

Then, applying Equation A-6 in order to solve for the loop current gain results in

$$T_{\mathrm{i}}=\frac{i_{\mathrm{y}}}{i_{\mathrm{x}}}=\frac{g_{\mathrm{m}}v_{\mathrm{x}}-\frac{v_{\mathrm{x}}}{Z_{\mathrm{s}}}}{\frac{v_{\mathrm{x}}}{Z_{\mathrm{f}}}}=g_{\mathrm{m}}Z_{\mathrm{f}}-\frac{Z_{\mathrm{f}}}{Z_{\mathrm{s}}}. \qquad \textbf{Eq. A-7}$$

Again, the overall loop voltage gain is $T=g_{\mathrm{m}}(Z_{\mathrm{s}}||Z_{\mathrm{f}})$. Modifying Equation A-7 to introduce this factor yields

$$T_{\mathrm{i}}=\frac{i_{\mathrm{y}}}{i_{\mathrm{x}}}=\frac{g_{\mathrm{m}}Z_{\mathrm{f}}Z_{\mathrm{s}}(Z_{\mathrm{f}}+Z_{\mathrm{s}})}{Z_{\mathrm{s}}(Z_{\mathrm{f}}+Z_{\mathrm{s}})}-\frac{Z_{\mathrm{f}}}{Z_{\mathrm{s}}}=T\left(1+\frac{Z_{\mathrm{f}}}{Z_{\mathrm{s}}}\right)-\frac{Z_{\mathrm{f}}}{Z_{\mathrm{s}}}. \qquad \textbf{Eq. A-8}$$

This time solving for the impedance ratio Z_f/Z_s gives

$$\frac{Z_{\mathrm{f}}}{Z_{\mathrm{s}}}=\frac{T_{\mathrm{i}}-T}{T-1}. \qquad \textbf{Eq. A-9}$$

Equating Equation A-5 and the reciprocal of Equation A-9 in order to eliminate the impedance ratio Z_s/Z_f produces

$$(T-1)^2=(T_{\mathrm{i}}-T)(T_{\mathrm{v}}-T). \qquad \textbf{Eq. A-10}$$

Finally, solving Equation A-10 for the overall loop gain T gives the desired result.

$$T=\frac{T_{\mathrm{v}}T_{\mathrm{i}}-1}{T_{\mathrm{v}}+T_{\mathrm{i}}-2}. \qquad \textbf{Eq. A-11}$$

QEX

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Network Control of the W8ZR StationPro II

Expand the capabitlity of this powerful device and control it over a LAN or even the Internet.

The StationPro II (SPII) is a powerful and flexible station switching device (Figure 1), allowing for selection of up to three HF transceivers (or classic separates), together with up to three HF power amplifiers per SPII device, all of which share a common antenna port.[1] As discussed in the original construction article by Jim Garland, W8ZR, additional SPII units can be networked together to create an even larger switching matrix.

Some operators may be interested in controlling the operation of their SPII devices over a local area network (LAN) or through a wide area network (e.g., Internet). Such control can be added internally to the SPII using a relatively inexpensive network control board and a homebrew interface board (IB). The SPII used at W9AC uses the CAI Web Control Board (WCB), available for approximately $35 from Amazon.com and other suppliers of network computer equipment. While it may be possible to add remote control capabilities to the simpler W8ZR StationPro I unit, additional circuit modifications may be required that go beyond the scope of this writing.

A significant feature of the WCB is that it contains a built-in Web server. Any computer with a Web browser on the network can access the SPII without the need for special control software or hardware interface to a computer. In fact, the SPII with its built-in WCB simply plugs into an open network router port. With a Web browser open, LAN or Internet access is easily accomplished through HTTP Port 80. A block diagram showing the integration of the SPII, WCB and IB is presented in Figure 2.

The WCB is capable of switching up to eight circuits through its TTL outputs although each output cannot directly switch a circuit like those used in the SPII. An interface board must be constructed to isolate the WCB's TTL outputs into a format suitable for switching the SPII's transceiver and amplifier select switch control functions. Either relays or optocoupling devices can be used for the interface. A schematic of an optically-coupled interface used at W9AC is

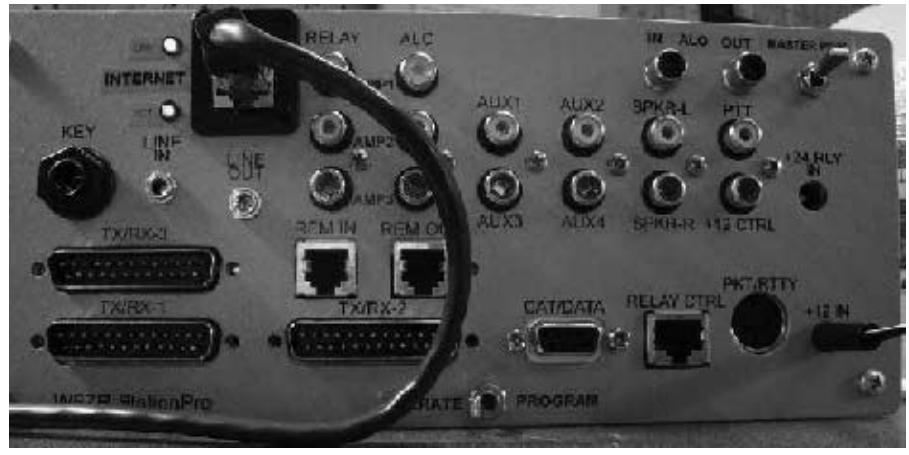

Figure 1 – The W8ZR StationPro II.

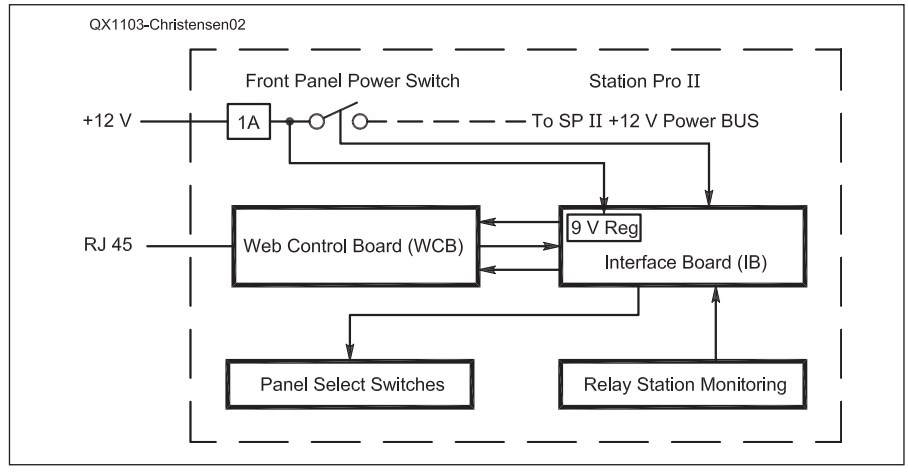

Figure 2 – A block diagram showing the integration of the SPII, WCB and IB.

[1]Notes appear on page 14.

shown in Figure 3. Moreover, the WCB can monitor the logic state of the SPII's transceivers and amplifier select relays, comprising a total of six circuits. Since the WCB can control and monitor eight circuits, an additional two circuits can be configured by the builder to control and/or monitor additional SPII functions. For example, I use the eighth control channel to turn on/off the SPII over the network.

Other functions are included with the WCB, including three analog-to-digital (ADC) input channels for voltage measurement, as well as input for temperature and humidity sensors. This write-up will not go into detail concerning these latter features; the discussion is limited to controlling the SPII's three transceivers and three amplifier select switch functions, in addition to the previously-mentioned remote on/off power control of the SPII.

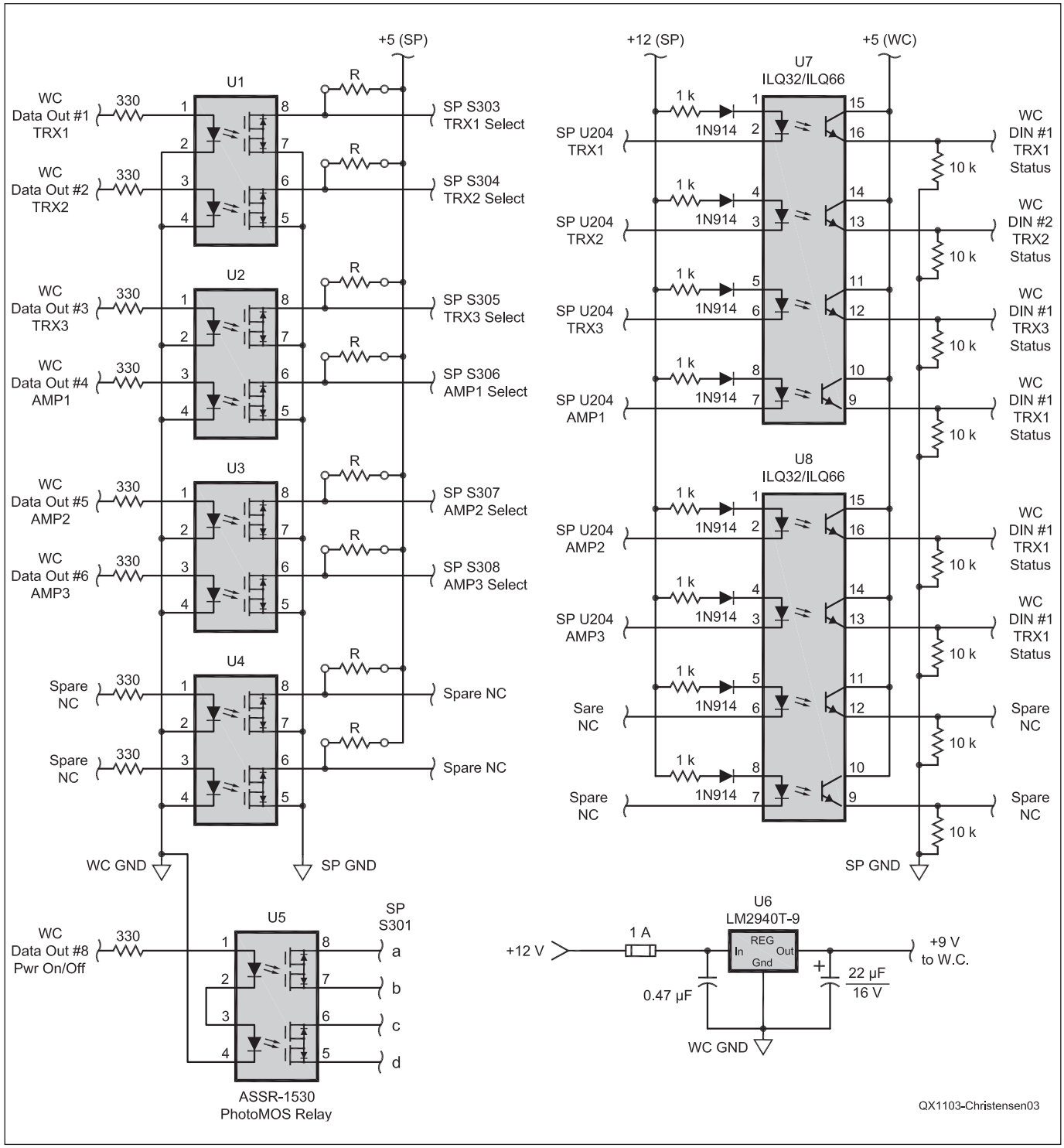

Figure 3 – A schematic diagram of the optically-coupled interface used at W9AC. U1 through U4 are ASSR-1228 or TLP627-2, TLP627-4 or equivalent. If TLP series are used, add pull-up resistors as shown at "R". Typical value is 100 kΩ at ⅛ W. U5 is an ASSR-1530 photoMOS relay. U6 is a 9V regulator and U7 and U8 are ILQ32 or ILQ66.

The SPII was designed such that a total of three SPII units can be networked together. However, my implementation of network control is limited to only one WCB on a multi SPII network. While it is certainly possible to add network control to each SPII used at a station, such control using the factory-default GUI may be awkward for users unless the WCB's firmware is re-programmed to better facilitate the switching function across multiple SPII units. Generally, users desiring Internet control will require a WCB within only one SPII unit on a multi-SPII network. Access on a multi-SPII network is then limited to three transceivers and three amplifiers.

Out of the box, the WCB uses a very basic GUI through a Web browser. The GUI was designed to allow its use in general-purpose switching applications where users have little or no programming skills. Any advancement of the GUI requires reprogramming of the WCB's firmware. However, the manufacturer provides a reasonably comprehensive programmer's guide for those users who desire to construct their own customized GUI interface. A copy of the programmer's guide is available for download from the manufacturer.[2]

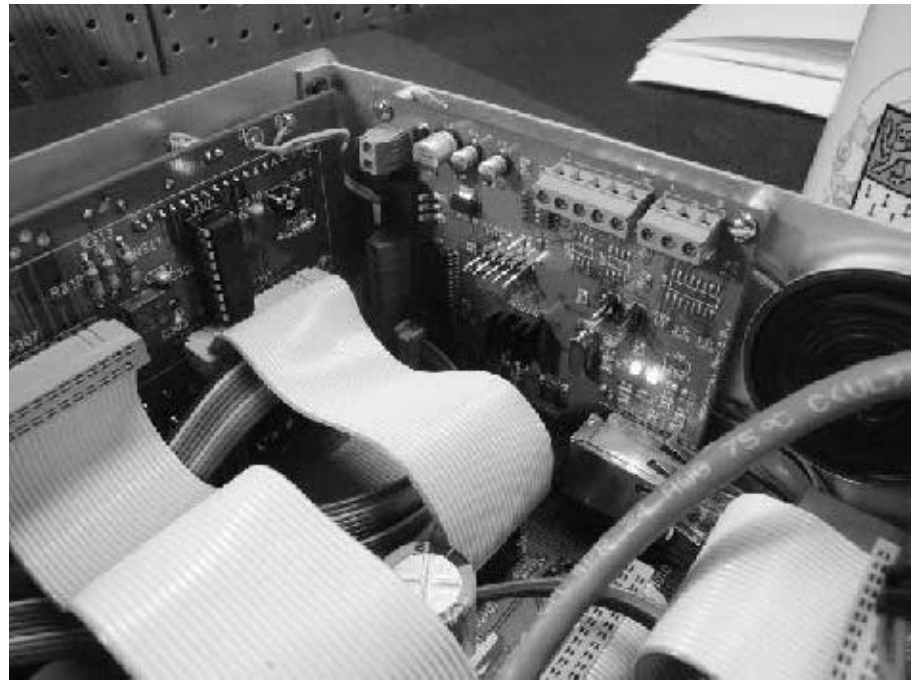

Figure 4 – The WCB's best location for mounting is on the SPII's left chassis panel

CAI Web Control Board Installation

The WCB uses an on-board +5 V voltage regulator and is powered by an input supply voltage between +6 and +9 V. The WCB's voltage regulator is rated for input voltages in excess of +12 V, but like most regulators, it is de-rated by the amount of the input/output voltage differential. Accordingly, an external regulator should be used when powering the WCB from the SPII's +12 V power source. The new regulator can be added on the homebrew interface board as discussed in the IB section. Power for the WCB is tapped between the SPII's 1A fuse and front panel power switch to allow for remote on/off power control.

As shown in Figure 4, most users will likely find that the WCB's best location for mounting is on the SPII's left chassis panel. Mounting against the chassis wall works well as ample room is provided for easy mounting, and mounting screws are hidden from view when the SPII's top and bottom clamshell covers are installed.

Once the WCB is mounted to the SPII's chassis wall with small ¼ inch-deep aluminum spacers, the WCB's input and output ports can be wired between the SPII and the homebrew IB. Multi-colored IDC computer ribbon cable was used for all powering and I/O connections. A photo of the IB appears in Figure 5.

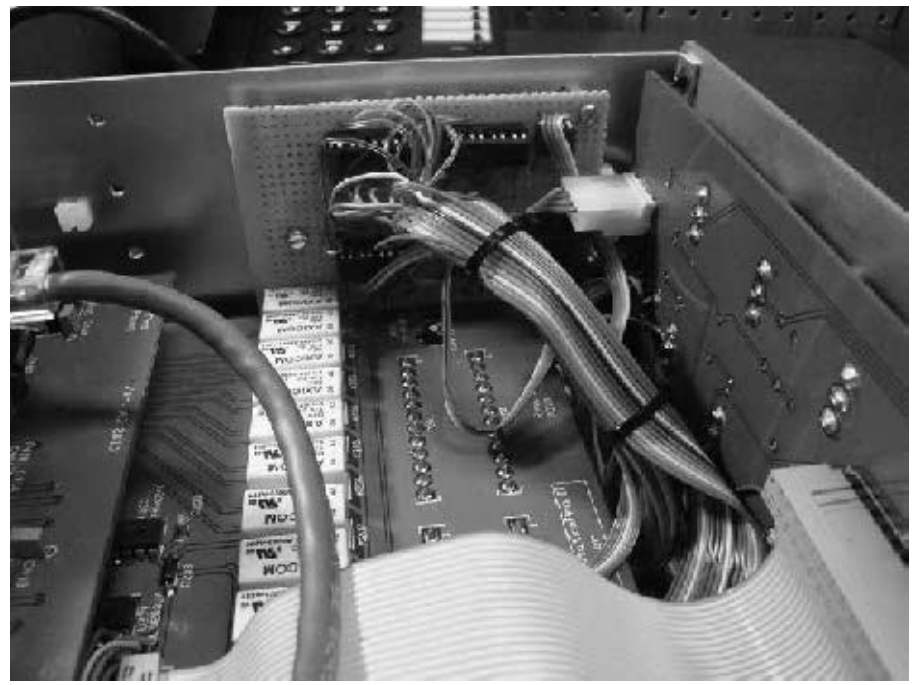

Figure 5 – A photo of the IB.

The IB as shown is constructed on Vectorbord® (4 x 3.5 inches) and contains a total of five photoMOS relays, two quad opto-Darlington couplers, and a +9 V low-drop voltage regulator. The IB is mounted on the right-side SPII chassis wall, opposite the WCB. A considerable amount of I/O wiring is required as evidenced in the photograph. For this reason, it's a good idea to keep wiring managed through the use of colored ribbon cables. Connection ports on the WCB are illustrated in the Figure 6.

From the diagram in Figure 6, it can be seen that a total of three connection ports are used with the WCB: In the lower-left, power is supplied from the IB's +9 V voltage regulator. J12 provides connectivity to the IB for SP-II status monitoring. Finally, the 10-pin output port is used to control the SP-II through the IB's optocouplers.

Connections between the IB and the

WCB's power and output ports are relatively easy using the supplied screw-down barrier strips. However, J12 uses a 16-pin DIP header. Pre-assembled header cables can be used with one end cut and terminated into stripped ends, or the builder can use a roll of multi-conductor ribbon cable, cut to the required length, and terminated into a DIP header socket.

The WCB has an integral RJ45 jack for Ethernet connectivity. I ran a 12-inch molded CAT-5e patch cable from the WCB to a panel-mounted RJ45 coupler/connector. Optionally, the builder may wish to run link and activity LEDs to the rear panel, in parallel with the existing LEDs as shown in the introductory photo.

Another option includes the addition of a "Master Power Switch" on the SPII's rear panel. Since the WCB is normally kept powered even when the SPII is powered down, the master power switch can be used in instances when it's desired to disconnect both the SPII and WCB.

Construction and Installation of the Interface Board (IB)

The IB is used as a buffered interface between the SPII and the WCB. Since the WCB's I/O utilizes TTL-based logic, an interface is necessary to adequately adapt logic levels between units. Although relays can be used as the interfacing mechanism, solid-state, optically-coupled devices have the advantage of long-term reliability, silent switching and low cost per switch pole.

From the schematic diagram, it can be seen that the IB is wired to the SPII's panel select switches for remote equipment selection as well as the SPII's relay control lines for status monitoring. The optical devices are all used to isolate these functions between the SPII and the WCB.

The IB can be constructed on Perfboard or preferably, "3-hole pattern" Vectorbord®, available from Mouser Electronics, DigiKey, and Newark Electronics. The board can be cut to approximately 4 x 3.5 inches.[3] My preference is the 3-hole pattern, with a ground bus that runs in between pin rows. This makes for easy placement of DIP-style ICs as well as convenient circuit ground connections. Also, a separate bus is interleaved for powering. Short of creating one's own printed circuit board, use of Vectorbord is highly encouraged as the IB wiring density is relatively high.

Three connection ports on the WCB are connected to the IB: (1) 2-terminal +9 V power connector; (2) 10-terminal strip for the digital output channels; and (3) a 16-pin IDC header connector at J12 for use with digital status input channels (i.e., monitoring the selection status of the transceivers and amps).

Connections to the digital status channels at J12 require a 16-pin female header connector and IDC ribbon cable. The builder can either construct the cable or purchase a ready-made IDC jumper cable, leaving one end exposed for connection to the IB.

U1-U4 utilize either ASSR-1228 photoMOS relays, or TLP627-2 (dual), or TLP627-4 (quad) photo-Darlington transistor arrays. If either TLP device is used, ensure that pull-up resistors are installed as noted on the schematic diagram.

Either ILQ32 or ILQ66 quad devices may be used at U7-U8. If these devices become difficult to locate, similar optocouplers or photoMOS relays can be used as substitutes.

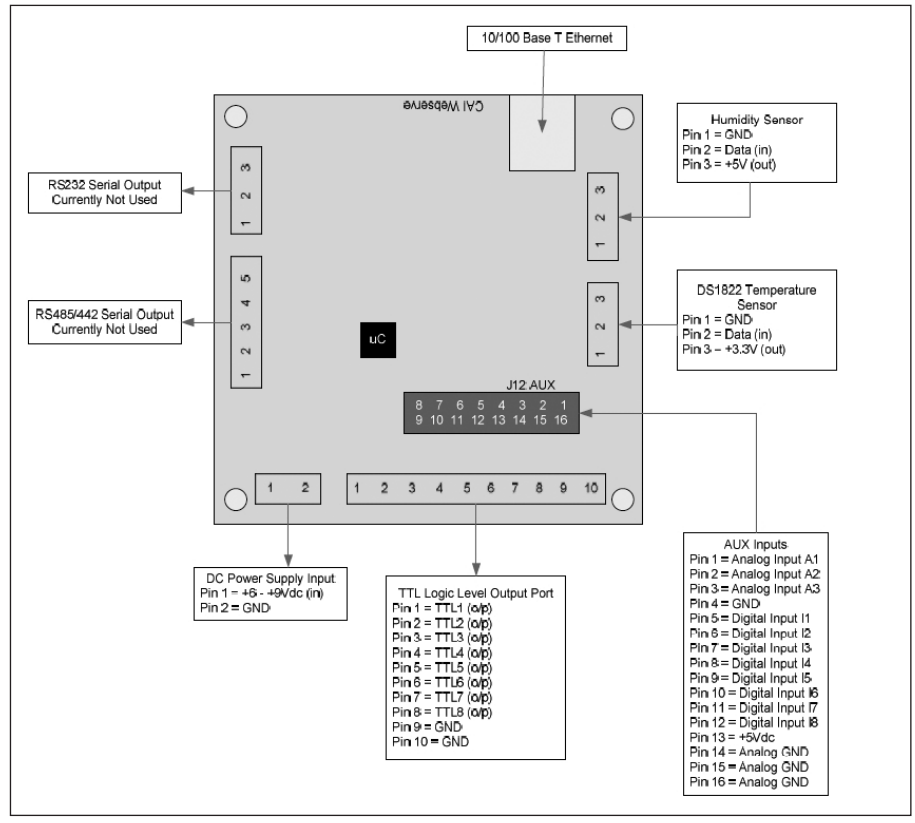

Figure 6 – Connection ports on the WCB.

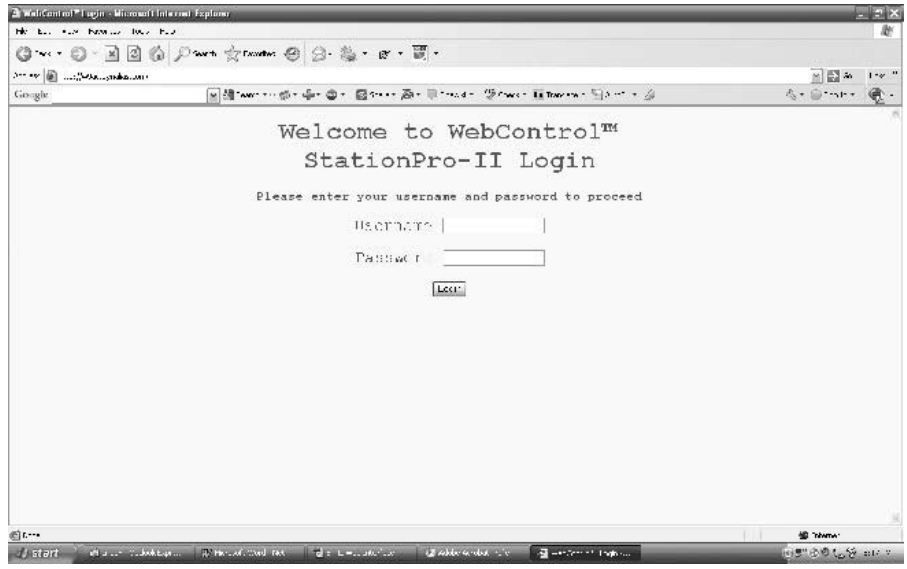

Figure 7 – The initial log-in screen.

U6 is a low-drop-out LM2940T-9 voltage regulator and is used to power the WCB from the SPII. Ensure that the input and output leads have noise-reducing bypass capacitors to circuit ground as shown on the schematic.

The ICs should be mounted directly over the ground bus strip on the Vectorbord. IC ground pins can be bent onto the ground bus, thereby eliminating the wiring between grounded ICs pins and the circuit ground points. With the exception of U5 (ASSR-1530), the remaining ICs can be socket-mounted. Troubleshooting during construction and installation is generally easier to facilitate when using IC sockets. Since U5 is in parallel with the SP-II front panel power switch, it switches a moderate amount of DC current and as such, this device should be soldered directly to the board.

Once the IB is constructed it can be mounted on the SP-II left chassis wall, opposite the WCB. Like the WCB, aluminum spacers should be used to elevate the IB from the chassis wall.

Network Control of the StationPro-II

As discussed in the preamble, the SPII can be controlled on a LAN or WAN network. No special software is required to access and control the SPII; a Web browser is used as a graphical controlling interface to select each transceiver and amplifier, and to power on/off the SPII. The WCB's Web server is simple in operation and the state of the channels is shown as a logic level. Once familiar with the screens, one can instantly determine the exact switching state of the SPII. As stated earlier, any advancement of the GUI requires reprogramming of the WCB's firmware.

The screen capture in Figure 7 displays the initial log-in screen. When first accessed, the user must enter the WCB's default UserID and password into the entry fields.

After logging-in, the Web server will take you to the master control status screen as shown in Figure 8. Several pieces of information become apparent. The status of all eight inputs and outputs is shown, as well as the network configuration. Notice that digital inputs are assigned either a "0" or "1." A "0" indicates that the SPII device (transceiver or amplifier) is currently off-line or that an amplifier is bypassed. A "1" indicates a device is active and on-line.

Clicking on the "Network" link opens the network set-up screen as shown in Figure 9. The WCB's default IP address is 192.168.1.15. You will need to either keep this address or enter a new static address that's compatible with your network IP assignments. On my network, the first 30 addresses are static. Addresses starting at 31 and continuing through 255 are dynamic.

Figure 8 – The master control status screen.

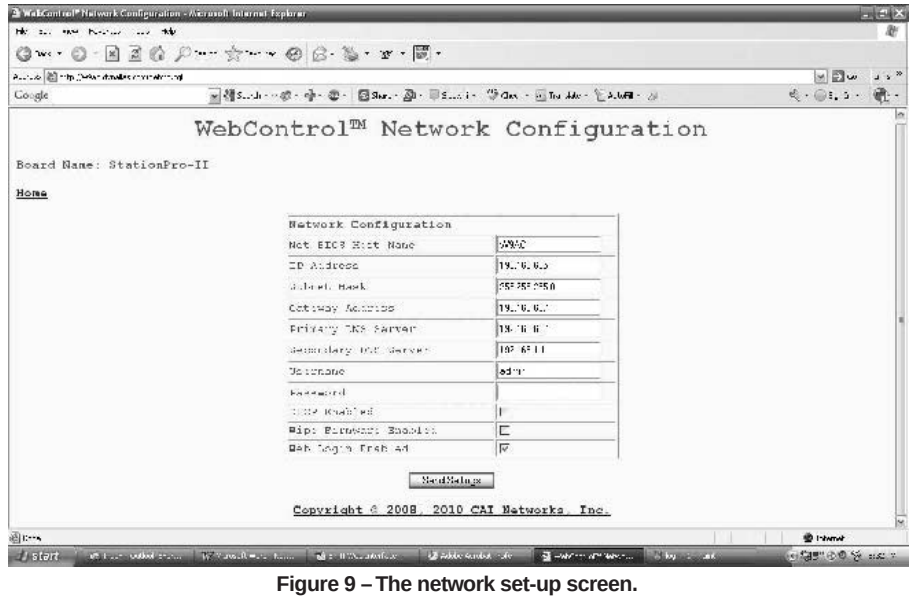

Figure 9 – The network set-up screen.

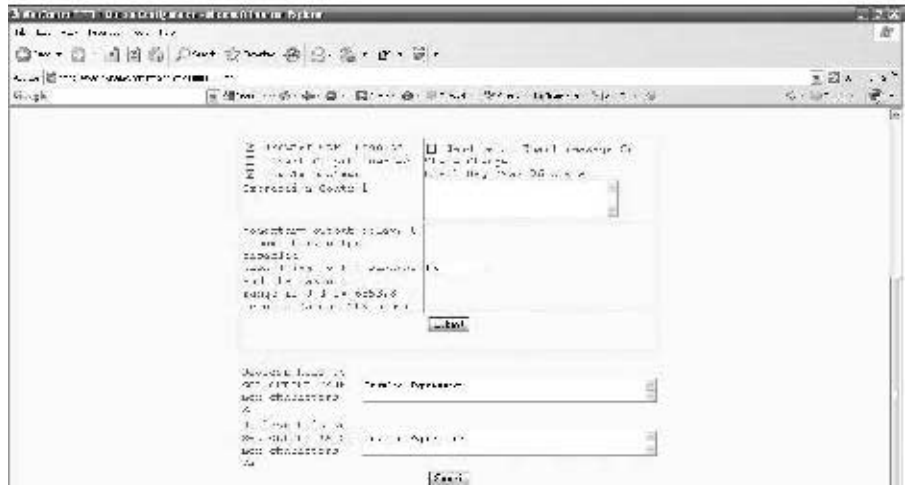

Figure 10 – The parameters of an output channel. Of particular importance, the second field allows for either a momentary or latching output state.

This allows for the upward scaling of the network as it grows — and also ensure that previously assigned IP addresses do not require re-assignment with static IP address growth.

The parameters of an output channel are shown in Figure 10. Of particular importance, the second field allows for either a momentary or latching output state. This output channel shows a half-second momentary pulse when activated. The momentary option should be used on all three transceiver and amplifier select channels.

The current input state of the active transceiver and amplifier is sampled from the SPII and displayed in Figure 11. Notice that input channels 3, 6, and 8 show a "1" logic state. This tells me that transceiver 3 (ch. 3), and amplifier 3 (ch. 6) are active. The same information is duplicated on the main status screen.

How is the SPII controlled on the network? Through the switching screen shown in Figure 12. Activating any transceiver or amplifier is as easy as clicking on the desired "On" button. Since transceiver and amplifier switching functions are momentary, the logic state will show as "0" since the state changes to "1" for only a half-second, with the duration determined by the output screen parameters as discussed earlier.

Other parameters of the WCB can be selected from the home page including pages for temperature and humidity sensor monitoring. Once programming or operation is complete, the user can remotely power-down the SPII and exit from the Web browser.

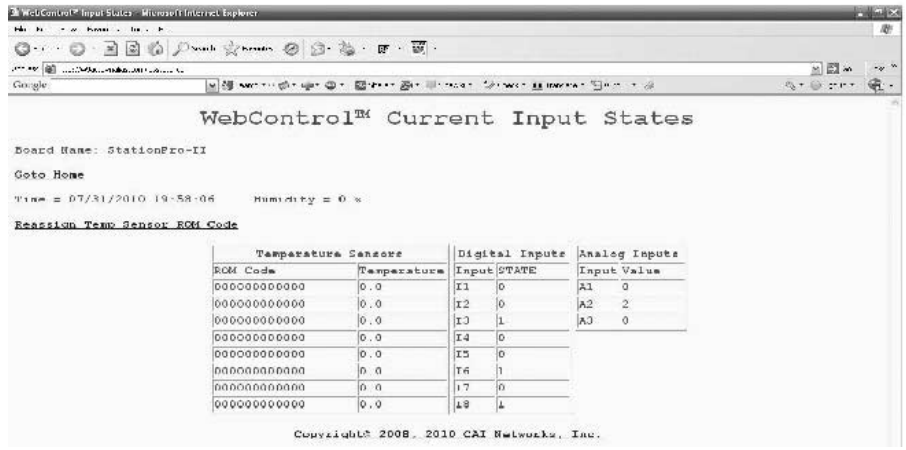

Figure 11 – The current input state of the active transceiver and amplifier is sampled from the SPII and displayed.

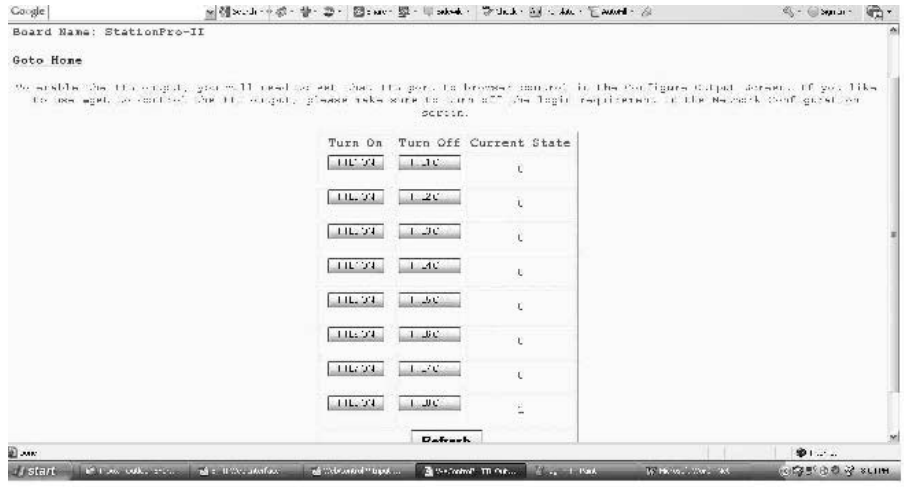

Figure 12 – The switching screen.

Conclusion

With the addition of an inexpensive network control board and a homebrewed logic interface, operation of the SPII on a computer network is easily accomplished. With the ability to select and control equipment over a local or wide area network, the completed project will give the user even more operating flexibility than that already provided by the stand-alone SPII.

Notes

[1]Garland, J.C., "The StationPro Master Station Controller", *QST*, August, 2010, pp. 30-34.
[2]**www.cainetworks.com/manuals/webcontrolWebControlUserGuide2-03-03.pdf**
[3]**www.vectorelect.com/**

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QEX

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The Effects of Ground Conductivity on Antenna Radials

Regardless of whether your vertical antenna uses elevated or buried radials, the conductivity of the soil beneath it has an important role to play.

In 1937 George Brown (later Executive Vice President of RCA) and his associates published the seminal paper, "Ground Systems as a Factor in Antenna Efficiency"[1] that described the results of their exhaustive investigation of buried radials under vertical antennas. This paper was so convincing that it was used by the FCC as the basis for rules governing the antenna systems that must be used with AM broadcast stations.

Twenty years ago John Frey, W3ESU (SK), Harry Mills, K4HU (SK) and I conducted a similar test program, but focused on *elevated* radials under vertical antennas. When he read the preliminary report of our findings, which resulted from more than 30,000 measurements, Dr Brown wrote,[2] "You men have done a superb job of inquiring into a difficult subject. You have revealed some new and important principles that must be published." The result was our IEEE paper[3] and our February, 1983 *QST* article.[4]

For the more than 20 years that have elapsed since our original test program I have had the nagging question: *Do buried or elevated radials provide the best ground system when used with vertical antennas?*

A search of the literature has failed to provide references to any investigations that might answer this question. The most comprehensive information that has been published is the excellent series by Rudy Severns, N6LF, in the Jan/Feb, Mar/Apr, May/Jun, July/Aug and Nov 2009 issues of *QEX* and in the March, 2010 issue of *QST*.[5] However, in his tests the radials were lying on the ground, rather than being buried, and thus do not exactly equate with those used by Brown.

[1]Notes appear on page 18.

Figure 1 – Our mesh ground screen in foreground, buried radials at center and elevated radials in the distance

That same early test program presented graphs showing that a direct correlation was found between the magnitude of return currents along elevated radials and the conductivity of the ground under them. However, no answer was given to another very pertinent question: *What effect does ground conductivity have on the performance of radials used as the ground system for vertical antennas?*

An answer to these questions might be derived by using a software program. But, being an old-fashioned and naturally suspicious ham, I wanted results that came from tests based on real-life conditions that took into account the vagaries of atmospheric propagation and factors such as ground conductivity, which must be guessed when a computer programs is used.

Test Site and Test Antennas

Adjoining my house is a cleared one acre field, which was a convenient location for antenna construction, as electrical power was available -- and it was close to dinner!

Three antennas were constructed in this field. Each consisted of identical 1/4-wavelength 10 meter verticals.

The first antenna was located over a 20 by 20 foot ground system consisting of aluminum mesh. This was the "standard" antenna that was to be used for comparison.

The second antenna was placed over 40 radials, buried 4 inches below the surface, on

a 20 by 20 foot square.

The third antenna is similar to the second, but the 40 insulated radials are elevated approximately 4 inches above ground level. (This is equivalent to counterpoise radials elevated almost 5 feet under a 160 meter vertical.)

The antennas are located two wavelengths apart, and careful tests have shown no interaction between adjacent antennas.

Figure 3 shows the VSWR of the antennas, as measured at the receiver. It is interesting to note that the antenna with the metallic mesh ground system, and the antenna with buried radials are both resonant at 28,600 kHz. However, the antenna with elevated radials is resonant at 28,500 kHz. This is a demonstration of capacitive bottom loading.[6] Here the capacity between the elevated radials and the ground is acting to "load" the antenna, and thus lower its resonant frequency. This is a phenomenon that has not been adequately described in the literature.

Ground conductivity was 1.97 milliSiemens/meter. Ground conductivity was measured at the center antenna — after it had been determined that the conductivity under each antenna was identical.

The logistics of the test program were somewhat intimidating. For example, it took three men half a day to level and prepare that area for the three antennas. A garden edger was used to make the slits needed to bury the radials of the second antenna. The edger is 6 inches wide. To bury the 480 feet of radials I had to step on the edger 960 times! To compare the three antennas a switching system was required. I could find no commercially available coax switch that switched both the center conductor and the braid, as had to be done for these tests. As a result, I derived an arrangement that only a ham could appreciate — it features microswitches soldered to coax fittings! Not pretty, but it works perfectly and allowed a test program that could not be accomplished otherwise.

Finally, more than 1,000 feet of coax was required to connect the antennas to the remote receiver.

Figure 2 – The antenna base brackets were welded to the radial wire collection plates.

Instrumentation

A considerable amount of thought was given to deciding how to test the three antennas. It was obvious that test results could not be based on signals transmitted by the three test antennas, as results would then depend on signal reports from other amateurs. As is eloquently described by Greg Ordy, W8WWV in his extensive papers[7] on "S Meter Blues," S meters in amateur equipment are notoriously inaccurate, S meter calibration varies widely from manufacturer to manufacturer and none of them seem to follow Technical Recommendation R.1 of the International Amateur Radio Union (IARU).[8] This recommendation defines S9 for the HF bands to be a receiver input power of –73 dBm. This is a level of 50 µV at the receiver's antenna input, assuming that the receiver's input impedance is 50 Ω.

In practice this is really not a problem. An S meter reading is influenced both by the level of the received signal and the gain of the antenna being used and thus means nothing in absolute terms. Also, the amateur community does not really depend on S meters; indeed, many of us send nothing but 59 reports, especially during contests or when contacting rare DX stations!

As the result of these factors it were decided to base the published results of this test program on the comparative signal strengths received by the three test antennas on a carefully calibrated receiver. To perform this calibration, a General Radio bridge oscillator and a precision step attenuator were used. The results indicated that a signal level of S0 on my ICOM 756 ProIII receiver was 31dB below the level needed to achieve S9, rather than the 54 dB that could have been expected if the IARU Recommendation had been followed.

The next problem was to make the S meter more visible. This was accomplished by, once again, turning to the exacting studies by Greg Ordy, W8WWV, and his computer program *S Meter Lite*. This program allows the S meter output of a receiver to be seen as a bar graph on a computer screen. With the setup used for these tests this resulted in a 9-inch-long bar graph that allowed great accuracy in reading signal strength.

One consideration that made testing easier was that it was not necessary to measure absolute signal strengths. Rather, what was required was an accurate measurement of the *differences* between the signals received by the test antennas. Thus, losses such as those in the 375 feet of coaxial cable feeding each antenna were not a factor as each antenna was physically identical and they are fed by identical lengths of identical coax.

Comparison Testing Procedures

Three different methods of comparing the performance of the three antennas were considered.

Receiving Tropospheric Signals

When using a receiving system that will read signal strengths with an accuracy of less than 0.2 dB it is virtually impossible to take useful readings of tropospheric signals, which are subject to the several dB QSB variations usually found on 10 meters. However, an unsuccessful attempt was made to obtain a subjective evaluation of the differences between the performance of the test antennas.

Receiving Ground Wave Signals

Ground wave signals can be visualized as sine waves with their peaks one wavelength apart. My friend and neighbor, Bob Evans,

W7RR, suggested that we investigate this effect. Bob mounted a 10 meter transmitter in his pickup, which was located about 1000 feet from the test antennas. While I checked received signal strength, he slowly drove one wavelength toward and away from the test antennas. Received signal strength changed by 11 dB and I could tell, by the change in signal strength, when the truck moved only a few inches!

The problems of trying to use ground wave signals was perfectly demonstrated when Jim Cassidy, KI7Y kindly provided test signals from his home, which is 19.2 miles, line of sight, from the test antennas. In this case the test antenna having buried radials showed a received signal that was 10 dB higher than that received from the test antenna operating over an aluminum mesh "perfect" ground system. Obviously, this was impossible!

These tests illustrated that comparison testing of two or more antennas using ground wave signals can only be done on a carefully designed antenna test range where the receiving antennas are each *exactly* the same distance from the signal source.

Using Atmospheric Noise as a Signal Source

By far the most accurate evaluation of the performance of the three test antennas was accomplished by employing an unusual procedure: using atmospheric noise as a signal source.

Atmospheric noise is the result of the very broadband electromagnetic impulses that are caused, primarily, by the 100 lightning flashes that occur every second somewhere in the world.[9] These impulses (sometimes called "Sterics" or "Spherics") may propagate for thousands of miles from the lightning source without major attenuation in the Earth-ionosphere waveguide.

Antennas operate by intercepting electromagnetic waves (including those created by lightning) and converting them into electrical current for the receiver to amplify and detect. Thus there is a direct correlation between atmospheric noise levels and the signal strengths indicated by a communications receiver.

Atmospheric noise, when measured at 30 MHz on my ICOM 756 Pro III, with both preamps operating, was entirely adequate to allow precise signal measurements. As these atmospheric signals are stable in the short term, they allow received signal strengths to be read with great accuracy.

To make sure that the polarity of atmospheric noise was suitable for tests with vertical antennas I built a dipole antenna that was resonant at the test frequency of 28.6 MHz. This antenna was then tested with its center approximately 10 feet above the ground. Received signal strength from this antenna was 11.7 dB higher when in the vertical position than it was in the horizontal position.

It was interesting to find that there are constant minute variations in the signal strength of atmospheric noise, as shown in the following 45 second scan — provided by the *S Meter Lite* software. Testing these variations caused no problem, as the software program allows the viewing of signal strength over extended time frames. I used 2 seconds. Thus, great accuracy is possible.

During a month's observation I have also noted hour-to-hour and day-to-day variations (an 8 dB maximum excursion during a month-long observation), as might be expected from the extensive literature available.[10,11,12]

Test Results

• **Tropospheric Signals**

No differences could be detected — by ear – between the performance of the antenna with buried radials (#2) and the one having elevated radials (#3).

• **Ground Wave Signals**

For the reasons described above, it was not possible to obtain any reliable data on the performance of the test antennas using ground wave signals.

• **Atmospheric Noise Signals**

As noted, lightning-induced electromagnetic radiation proved to be an excellent signal source, 24 hours a day, and produced accurate test data.

The original 100 tests were conducted at the end of a typically beautiful Oregon summer, with not a drop of rain for eight weeks, followed by light sprinkles. Ground conductivity was correspondingly low (1.97 milliSiemens/meter).

• **With ground conductivity ranging from 2 to 4 milliSiemens/meter**…

A ground system consisting of 40 *buried* radials under a ¼ wavelength vertical antenna provided 3.45 dB less signal strength than an identical antenna located over a solid metallic mesh ground system.

A ground system consisting of 40 *elevated* ("counterpoise") radials under an identical antenna provided 2.27 dB less signal strength than an identical antenna located over a solid metallic mesh ground system.

Thus, a ¼ wavelength vertical antenna using 40 elevated counterpoise radials as a ground system will provide 1.18 dB more

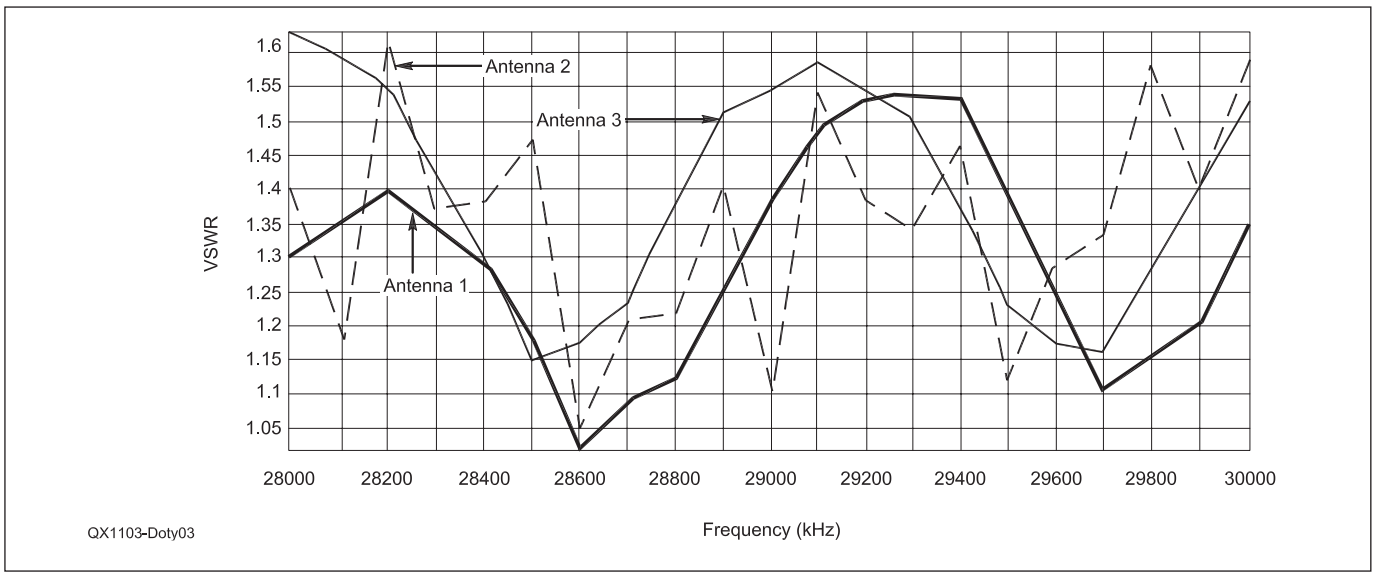

Figure 3 – The VSWR profiles of the three antennas as measured at the receiver.

signal strength than an identical antenna using 40 buried radials as a ground system.

At the conclusion of those tests we had 3 inches of rain over a three day period. This resulted in 30% increase in ground conductivity — and a startling, and unexpected, change in the performance of the antennas with buried and elevated radials.

• **With ground conductivity above 4 milliSiemens/meter**…

A ground system consisting of 40 *buried* radials under a ¼ wavelength antenna provided 4.72 dB less signal strength than an identical antenna located over a solid mesh ground system.

A ground system consisting of 40 *elevated* "counterpoise" radials under an identical antenna provided 4.99 dB less signal strength than an identical antenna located over a solid mesh ground system.

Thus a ¼ wavelength using 40 buried radials as a ground system will provide 0.28 dB more signal strength than an identical antenna using 40 elevated radials as a ground system.

Note that these results are exactly opposite those found when the antennas were operating over lower conductivity ground.

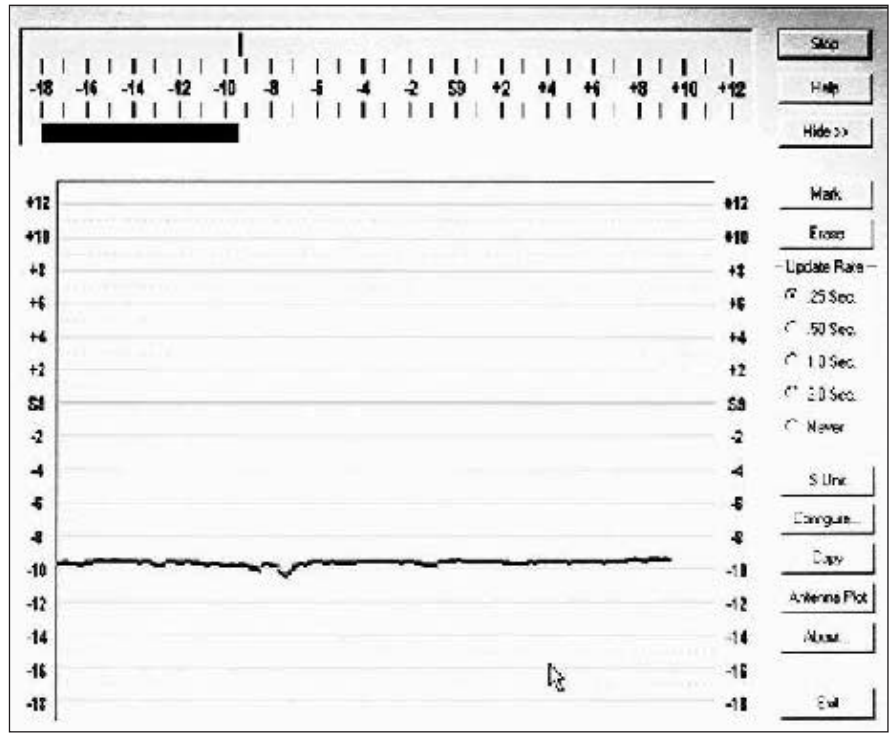

Figure 4 -- It was interesting to find that there are constant minute variations in the signal strength of atmospheric noise, as shown in this 45 second scan provided by the *S Meter Lite* software.

Overview

The radical change in performance shown above for radial ground systems operating with differing values of ground conductivity appears to be unprecedented. I do not believe that this phenomena has been described in previous Amateur Radio or IEEE literature.

Many years ago I had an interesting discussion about our work with elevated, or counterpoise, radials with George Brown in his Princeton, New Jersey home. In this discussion Dr Brown offered the thought that elevated radials might be expected to be more efficient because they collect return currents before they reach the ground. By comparison, buried radials collect these currents after they have entered the ground and thus had to flow through earth, which usually has considerable resistance to current flow, before being collected by the buried radials.

From the work described above it appears that there is a point where a higher level of ground conductivity actually assists buried radials in collecting return currents. It is hoped that this report will initiate further research in this area and allow for the development of a precise explanation of this unusual phenomena.

Acknowledgements

This test program ended up being, to a good degree, a communal project, with significant, useful and very much appreciated input from:

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Bob Evans, W7RR, who contributed greatly with his years of knowledge from his AT&T and Amateur Radio experience.

Jim Cassidy, KI7Y, who donated his time to help with the ground wave evaluation.

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Barry Boothe, W9UCW, for proofreading this article and suggesting appropriate corrections.

Arch Doty, W7ACD, is a Life Member of the ARRL. When not experimenting with antennas he is an avid DXer, having earned "No 1 DXCC," and having operated from 28 overseas countries using reciprocal licenses. Arch is a former Director of QCWA, the Radio Club of America and the US Marconi Foundation. He is a Senior Life Member of IEEE and has been a member of the IEEE Antenna and Propagation Society for more than 30 years. Arch lives near the top of a small mountain near Portland, Oregon with his tolerant wife, Adah, and two Golden Retrievers who delight in helping with outdoor antenna tests.

Notes

[1]Brown, Lewis and Epstine, "Ground Systems as a Factor in Antenna Efficiency," *Proceedings of the IRE*, June 1937.

[2]Personal correspondence, George Brown to Arch Doty, Jr. 1981.

[3]Doty, Frey and Mills, "Characteristics of the Counterpoise and Elevated Ground Screen", Professional Program, Session 9, Southcon'83 (IEEE), Atlanta, GA, January 1983.

[4]Doty, Frey and Mills, "Efficient Ground Systems for Vertical Antennas," *QST*, Feb. 1983, pp 20-25.

[5]R. Severns, N6LF, "An Experimental Look at Ground Systems for HF Verticals," *QST*, March 2010, pp 30-33.

[6]Greg Ordy, W8WWV, *W8WWV's S Meter Lite* software, **www.seed-solutions.com/gregordy/Software/SmeterLite.htm**.

[7]International Amateur Radio Union Region 1 (1981) Technical Recommendation R.1, Brighton, England, UK.

[8]A.C. Doty, Jr.,"Capacitive Loading of Vertical Antennas", **www.w7acd.com**, 2009.

[9]"Atmospheric Noise" **http://en.wikipedia.org/wiki/Atmospheric_noise**

[10]D.C. Lawrence, "CCIR Report 322 Noise Variation Parameters", NRaD Technical Docunent 2813, Naval Command, Control and Ocean Surveillance Center, San Diego, CA, June 1985.

[11]Spaulding and Washburn, "Atmospheric Radio Noise: Worldwide Levels and Other Characteristics", NTIA Report 85-173, US Department of Commerce, Washington, DC, April 1985.

[12]C.J. Coleman, "The Directional Aspect of Atmospheric Noise and its Impact Upon HF Communications Systems", The University of Adelaide, South Australia.

QEX

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Converting a Vintage 5 MHz Frequency Standard to 10 MHz with a Low Spurious Frequency Doubler

Presenting a very clean frequency doubler and an excellent example of a method to design a clean Class A amplifier.

Introduction

In this article I describe the design, construction, and test of a quadrature driven mixer frequency doubler and an output amplifier having exceptionally low spurious levels. A major feature of the design is that low spurs are achieved without use of any high Q filters. The circuit was developed to obtain a 10 MHz output from a vintage Vectron[1] FS321A-1 5 MHz frequency standard. This filled a need in my lab because some test equipment made in the past 20 years or so will only accept a 10 MHz external frequency reference. In addition to making the old frequency standard useful, this project provided an interesting opportunity to quantify the conversion loss and spurious rejection performance potential of a quadrature driven mixer frequency doubler. The design required a highly accurate –90 degree phase shift network. Included is information on how to design these networks for the more general case. A spreadsheet that automates the phase shift network design is provided on the *QEX* website: **www.arrl.org/qexfiles**. Sufficient design data and test results are presented so others may be able to adapt it to their application.

Frequency Standards

The Vectron FS321A-1 pictured in Figure 1 is typical of metrology lab frequency standards used until they were supplanted by Cesium and Rubidium stabilized oscillators. Today the availability of rubidium stabilized frequency standards at low cost has resulted in the retirement of old, but excellent, quartz oscillators. Often they can be found on the surplus market at very attractive prices.

Figure 1 – The complete 10 MHz Frequency Standard distribution system. The 10 MHz output from the modified Vectron FS321A-1 frequency standard is sent to as many as 12 loads by the Precise Time and Frequency, Inc. Model 1203C distribution amplifier.

Historically many industrial standards labs maintained these precision crystal oscillators as the "working standard" for periodic calibration of the crystal oscillators in frequency counters, synthesizers and other test equipment. The local frequency standard was calibrated using standard frequency signals broadcast from the National Institute of Standards and Technology (NIST). As most hams know, these signals are broadcast by WWV on HF and by WWVB at 60 kHz. Even 50 years ago, by using the phase stable signals from WWVB,[2,3] the frequency precision obtainable was as good as 1 part in 10^{12}. References 2 and 3 are links to the NIST library that is a source of fascinating history of the subject.

The HP 105A, Austron 1250A, Sulzer 5A and Vectron FS321A-1 are examples of precision crystal frequency standards from that era. These units typically featured double ovens with highly stable proportional temperature control. Many featured back up batteries to maintain stable operation during power interruptions. When introduced, these oscillators represented the state of the art in stability and aging rate. Even by today's standards they are *very* stable. Over time, aging rates improved from 5 parts in 10^9 per day to 1 part in 10^{12} per day by the early 1960s.[4] As crystal technology improved, the operating frequency of the oscillators was increased to gain advantages in aging rate and stability. Initially 100 kHz was the "standard." As time went on, frequencies of 1.0, 2.0, 2.5, 5 and finally 10 MHz came into use as higher frequency crystals provided improved per-

[1]Notes appear on page 33.

formance. To maintain compatibility with the ubiquitous "Frequency Reference Input" provided on many high quality instruments, the later frequency standard boxes provided internal dividers. For example, a 5 MHz standard might also provide reference outputs at 1.0 MHz and 100 kHz for backward compatibility with older instruments.

Often the local frequency standard signal was distributed throughout a lab from a multiple output "distribution amplifier" via coax lines to directly drive instruments. Figure 1 also shows the Precise Time and Frequency, Inc. Model 1203C[5] distribution amplifier I use to distribute the 10 MHz reference signal from the modified Vectron oscillator. It accepts one input and provides twelve buffered 10 MHz, 50 Ω outputs to test equipment or other gear.

The instrument makers sometimes provided means to phase lock their internal time bases to one or more of the common reference frequencies. For example my HP5345A counter uses an internal 10 MHz time base; but it will accept external reference signals of 1, 2, 2.5, 5, or 10 MHz. However, not all equipment is that versatile. Some of my test gear will accept only 10 MHz. Thus the present project was born.

Why a Quartz Frequency Standard

I have a (one time) GPS calibrated rubidium frequency standard that uses a surplus rubidium oscillator assembly, so why bother with a quartz-based frequency standard? For one thing, I hate to see a piece of really good old hardware retired, a personal failing perhaps, and also because a standards lab quality quartz oscillator is really quite good. But the main motive is that quartz oscillators are not prone to wear out; in fact, their stability improves with age. Rubidium standards do have a finite (if long) lifetime.[6] In the case of my surplus rubidium stabilized oscillator, I have no idea how many hours were accumulated before it came into my hands. Running it continuously when its full accuracy is not required seems unwise. Until I can implement a NIST traceable external reference, my approach is to use the rubidium oscillator as the local "calibration standard." It is only fired up for periodic calibration of the quartz frequency standard. The rubidium oscillator is run for 24 hours to fully stabilize. Then, the continuously running quartz oscillator is checked against it. This procedure minimizes the aging rate and extends the useful life of the rubidium oscillator.

Vectron FS321A-1 Frequency Standard

I found my Vectron oscillator on the surplus market. From the description and photos I concluded that it had a double oven and thus was a very high quality unit. The description indicated the 100 kHz and 1 MHz outputs came on at once but that about 10 minutes was required for the 5 MHz output to come up. This I took as a clue that there might be a very narrow band crystal filter in the 5 MHz output, perhaps for phase noise clean up. (The output could only pass through the filter when the ovens were heated and the oscillator was on frequency). This turned out to be the case. I did find the filter. No operating manual or data sheet was received with the unit, but according to a calibration sticker it was last calibrated in October 2008. So far, so good.

Figure 2 is a partial block diagram I created after poking around in the oscillator cabinet. It had several assemblies to which I have assigned my own names for convenience. I found a battery charging power supply that provided an unregulated output of roughly 26

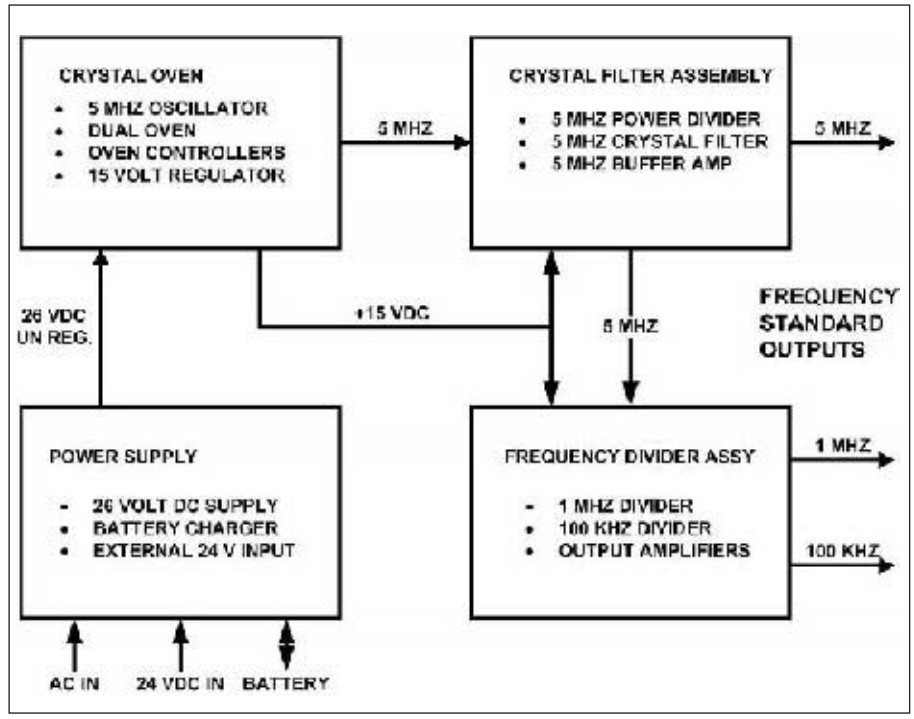

Figure 2 – A Partial Block Diagram of the Vectron FS321A-1 5 MHz Frequency Standard. The +15 volt regulator is contained within the crystal oven.

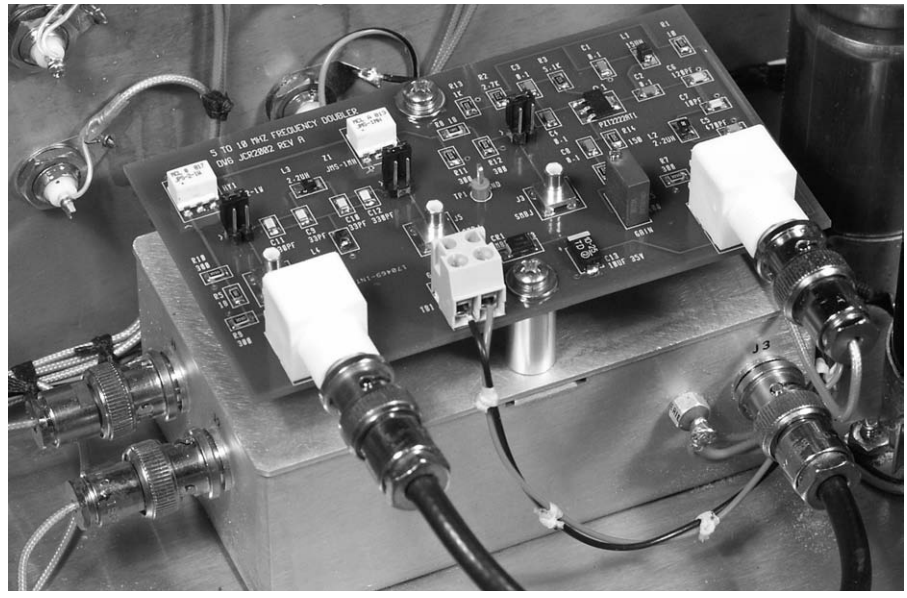

Figure 3 – The Frequency Doubler PCB mounted on top of the Filter Assembly in the Vectron FS321A-1 Frequency Standard. The 5 MHz output cable is removed from J3 on the filter assembly and connected to J2, the 10 MHz output of the Doubler PCB. An RG-58 jumper routes the 5 MHz signal at J3 to the 5 MHz input, J1, on the Doubler PCB.

Table 1
Frequency Doubler Specification

Requirement Description	Specification	Comment	Reference
5 MHz Power Input	+16 dBm into 50 Ω	Measured 5 MHz power output of Vectron Frequency Standard	
10 MHz Power Output	+13 dBm (1Vrms) into 50 Ω	Requirement derived from input/output specification of comparable distribution amplifiers and instruments	7, 8, 9
Gain Adjustment	+/- 3 dB	To trim 10 MHz output from doubler to +13 dBm	
Suppression of Harmonic Distortion	Minimum > 40 dBc Goal > 50 dBc	Comparable Frequency Standard and distribution amplifier specifications	7, 8, 9
Load Sensitivity	Output Stable into any Load including short or Open circuits	Instrument terminations may not be 50 Ω loads	
Power Supply Voltage	+15V +/-3V	Operation on +12V may be desirable in other Applications	
Power Supply Current	< 25 mA @ 15V	Estimate of safe current available from +15V Supply regulator in the FS 321A-1	

V. This was used to charge a backup battery of NiCd D cells that had long since died. The un-regulated battery or 26 V power was sent to the crystal oven assembly. There was also a terminal block and switch on the rear panel to enable an external 20 to 28 V dc power source to be used. As it turned out that suited my needs exactly. I had 24 V backup power available.

The crystal oven assembly was about 6 by 4 by 4 inches and to my surprise contained a 15 V regulator that accepted the unregulated 26 V input and provided a +15 V output to the crystal filter assembly and the frequency divider assembly, as well as for internal use. Apparently the idea was to stabilize the 15 V supply by placing it in the oven, but I don't really know. The 5 MHz output from the crystal oven was routed to the crystal filter assembly. It is the small box under the doubler printed wiring board in Figure 3.

At the crystal filter assembly a resistive power divider taps off a sample of the 5 MHz signal and routes it to the Frequency Divider Assembly. The remaining 5 MHz signal goes to a glass encased crystal, that I believe is a simple crystal filter. From the crystal, an output amplifier increases the signal level to 16 dBm and routes it to the front and rear panel BNC connectors.

As shown in Figure 2, the Frequency Divider Assembly accepts the 5 MHz input and outputs 100 kHz and 1 MHz. The frequency divider was a surprise. The outputs are sine waves and there is not an analog or digital IC anywhere in sight. The dividers are one form or another of the analog frequency dividers used before the advent of digital ICs. The outputs are clean sine waves that are routed to the front and rear panel BNC connectors.

Not shown in the block diagram are metering circuits for the 100 kHz, 1 MHz and 5 MHz output voltages, the +15 V regulator, the backup battery and also for the status of each oven. A ten-turn pot on the front panel is provided for fine adjustment of the oscillator frequency during calibration.

Old equipment is always intriguing; I would like to explore the box in more detail, if only to understand the analog frequency dividers, but with no manual or schematic, one has to be careful not to break some irreplaceable component. There are no useful date stamps, but from the discrete technology the unit appears to be between 40 and 50 years old. If so, the crystal is "well aged" and should be quite stable.

Frequency Doubler Design Requirements

Prior to starting this design, specifications were developed by measuring the performance of the Vectron Frequency Standard. Other electrical specifications were derived from catalog specifications for distribution amplifiers, other frequency standards, and test equipment instruction books. The requirements are summarized in Table 1 along with the source of the specification. Most lab frequency standards seemed to output about 1 Vrms into a 50 Ω load. Distribution amplifiers are designed to accept that input and are either unity gain or provide gain adjustable outputs that can be set to 1 Vrms. The instruments I looked at do

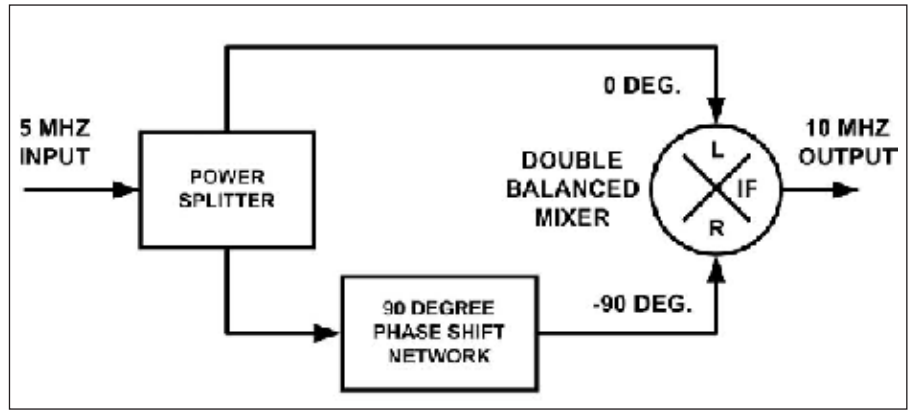

Figure 4 – The basic frequency doubler consists of an in-phase power divider, a 90 degree phase shift network, and a double balanced mixer. The phase shift may be either +90 or –90 degrees. In this design –90 degrees was used. The phase shift may be introduced into either the LO or the RF port of the mixer.

not always provide a 50Ω termination, however they often specify a 1 Vrms, 50 Ω source for the reference input.

For my design I wanted to install the frequency doubler within the Vectron cabinet and to power it from the existing +15 V supply. The current available was unknown so the doubler current draw was to be minimized. For ease of construction, use of surface mounted parts was also a desirable feature.

Phase noise was not specified, as I had no convenient means to measure it other than a spectrum analyzer. Additionally, my goal was to provide a common accurate frequency reference for test equipment, and not specifically to stabilize the LO of a sensitive receiver.

Design Approach

At first, I considered using the classic Class C push-push doubler circuit. In the push-push circuit the bases of two bipolar transistors are driven in push-pull and the collectors connected in parallel. The fundamental frequency and the odd harmonics are cancelled in the paralleled collectors by the balanced drive. Generally, a resonant filter is used in the collector circuit to reconstruct the second harmonic and suppress the higher order even harmonics. Using quite ordinary bipolar transistors, the basic scheme is capable of odd harmonic suppression of more than 30 dB, and power gains of 10 dB or so up to UHF.

After a couple of quick designs of two pole band-pass filters for 10 MHz, it was obvious that the unloaded Q required for the inductors was incompatible with the small surface mount parts I had in mind. Additionally, the last thing I needed was a lot of power gain. The overall circuit was to have a loss of 3 dB. With +16 dBm of drive available, a passive doubler followed by a low distortion amplifier seemed the better choice.

Figure 4 is a block diagram of the doubler approach. When a double balanced mixer is driven with a 90 degree phase difference at the RF and LO ports, the IF port output is (ideally) 0 V dc and the second harmonic of the input frequency. The basic idea has been implemented many times using diode mixers, analog multipliers, and exclusive OR gates. If the configuration has a specific name, I have never run across it. So I call it a Quadrature Driven Mixer Doubler, or QDMD for short. I found many references on the Web showing variations of the basic idea. The IEEE digital library had a lot of documents related to specific implementations, but within my time constraints, I was not able to find anything seminal. I would like to see who did it first.

Many of the references[10] were at the application note level without a lot of attention paid to the accuracy requirements for the phase shift network. Minimizing spurious output levels was generally not discussed. Could both low conversion loss and good suppression of the spurious outputs be obtained using a really accurate 90-degree phase shifter, and a highly balanced mixer?

There is nothing like a good, however crude, experiment to illuminate an issue. In the junk box I found an ancient Relcom M1B mixer, and a MiniCircuits ZSC-2-1W power splitter. To house the phase shifter I found a small box with two BNC connectors. Using equations from *Electronic Filter Design Handbook*,[11] a second order, –90 degree all pass phase shift network was designed. Refer to the "Designing the Phase Shift Network" sidebar for a discussion of the phase shift network. I used a spreadsheet to partially automate the network design process. The spreadsheet may be used for phase shifters at other frequencies, impedances, and for phase shifts other then 90 degrees. It may be found on the *QEX* website.

With available leaded components, the phase shift network was built into the box with the BNC connectors. Test with a network analyzer showed a phase shift of –89 degrees at 5 MHz.

Next, the doubler parts were connected in true "hanging breadboard" style using three short BNC jumper cables to connect the power splitter, phase shifter box, and the mixer. The phase shift added by the cables is insignificant at 5 MHz. Upon test, the results shown in Table 2 were obtained.

For input powers of +11 dBm or more, the conversion loss was less than 10 dB. The fundamental and odd harmonic suppression was greater than 40 dB, while the fourth harmonic (20 MHz) was attenuated by more than 30 dB. With these levels of spur suppression only a minimal amount of filtering in the output amplifier would be required. Most importantly no high Q filter components would be needed.

Prototype Doubler

With these encouraging results the next step was to prototype the QDMD on a printed circuit board (PCB) using the intended surface mount parts. This would provide the data required for design of the output amplifier and associated filtering. Accuracy of the phase shift network, mixer balance and isolation, along with the phase and amplitude balance of the power divider set the ultimate performance of the circuit. For this design a MiniCircuits[12] JPS-2-1W power splitter was selected. At 5 MHz the typical amplitude balance is better than 0.01 dB and the typical phase unbalance is 0.03 degrees.

For the mixer, the critical parameters are the LO to IF, and the RF to IF isolation because the inputs are to the LO and RF ports, and the output is taken at the IF port. Any leakage will contribute to the spurs seen at the IF port (i.e. the doubler) output.

Another MiniCircuits part, the JMS-1MH mixer was selected for the mixer. From their Web site data, the LO to IF isolation is typically more than 60 dB. The RF to IF isolation is more than 45 dB. This is a Level 13 mixer optimized for LO levels of about 13 +/- 3 dBm. Both parts use the same surface mount package. The connections protrude from the edge of the package making these parts very easy to install with normal soldering tools. The PCB pattern and package dimensions are also found on the MiniCircuits Web site. MiniCircuits will accept small quantity web orders.

Figure 5 is the schematic of the prototype frequency doubler. The 5 MHz signal is input at BNC connector, J-1, and split into two paths by the power splitter, HY1. Output 2 of the splitter is connected directly to the LO port of the mixer, Z1. Output 1 of HY1 is routed to the phase shift network via a 4-post header JP1. The phase shift network delays the signal by 90 degrees and it is then routed to the RF port of mixer, Z1, via the

Table 2

Performance of the "Hanging Breadboard" Quadrature Driven Mixer Doubler (dBm)

5 MHz Input	10 MHz Output	5 MHz Spur	15 MHz Spur	20 MHz Spur	25 MHz Spur
10	0.1	–39	–62	–35	–55
11	1.6	–40	–67	–36	–54
12	2.4	–40	–58	–39	–52
13	4.2	–42	–55	–34	–50
14	5.4	–40.2	–57	–36	–55
15	6.5	–43.6	–50	–31	–57
16	7.5	–54	–50.5	–28	–62

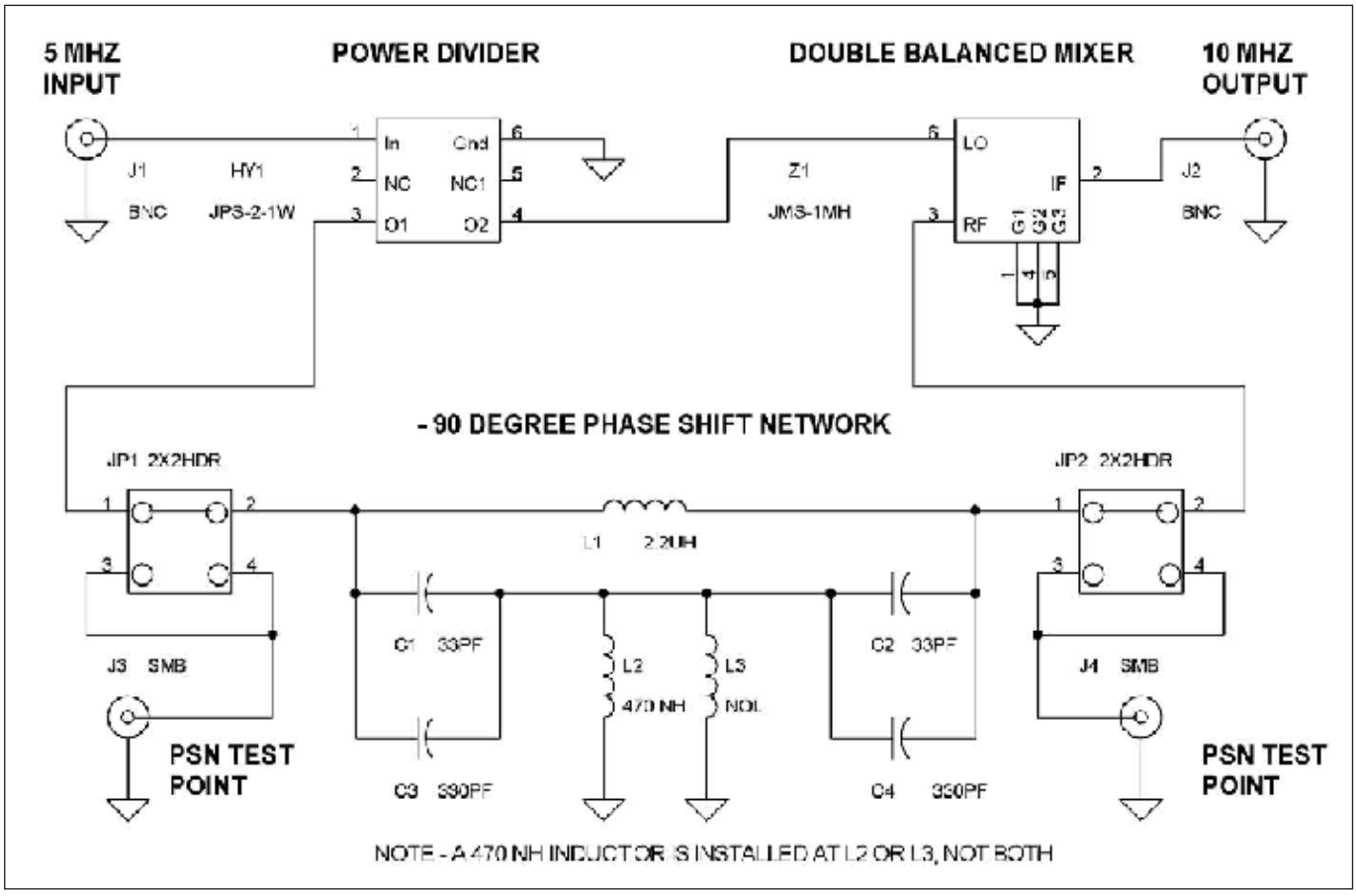

Figure 5 – Prototype frequency doubler schematic diagram. The shunts at JP1 and JP2 may be reconnected from 1-2 to 2-4 enabling the phase shift network to be tested via J3 and J4.

header JP2. In normal operation jumpers (shunts) connect pin 1 to pin 2 of both JP1 and JP-2. The 10 MHz output is obtained at the IF port of the mixer and sent to J2. To accurately measure the performance of the phase shift network, the jumpers at JP1 and JP2 are re-set to connect pins 2 and 4 on each header. The input and output of the phase shift network are then routed to the two phase shift network test points, SMB jacks, J3 and J4. This enables a convenient direct coaxial connection using SMB coax cables from a network analyzer for phase, impedance and insertion loss measurements.

Figure 6 is a photo of the completed QDMD prototype. It was built on 0.062 FR4. All circuitry and components are on the top of the board. The entire bottom of the board is a solid ground plane connected to the components with vias. Due to the low frequency it was not required to control the line widths for matched microstrip connections. All parts were surface mount with the exception of the connectors and headers. I prefer through-hole mounting for parts that will be subject to mechanical stress. On the schematic, two inductors, L2, and L3, are shown connected in parallel. In actuality only one is installed.

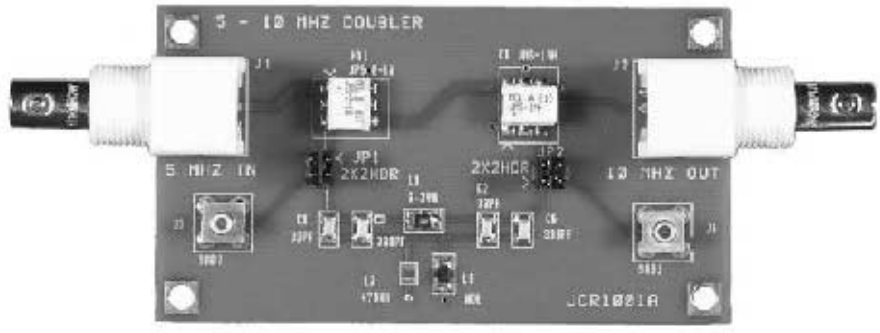

Figure 6 – The test board used to evaluate the prototype frequency doubler. The input is at the left and the output at the right. The phase shift network was arranged along the lower edge. L2 is not populated, the 470 nH inductor is installed at L3.

At the time it was unknown if I would obtain the 470 nH part in a 1008 or 0805 surface mount package, so pads for each were included in the PCB layout. As it turned out a 470 nH inductor in a 1008 package was installed at L3 and L2 was unpopulated.

Prototype Doubler Test Results

Test goals were to quantify the performance of the phase shift network and to establish the overall performance of the QDMD with regard to conversion loss and spur rejection using the selected surface mount components. Quantification of the output spur levels was a necessary input to the design of an output amplifier having minimal filtering.

First the performance of the phase shift network was measured. JP1 and JP2 were connected to access the phase shift network via J3 and J4. The input impedance, insertion loss, and insertion phase of the phase shift

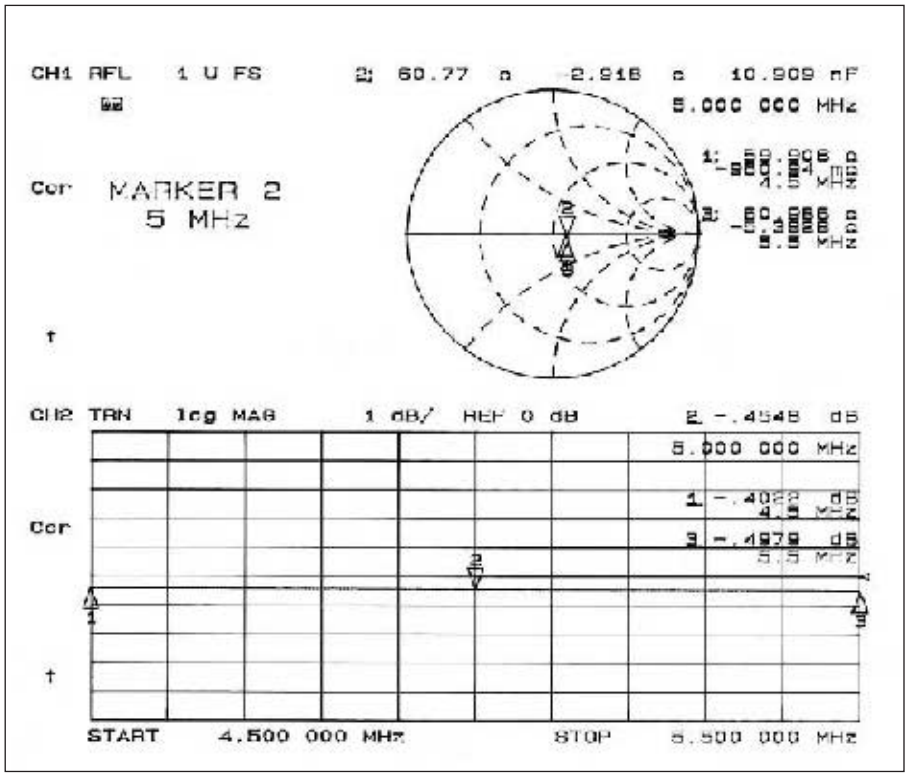

Figure 7 – Prototype phase shift network input impedance and insertion loss with the standard component values shown in Figure 5. The Smith Chart shows a constant input impedance of 60 Ω from 4.5 to 5.5 MHz. The insertion loss is 0.454 dB at 5 MHz.

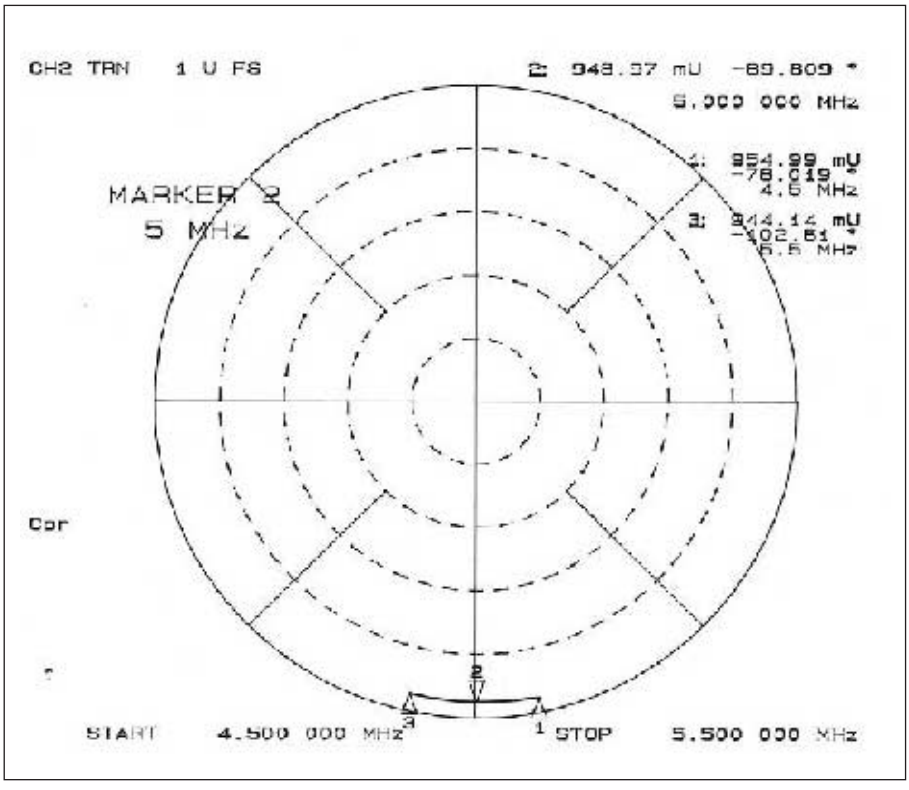

Figure 8 – This is a network analyzer polar plot of phase shift for the prototype phase shift network from 4.5 to 5.5 MHz. At 5.0 MHz the phase shift is –89.8 degrees. The design goal was –90 degrees. From 4.5 to 5.5 MHz the total phase change is 24 degrees.

network were measured from 4.5 to 5.5 MHz using a network analyzer. Figure 7 is a set of two plots showing the input impedance and insertion loss of the phase shift network. At 5 MHz the input impedance is 60 –j2.9 Ω and it does not change significantly with frequency. Using standard value inductors raised the impedance from the ideal 50 Ω design. The insertion loss is 0.45 dB. Figure 8 is a polar plot showing the phase shift from 4.5 to 5.5 MHz. At 5 MHz the phase shifter measured –89.8 degrees. This was about as close to –90 degrees as one could hope for.

JP1 and JP2 were re-configured to connect the phase shift network to the power splitter and mixer. The doubler was then tested using a calibrated signal generator and spectrum analyzer. Power input to the doubler at 5 MHz was stepped from +6 to +16 dBm in 1 dB steps. The 10 MHz output and other harmonic outputs were recorded. Figure 9 is a spectrum analyzer screen shot showing the output spectrum with a 5 MHz input of +13 dBm. The 10 MHz output was +3.5 dBm indicating a conversion loss of 9.5 dB. The 5 MHz fundamental and all odd harmonics were below the –52.5 dBm reference display line (DL on the analyzer screen). The principal even harmonics were the fourth (20 MHz) at about –23 dBm and the sixth (30 MHz) at about –20 dBm.

Data obtained from the spectrum analyzer was tabulated and plotted. Figure 10 shows how the doubler performance changed as a function of the 5 MHz input power level. The circuit was well behaved with no large changes in performance for a wide range of input power levels. For inputs of roughly 9 dBm and above the conversion loss was 10 dB or less. The 5 MHz fundamental and odd harmonics were 50 dB or more below the10 MHz output, so the doubler could easily meet my –40 dBc spur specification at these frequencies with no additional filtering. The fourth harmonic would be the most difficult to filter as it was the largest spur and is close to the desired output frequency. However with a + 13 dBm input, the fourth harmonic was still more than –26 dBc. It and the other high order even harmonics (40 and 60 MHz) could be suppressed below –40 dBc with only simple filtering.

Is the 90 Degree Phase Shifter Required

One often quoted source, the Phillips application note AN1893,[10] and others indicate the primary purpose of the phase shift network is to remove the dc level on the output. While this is true, it is not the whole story or even the most important part. The accuracy of the phase shift network affects not just the dc level. More importantly it also affects the level of undesired harmonics and

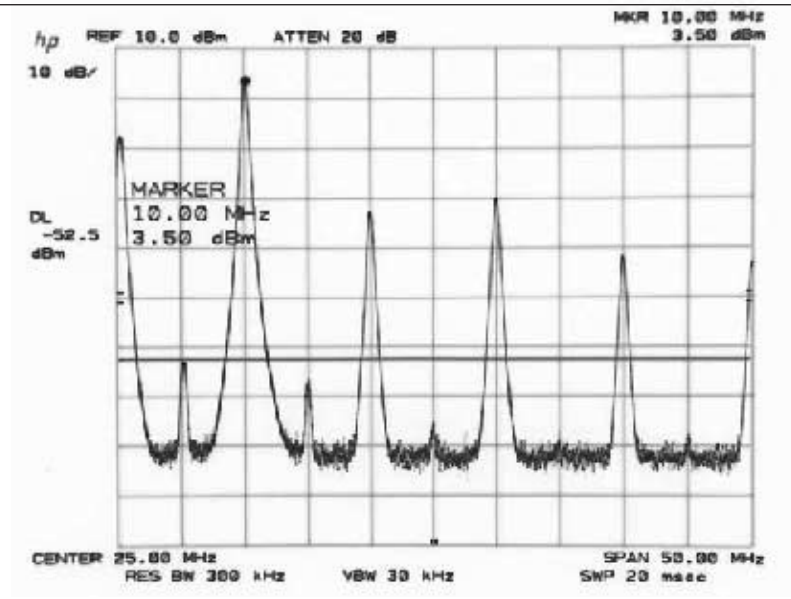

Figure 9 – Output spectrum of the prototype QDMD with a +13 dBm input at 5 MHz. The output is +3.5 dBm at 10 MHz. The horizontal display line is positioned at –52.5 dBm and just above the 5 MHz input spur indicating the 5 MHz spur is 56 dB below the 10 MHz output. The other odd harmonics are suppressed even more. The fourth harmonic (20 MHz) is 25 dB below the 10 MHz output.

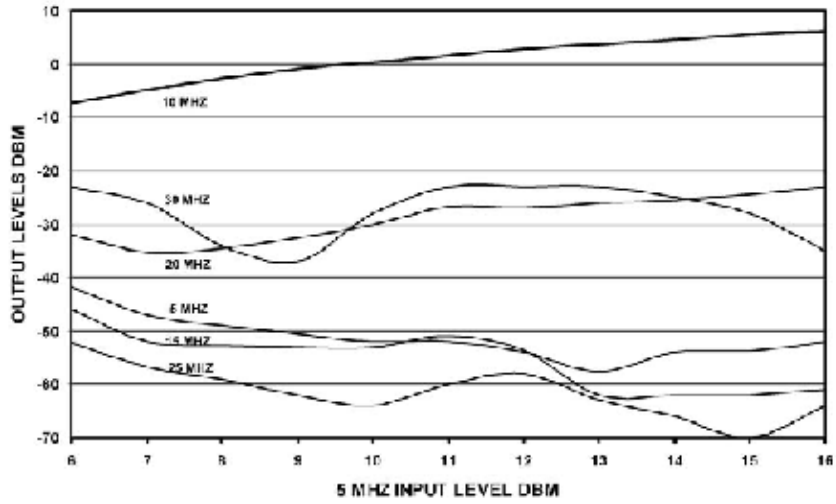

Figure 10 – This graph shows the 10 MHz output level for inputs from +6 to +16 dBm. Also shown are the levels of the undesired harmonics. The circuit is well behaved over a wide range of input power levels with good suppression of the undesired outputs.

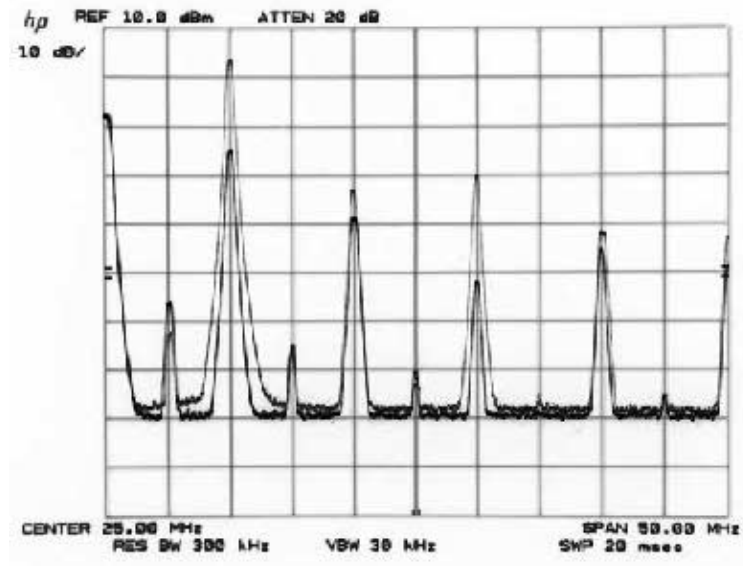

Figure 11 – In this photo two overlaid spectrum analyzer plots illustrate the effect of operating the doubler with and without the phase shift network. The input power was +13 dBm. In the upper trace the 10 MHz output level is +3.5 dBm. With the phase shift network bypassed the lower trace shows the 10 MHz output level drops to –15 dBm and the 20 MHz harmonic level is increased relative to 10 MHz.

the second harmonic conversion loss. To illustrate this I did two simple tests. I used the spectrum analyzer to capture and display on a single screen the doubler output with the 90 degree phase shifter connected as usual, and also with it bypassed. Figure 11 is the result. The input was +13 dBm and the only change was to remove the shunts and bypass the phase shift network with a jumper wire from JP1 pin 1 to JP2 pin 2. The figure shows the 10 MHz output dropping from + 3 to –15 dBm. Also, suppression of the fourth harmonic degraded to only –14 dBc.

Another test illustrated the effect of phase shifts other than 90 degrees. Since the phase shift network is frequency sensitive and the other parts are broadband, shifting the input frequency above and below 5 MHz was an easy way to change the phase shift. What I found was that the for inputs of 4.5 and 5.5 MHz, corresponding to phase shifts of 78 and 102 degrees (i.e. 90 +/- 12), the doubler performance stayed about the same. However, the dc level did come up and the second harmonic suppression was degraded. For input frequencies of 4 and 6 MHz (67 and 115 degree phase shift) the conversion loss increased by about 3 dB and the spurs came up even more. Conclusion – the phase shift network is required and for best performance, the phase shift should be as close to 90 degrees as practical.

Doubler – Amplifier System Design

With the performance of the QDMD quantified, the next step was to develop a block diagram and power budget for the complete multiplier-amplifier assembly. While this is not a complex system, a simple power budget quickly nails down the exact input and output levels for all of the components and was essential to determining the gain and output power requirements for the amplifier.

Figure 12 is the system block diagram used to develop the power budget. From the test data, it was decided to operate the doubler section with a + 13 dBm input. At this input level, optimal rejection of the nearby 5 and 15 MHz spurs was obtained on the prototype. Also, I wanted to use attenuators at the input, output, and between stages. This is one of my favorite design practices because pads in these places would reduce the input power to the desired +13 dBm at the doubler and reduce VSWR interactions throughout. The pad at the output would also help stabilize the amplifier if operated into unmatched loads. Initially 3-dB attenuation was specified for the interstage and output pads as well. This would leave some room for gain adjustment if required on the actual hardware.

A spreadsheet, Table 3, summed all the gains and losses for the elements shown in Figure 11. A power output of +13 dBm was required from the output pad, AT 3. Using the spreadsheet to do the math, the gain of amplifier, A1, was adjusted to obtain the required output.

An amplifier gain of 15.5 dB was required. To overcome the planned 3 dB loss in the output attenuator, the amplifier would have to deliver 16 dBm at its output port (16 dBm is 40 mW).

Table 3
Frequency Doubler Power Budget

Parameter	Gain, Loss, or Level
Input Power from 5 MHz Frequency Standard	16.0 dBm
Insertion Loss of Input Attenuator (AT1)	3.0 dB
Output Power from AT1, Input Power to X2	13.0 dBm
Conversion Loss of X2	9.5 dB
Output power from X2	3.5 dBm
Insertion Loss of Interstage Attenuator (AT2)	3.0 dB
Output of AT2	0.5 dBm
Gain of Amplifier (A1)	15.5 dB
Output Power of A1	16.0 dBm
Insertion Loss of Output Attenuator	3.0 dB
10 MHz Power Output	13.0 dBm
Required 10 MHz Power Output	13.0 dBm

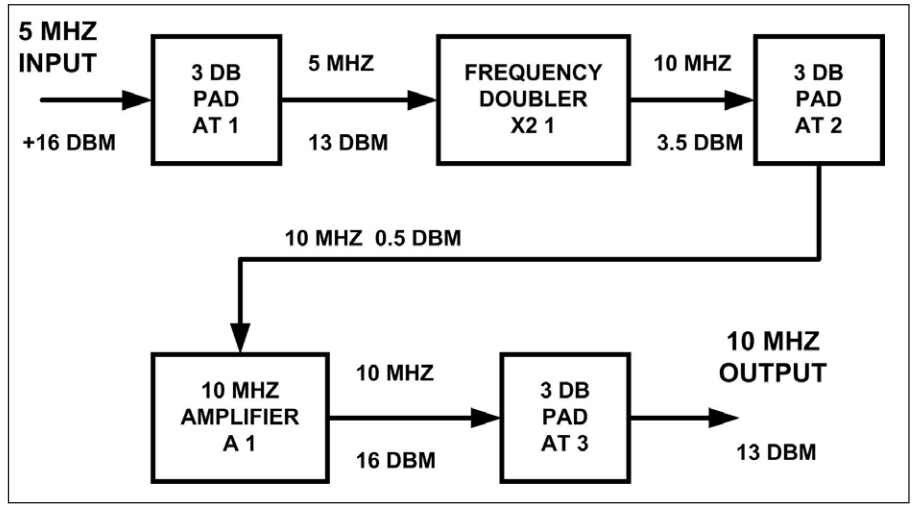

Figure 12 – Block diagram of the complete 5 to 10 MHz Frequency Doubler. 3 dB attenuators are used between stages to reduce mismatch interactions, set power levels, and to provide a defined load if the output is operated into a mismatch.

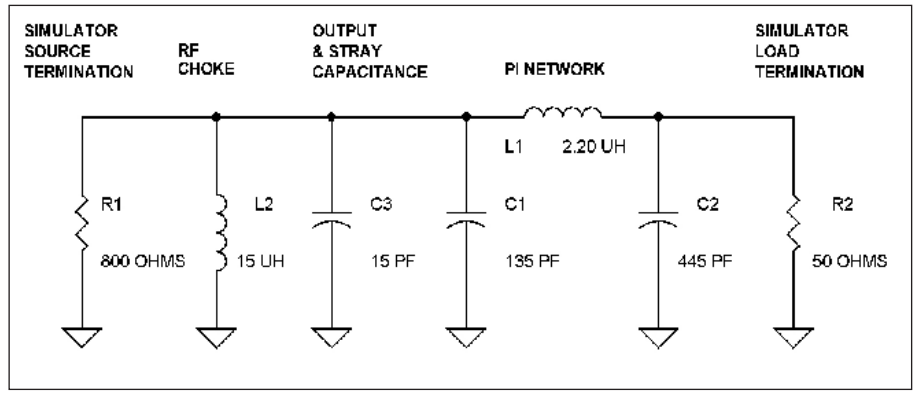

Figure 13 – Circuit used to model the amplifier stage output network. In addition to the impedance transformation network (L1, C1, and C2), the model includes L2, used to supply dc to the collector, and C3 that simulates the transistor output capacitance and stray capacitance.

Amplifier Tradeoffs

My first thought was to use one of the ubiquitous Monolithic Microwave Integrated Circuit (MIMIC) amplifiers that have so eased the lives of RF designers. These devices are small, not expensive, provide sufficient gain and are easily applied. The inputs and outputs are matched to 50 Ω. However, because the matching is done with feedback and not an actual impedance transformation, the current drawn at output levels above a few milliwatts is prohibitive. I tested one MMIC that easily provided the output power, and with low distortion, but it required 130 mA to operate. This far exceeded my 25 mA requirement. High speed, high power video op-amps and line drivers were also considered. But again, the current draw was an issue. The amplifier is required to deliver +16 dBm, or 40 mW to a 50 Ω load. The RMS current required at the 50 Ω load is found from

$P=I_{rms}^{2} \times R$, and solving for I,

$$I_{rms} = \sqrt{\frac{P}{R}} = \sqrt{\frac{0.04}{50}} = 0.028 \text{ A or } 28 \text{ mA.}$$

The peak current, $I_{peak} = I_{rms} \times 1.414 = 39.5$ mA.

This is the current delivered to the load and does not include allowance for device bias current, design margin, or inefficiency. Without impedance transformation, a practical amplifier would require much more than 25 mA.

Considering the above, it was decided to use a single stage bipolar design. Since the available +15 V supply far exceeded the required peak output voltage, an output impedance transformation would trade peak to peak collector voltage for supply current. The impedance matching network could also be tailored to provide filtering of the 20 and 40 MHz spurs from the doubler stage without additional components. A few sums on the back of the proverbial envelope proved this to be the best approach.

Output Amp Design Assumptions

To get the design started, a number of assumptions were made, here are a few of them:

a. The amplifier would be a common emitter design using a transistor from the 2N2222A family. These are readily available in surface mount packages. The 2N2222A has a Beta > 70 which is flat over the range of operating currents anticipated. It also has a low output capacitance, and is useful through VHF.

b. Emitter degeneration and shunt collector to base feedback would be used to set the stage gain, and to set the input impedance. Feedback would also stabilize the stage for unusual loads.

c. A low Q, C input/output Pi section would be used for the output impedance transformation network. Because it has an inherent low-pass filter response above resonance, the circuit could also filter off the undesired spurious outputs with no added parts.

d. For good dc stability, the transistor emitter voltage would be set at 3.3 V by biasing the base at 4 V with a stiff voltage divider. Any change in V_{BE} with temperature is thereby a small fraction of the drop across the emitter bias resistor so the emitter current remains stable.

e. Biasing the base at 4 V limited the available downward collector swing to 11 (i.e. 15 – 4 V) before the stage would clip. Thus the maximum peak to peak voltage available in the collector circuit could only be 2 × 11 V or 22 Vpp.

f. For low distortion the transistor idling current would be set at least 2 times the peak collector current so the transistor would not approach cutoff – true Class A operation.

g. Also for low distortion, *the transistor should not be allowed to approach the clipping point at full power output.* To ensure this could not happen, the load resistance presented to the transistor would purposely be made *lower* than the optimal impedance for best efficiency. This would limit the peak to peak voltage and prevent clipping.

Output Load Impedance and dc Operating Point

The load resistance and available peak voltage at the transistor determine the peak current in the output tank circuit, and ultimately the power drawn by the circuit. Operating in Class A requires the transistor idling current to be more than the peak current.

For this design the logical process was as follows:

a. I determined a trial working load impedance that prevented clipping on the negative swing of the collector voltage.

b. Using this impedance I determined the peak RF current in the output load. For Class A operation the transistor idle current was set to substantially more than the peak RF current. This assured the transistor would never cut off on the positive swing of the RF cycle. The current required to operate the stage was determined and found to be acceptably close to my 25 mA requirement. If the current had turned out to be too high, the available voltage swing, or biasing conditions would have had to be adjusted.

c. The output Pi network was then designed to transform the 50 Ω load up to the load impedance determined in step (a) above.

For frequencies where the output capacitance and inductance of the transistor may be largely ignored, the "optimal" load resistance is determined by the required power output and the available peak to peak voltage swing in the collector circuit. With this load the voltage swing is maximized and the peak current in the device is minimized, resulting in the required power being obtained with minimum current. This load resistance is[13]

$$R_L = \frac{[Vcc - Vce_{sat}]^2}{2Po}$$

where;

Po is the required power output in watts

Vcc is the collector supply voltage.

Vce_{sat} is normally the device saturation voltage, where the collector voltage swings below the base voltage.

If the device is not driven to saturation, as in this case, Vce_{min} can be defined as *the lowest voltage from collector to emitter* during the RF cycle. From this we can define the peak voltage swing above and below Vcc as:

$$Vp = Vcc - Vce_{min}$$

Then the equation for the load resistance simplifies to:

$$R_L = \frac{[Vp]^2}{2Po}$$

Remembering that for this design, the base voltage is arbitrarily set at 4 V and Vcc is 15 V. The maximum possible Vp is the difference; 15 V – 4 V = 11 V. Entering Vp = 11, and Po = 0.040 Watts, the resulting load impedance is;

$$R_L = \frac{[11]^2}{2 \text{ x } (0.04)} = 1512 \ \Omega$$

A 1512 Ω load would provide the greatest efficiency within the constraint that the base voltage (Vb) is set to 4 V. With a 1512 Ω load, the amplifier would just clip on the downward swing of the collector voltage.

To avoid clipping, Vp may be reduced to any degree desired by using a lower load resistance. The only tradeoff is increased current drain. I decided to keep Vce at 3 V or more. The transistor would always operate well above the clipping point. With this new limitation, the maximum permitted peak voltage Vp = 15 V – (4 V + 3 V) = 8 V. The load resistance to be presented to the transistor by the output impedance transformation network then became:

$$R_L = \frac{[8]^2}{2 \text{ x } (0.04)} = 800 \ \Omega$$

To maintain Class A operation, a dc quiescent current must be set for the transistor. For low distortion the transistor must not be allowed to cutoff or clip, and the best linearity will be obtained if the change in collector current during the RF cycle is minimized. However, a high idling current must be traded off against the available supply current and power dissipated by the device.

I proceeded as follows. First the peak current in the load was found from the peak voltage and load resistance. From Ohms law this is simply:

$$I_{peak} = \frac{Vp}{R_L} = \frac{8}{800} = 0.01 \text{ A, or } 10 \text{ mA.}$$

Originally I planned an idle current of 2 times the peak current or 20 mA. With an idle current of 20 mA, the transistor current would swing from 30 mA (20 mA + 10 mA) at the low voltage point in the collector waveform, and to 10 mA (20 mA – 10 mA) at the high voltage point in the collector waveform. The transistor would never saturate or reach cutoff, assuring Class A operation. With equal positive and negative current swings in the collector current, the collector supply current would simply be the idling current of 20 mA. The base bias network would require another 4 or 5 mA, putting the total current right at the 25 mA design goal. As it turned out, the exact resistors required for the base bias divider and emitter resistor were out of stock. The values ultimately selected were a compromise. The final idling current is 22 mA and the overall current required is 27 mA.

Having confirmed that a Vp of 8 V and a load resistance of 800 Ω would provide the required 40 mW with an acceptable supply current, the last step was to design the output impedance transformation network. For this design, the capacitor input Pi-network offered several advantages:

a. Low-pass response would filter the remaining 20 and 30 MHz harmonics at the doubler output.
b. The input capacitor could be adjusted slightly to absorb the output capacitance of the transistor, and also to tune out the effect of the RF choke used to feed dc to the collector circuit.
c. Importantly, the Q of the network could be fiddled with to adjust the value of the series inductor to be a standard part value.

Equations for matching network designs including the Pi section may be found in a number of references.[13, 14] For my design I used a BASIC program I wrote long ago. It made it easy to iterate the Q to obtain a standard value inductor. For others, I refer you to page 14.60 of the 2008 edition of *The ARRL Handbook*.[14] The *Handbook* included a CD with a program MATCH.EXE that designs 14 matching networks, including the Pi section used here. My program and MATCH.EXE produced essentially identical results; summarized in Table 4.

Computer Simulation

With the Table 4 values determined, the next step was to model the collector circuit; to include not only the impedance transformation network, but also the output capacitance of the transistor, stray capacitance, and the dc supply RF choke. Figure 13 is a schematic of the model that was implemented using the now-discontinued *ARRL Radio Designer* program.

In the model, C1, C2, and L1 comprise the Pi-network with the calculated part values. L2 was set to a standard 2.2 µH inductor by adjusting the Q to 6.8. R1 is the 800 Ω source termination set up in the software. R2 is the 50 Ω termination the network is to transform up to 800 Ω. L2 is the dc feed choke, and C3 is a dummy capacitor consisting of the sum of the transistor output capacitance (8 pF), the capacitance required to tune out L2, plus any stray C added by the board.

Table 4
Theoretical Pi-Network Design

Input Resistance	800 Ω
Output Resistance	50 Ω
Operating Frequency	10.0 MHz
Specified Q	6.8
Input Side Capacitor	135 pF
Series Indictor	2.2 µH
Output Side Capacitor	445 pF

Figure 14 is the simulation result; the 50 to 800 Ω impedance transformation is quite good with a return loss (MS11, or MS22) of 30 dB or so. The insertion loss (MS21) is 0 dB at 10 MHz. As desired, the overall response is low-pass. At 20 MHz the attenuation is 27 dB, and at 30 MHz, the attenuation increases to 39 dB. This attenuation would be more than sufficient to reduce the undesired even harmonic outputs of the doubler to below –40 dBc.

Putting It All Together

Figure 15 is the schematic for the final doubler design and Figure 16 a photo of the board fabricated on 0.062 FR-4. It was possible to lay out the PCB without any crossovers or any circuitry on the backside, which is all RF goundplane. All ground connections were direct to the ground plane using plated through vias.

The 5 MHz input from the frequency standard is input at the BNC connector J1 and routed to the 3 dB pad (R5, R9, R10) where the level is reduced to +13 dBm. From the pad the signal is applied to the QDMD at the power splitter, HY1. Circuitry and opera-

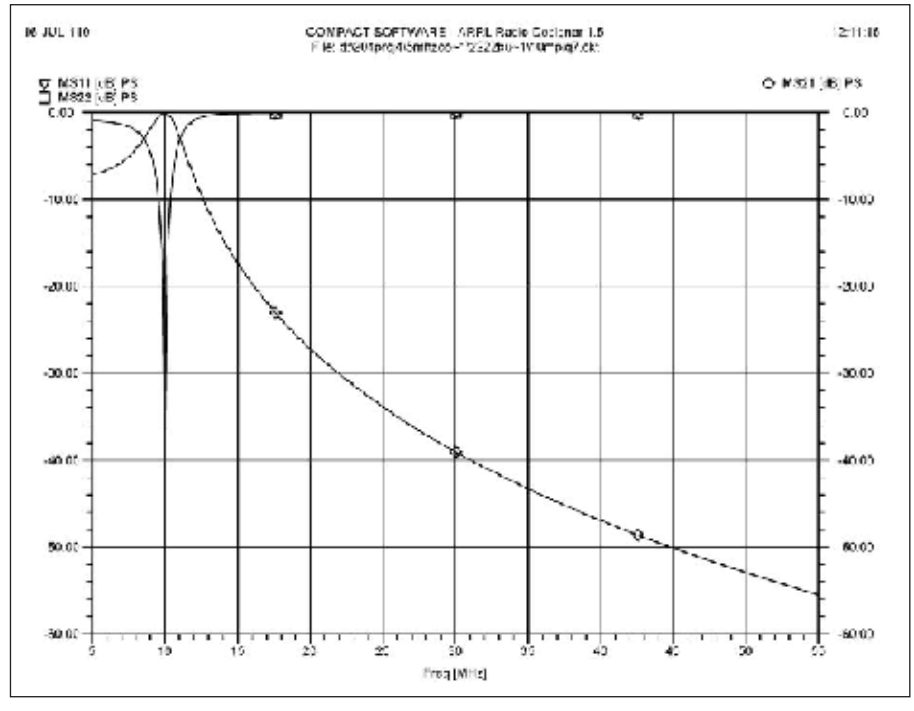

Figure 14 – Simulated response of the amplifier output network with the element values shown in Figure 13. This network has a Q = 6.8 so the 5 and 15 MHz spurious signals are not significantly attenuated. High odd harmonic attenuation by the ×2 multiplier will suppress these frequencies.

tion of the ×2 multiplier section is identical to the prototype QDMD board described above. Test points J3, and J4, and the associated headers JP2 and JP3 were retained to troubleshoot the phase shift network if required. Output from the QDMD at the IF port of mixer, Z1, is +3.5 dBm at 10 MHz. From Z1 the signal passes through a second 3 dB pad (R11, R8, R12) to header JP1. A shunt at JP1 normally connects pins 1 and 2, routing the signal to C4 and the amplifier input. For testing, the shunt at JP1 can be connected from pin 1 to pin 3, making the output from the pad available at test point J5. Alternatively the shunt may be connected from pin 2 to pin 4, making the amplifier input accessible from J5. This connection was used to obtain the amplifier performance data presented below.

From C4 the signal is applied to the base of the amplifier stage, Q1. For Q1 a surface mount transistor equivalent to the 2N2222A was selected. High current gain (Beta) of 70, and a 300 MHz gain-bandwidth product make the 2N2222 family a favorite of designers. They are available in two surface mount packages, the SOT23, and the SOT223. The SOT23 packaged devices such as the MMBT22222LT1G can dissipate 223 mW. In my amplifier the power dissipated is the Vce multiplied by the collector current (11 V × 0.022 A) or 242 mW. This exceeds the capability of the SOT23. The PZT2222AT1 is the same device, but in the larger SOT223 package, it can dissipate up to 1.5 W. It was selected for Q1.

The dc operating point of Q1 is set by the base divider, R2 and R13, and the emitter resistor, R14. A simplified bias design was used. For Q1 the minimum current gain of 70 is specified at 10 mA and increases to 100 at 150 mA. I always use a lower "forced" Beta to account for temperature effects and the odd device that does not meet the minimum specification. For this design a worst case Beta of 50 was used. The worst case maximum base current to drive the transistor to 20 mA (design goal) collector current was Icol/Beta = .020/50 = 0.4 mA. To make the base divider "stiff" and hold the base voltage at 4 V, the current in the divider was set at about 10 times the base current or 4 mA. Next the base divider resistors were calculated. The initial values for R2 and R13 were 2.5 K and 1.0 K respectively. With only the RF choke L1 between Vcc and the collector, at dc the circuit is essentially an emitter follower. The emitter voltage, Ve = Vbase – 0.7 V or about 3.3 V. Provided the available base drive is sufficient (which it is), the emitter (and collector) current is approximately Ve/R14, and R14 = Ve/Ie. So R14 = Ve/Ie = 3.3 V/.020 A = 165 Ω. This method is approximate in that the base current is ignored. However, even with a forced Beta

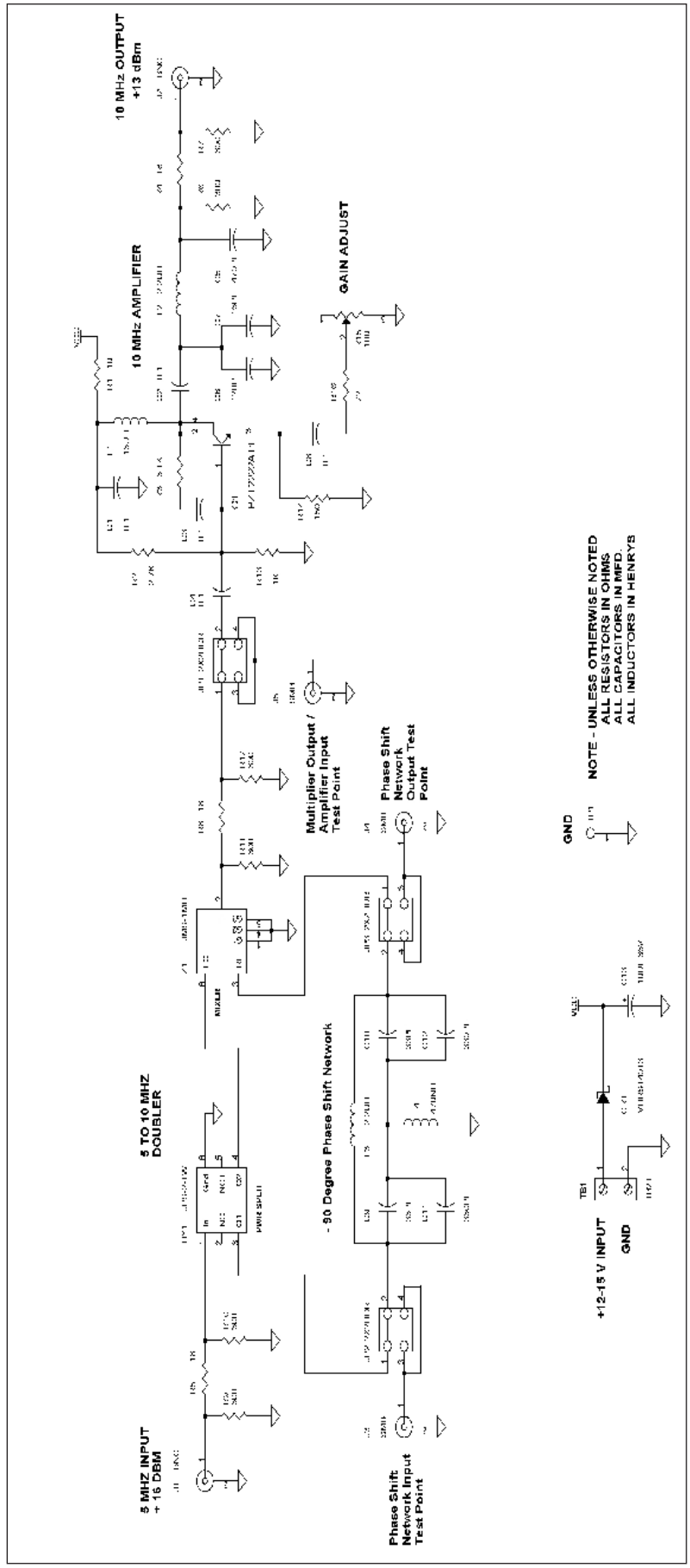

Figure 15 – Schematic of the complete 5 to 10 MHz Doubler

of 50, the error is only about 2%. Since this is less than the 5 % tolerance of the resistors used, the method serves well for practical work. Due to part availability, the exact resistors could not be obtained and the values shown on the schematic were substituted. R2 is 2.7 K and R14 is 150 Ω. As a result the transistor collector current turned out to be 22 mA.

A single bipolar transistor of the 2N2222 type can provide much more gain than needed for this design. Two kinds of feedback were used to reduce the gain. AC Resistance in series with the emitter raises the input impedance and also sets the voltage gain of the stage. The series connection of C8, R16, and R15 connected in parallel with the emitter bias resistor, R14, determined the ac resistance from the emitter to ground. Adjustment of R15 provided a gain variation of more than 6 dB. R3 and C3 provide shunt feedback from the collector to the base of Q1. Shunt feedback lowered the input impedance into the desired range, less than 100 Ω, and further reduced the gain.

With the shunt feedback, the input impedance can be lowered to any extent at some loss in gain. However, adjustment of the amplifier gain with the emitter resistance does change the input impedance. This is where a pad can help. Use of the 3dB pad at the output of Z1 stabilizes the load seen by Z1 and the source impedance seen by the amplifier.

L2, C6, C7 and C5 comprise the output impedance transformation network. It is essentially the same Pi-network modeled above. However, to maintain the resonance at 10 MHz with a standard value 470 pF capacitor at C5, and including the output capacitance of Q1, the total value of C6 + C7, had to be reduced to 135 pF. C6 was fixed at 120 pF. Then, in test, C7 was adjusted in 5 pF steps to tune the network to exactly 10 MHz. This method eliminated the need for a trimmer capacitor.

A 3 dB pad (R6, R4, and R7) from C5 to the output connector, J2, completes the amplifier circuit. The pad in this position provides a defined load and prevents instability if the amplifier is operated into an open circuit or high impedance.

Power is applied at terminal block, TB1. TB1 is a plug-in terminal block that plugs onto header pins soldered to the board. To remove the board it can be simply unplugged with the wiring left connected. The circuit is protected from reverse polarity by CR1, a Schottky diode.

Performance

Prior to installation, the Doubler – Amplifier board was evaluated to compare the required, predicted and actual performance. Performance of the QDMD multiplier

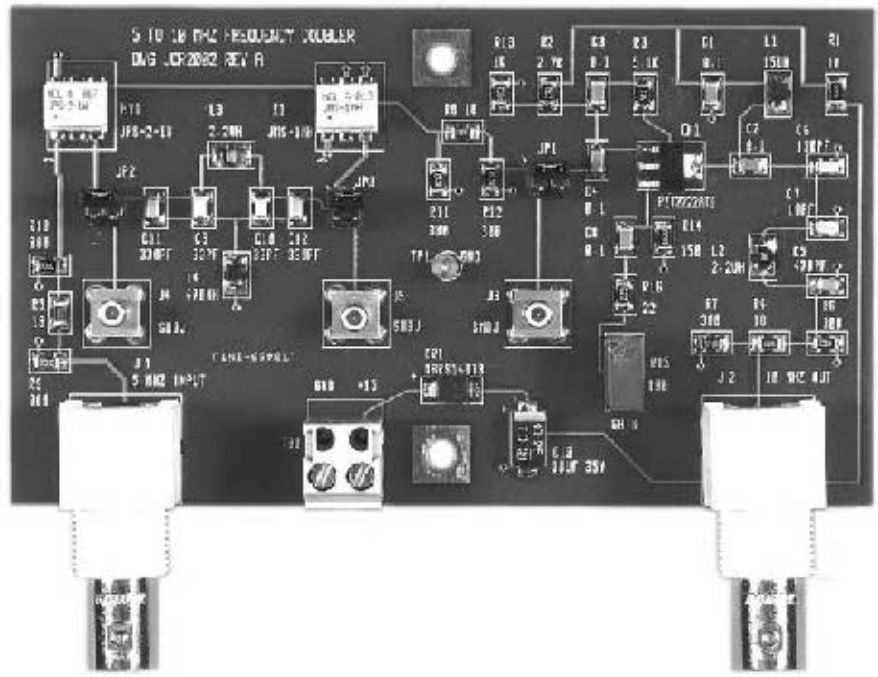

Figure 16 – The assembled 5 to 10 MHZ Frequency Doubler. Except for the connectors, the pot, and the terminal block all surface mount parts are employed. The phase shift network is located between the power splitter, HY1 and the mixer, Z1. The inductors in the phase shift network are positioned to avoid magnetic coupling. The base bias and shunt feedback networks are at upper right and the output circuit is positioned along the right edge of the board. One of the collector terminals of Q1 is a large heat sink tab that is soldered to a pad on the board near C2.

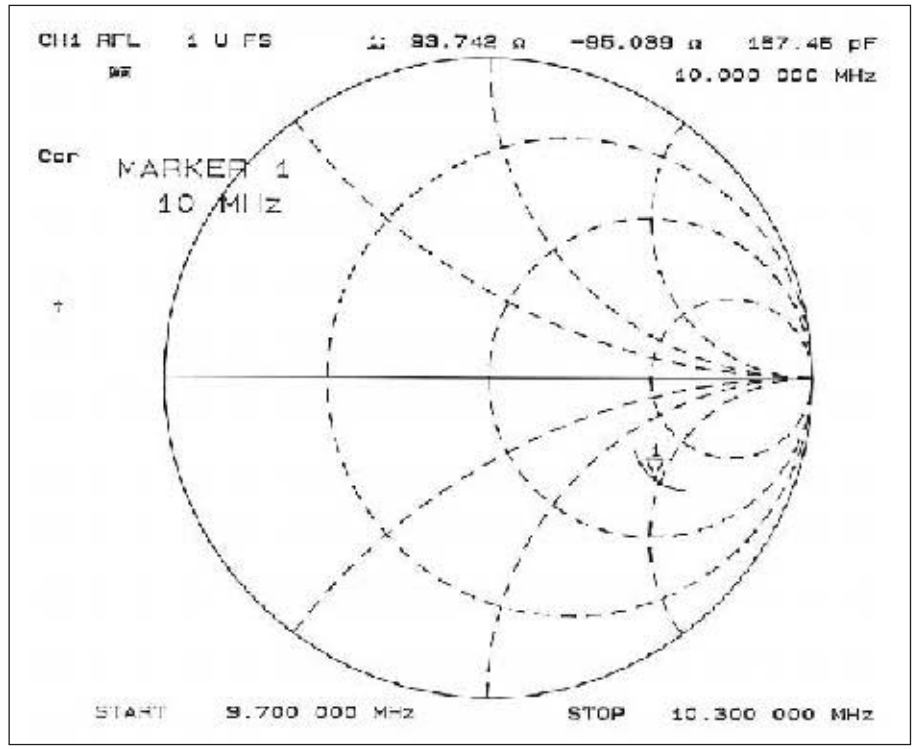

Figure 17 – Smith Chart plot of the amplifier input impedance from 9.7 to 10.3 MHz with the gain control, R15, set for maximum gain. At 10 MHz the input impedance is 93 – j95 Ohms. Decreasing the gain, i.e. increasing R15, moves the impedance higher. The 3 dB pad between the amplifier input and the ×2 multiplier reduces the impedance change seen at the QDMD output.

section was identical to the prototype, so it is not repeated here. Testing was directed at the amplifier section, and the overall performance of the PCB. After installation, the performance in the frequency standard was tested.

Using a HP8752C network analyzer, the input impedance and gain of the amplifier were measured. JP1 was connected to access the amplifier input directly via the SMB connector J5. Figure 17 is a Smith chart plot showing the input impedance of the amplifier from 9.7 to 10.3 MHz. At 10 MHz, with R15 set for maximum gain, the input impedance is 93 – j95 Ω. Decreasing the gain, with R15, increased the impedance as expected. Reducing the value of R3 would have brought the impedance closer to 50 Ω. However with the 3 dB pad at the input to stabilize the impedance seen by the QDMD section, the results obtained were deemed good enough.

The insertion gain of the amplifier was swept from 5 to 55 MHz with the results plotted in Figure 18. The measured amplifier gain at the maximum setting of R15 was 16.18 dB and included the loss in the 3 dB pad at the output. Correcting for the 3 dB pad at the output, the actual amplifier gain is 19.18 dB or about 4 dB more than required of the amplifier in the power budget, Table 3. The expected low pass response was obtained. Table 5 compares the measured amplifier frequency response data with the expected response from the output network simulation, Figure 14. Expected and actual performance agreed closely, with the disagreement increasing to only 3.39 dB at 40 MHz.

Table 5 illustrates the importance of the excellent fundamental (5 MHz), 3rd (15 MHz) and higher harmonic suppression by the QDMD in meeting the 40 dB overall harmonic attenuation specification. The attenuation by the amplifier output network is only 8 dB at 5 MHz, and 18.99 dB at 15 MHz.

Also of interest is the harmonic distortion of the 10 MHz amplifier stage. This was measured with a HP 8568B spectrum analyzer and Figure 19 shows the results. For this test the amplifier was operated at full gain and the power output set at +13 dBm. The power reading on the analyzer was verified with a HP-432 power meter. Using the analyzer marker function the second harmonic level was measured at –56.8 dBc. The higher harmonics were in the noise. This test confirmed that using a Class A amplifier, with feedback, and a low-pass output network would prevent the amplifier from contributing significantly to the overall spurious output level.

The final RF test at the board level was to measure the ac peak to peak voltage at the collector of Q1. This would confirm correct operation of the output impedance transformation network. If the load at the collector was 800 Ω, the expected voltage would be 16 Vpp at rated power output. The test was made with the amplifier delivering 40 mW (+16 dBm) to the 3 dB pad and + 13 dBm at the output connector J2. Using a Tektronix 475 scope with a low capacitance probe, the collector waveform shown in Figure 20 was obtained. The vertical sensitivity is 5 V per division and the voltage is 16 Vpp indicating the load is close to the 800 Ω design value. The dc current draw was measured at Vcc of 15.0 V. The total for the collector current and base bias network added up to 27 mA. Increasing R14 to 165 Ω, would have reduced the current to the specified 25 mA, but close enough is good enough, so I left it alone. Open circuit stability was verified by operating the amplifier into the high impedance scope input and also by placing a 1000 Ω resistor in series with the input to the spectrum analyzer. No instability occurred and the collector waveform did not clip.

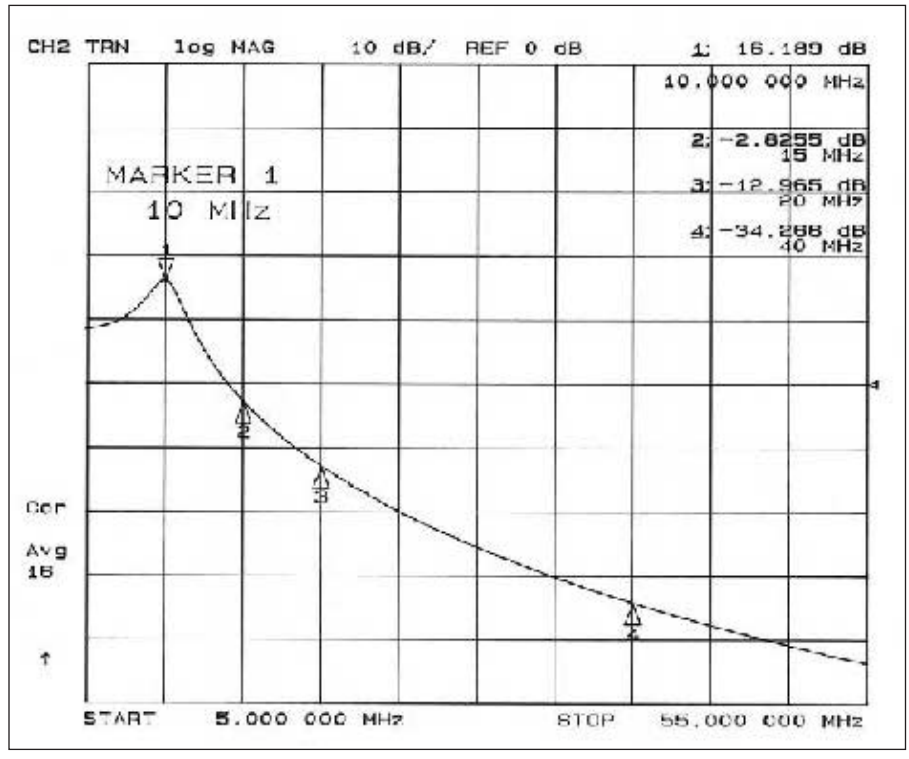

Figure 18 – Network analyzer plot showing the amplifier stage response from 5 to 55 MHz. The gain reference is 0 dB and the amplifier gain at 10 MHz is 16.189 dB. The input to the amplifier is via the SMB test connector J5 and the output is from the BNC connector J2. The measured gain includes the loss of the 3 dB pad at the output, making the un-attenuated Q1 gain 19 dB.

Table 5
Simulated and Measured Amplifier Harmonics

Frequency (MHz)	Amplifier Gain (dB)	Attenuation Relative To 10 MHz (dB)	Simulation Attenuation (db)	Difference (db)
5	8.00	8.19	7	1.19
10	16.19	0.00	0	0.00
15	-2.80	18.99	18	0.99
20	-12.96	29.15	27	2.15
25	-20.00	36.19	34	2.19
30	-25.00	41.19	39	2.19
35	-30.00	46.19	44	2.19
40	-34.20	50.39	37	3.39

Packaging, Installation, and Final Test

A primary concern in designing the doubler installation was that I had no idea of the shock or vibration tolerance of the Vectron FS321A-1. Since I did not want to break anything, a major consideration was to minimize the amount of mechanical trauma inflicted by center punching or drilling. The scheme I came up with, Figure 3, required no new holes in the FS321A-1, and only two solder connections for +15 and ground. The printed wiring board was made the same dimensions, 2.6 by 4.5 inches, as the cover for the crystal filter assembly. By providing mounting holes in the board that lined up with the cover mounting holes, the board could be stacked on top of the cover using spacers and longer screws. To keep things nice and level, two fat .36 inch diameter spacers were turned from 3/8 inch aluminum bar stock.

Installation took only a few minutes. First the PCB was mounted using long screws and the spacers. Next, +15 and ground were wired to TB1 on the board. J3, located near the feed through capacitor on the filter assembly was the (former) 5 MHz output. The cable from J3 to the outside world was disconnected from J3. It was reconnected to the doubler 10 MHz output at J2, just above. Next, a short BNC jumper cable was connected from J3 on the filter assembly to J1, the 5 MHz input, of the doubler PCB. Finally, power was applied and the gain control, R15, was adjusted to obtain 10 MHz at +13 dBm at the former 5 MHz output connectors.

Final testing was performed with the spectrum analyzer. Figure 21, shows the 10 MHz output with the frequency doubler installed in the Vectron 321A-1. Power output at 10 MHz is 13.2 dBm. The reference display line on the analyzer is set just at the top of the highest level spurious outputs at –40 dBm. This indicates the worst spur level is – 53.2 dBc, and well within specification.

Conclusion

This project turned out to be satisfying on several levels. First, I got to have a detailed look at the performance of a frequency doubler implemented with a quadrature driven mixer. The test data showed that by using a highly accurate phase shift network, a well-balanced power splitter, and a mixer with high isolation; good suppression of the undesired outputs could be obtained. Using available surface mount components the suppression of the fundamental and odd harmonics was found to be more than 50 dB. While the even harmonic spurs were not as well suppressed, an attenuation of more than 25 dBc of the fourth harmonic was achieved for the surface mount version and well over 30 dBc for the "hanging breadboard".

Taking advantage of the good spur performance of the QDMD, a low distortion output amplifier was designed which, with only minimal filtering, resulted in the complete assembly easily achieving the –50 dBc spur level goal. Using impedance transformation to tailor the load seen by the amplifier, it was possible to ensure low distortion Class A operation, while still operating with the limited current available from the FS321A-1 power supply. Finally, the objective of making the old 5 MHz frequency standard supply 10 MHz reference signals was implemented. The modified

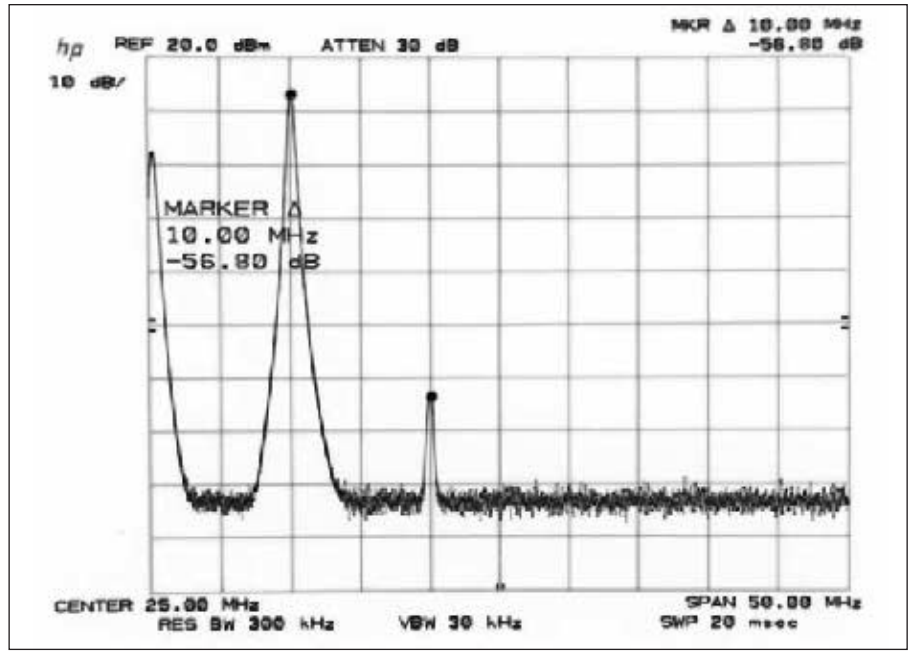

Figure 19 – Amplifier stage harmonic distortion with the amplifier driven at 10 MHz with –3.6 dBm input and the output set to +13 dBm. The second harmonic is at –56 dBc owing to the low pass roll off of the output network and low distortion Class A operation.

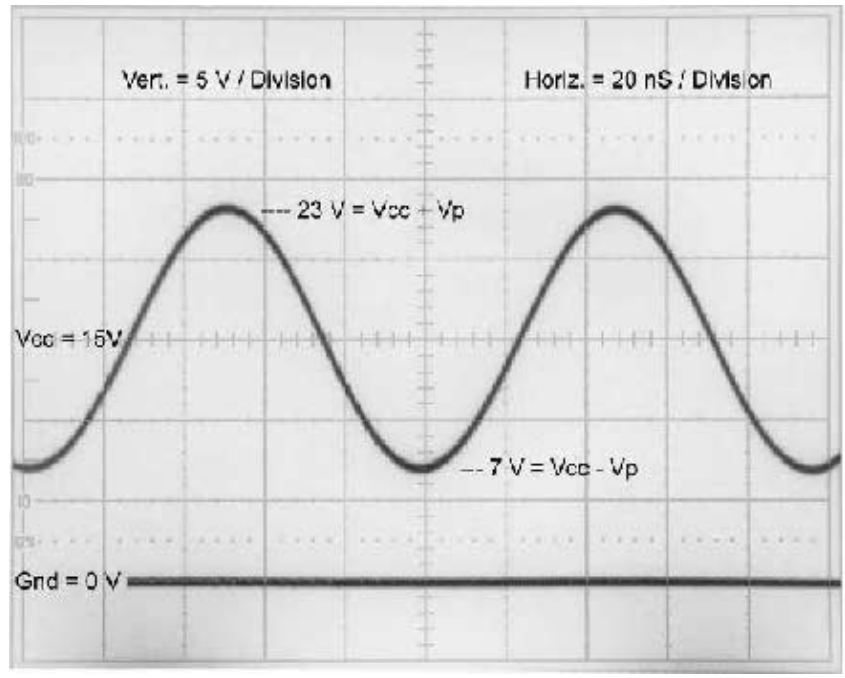

Figure 20 – Waveform at the collector of Q1 with +16 dBm (40 milliWatts) output to the 3 dB pad between the amplifier and J2. The peak to peak voltage at the collector is 16 V_{p-p} and it swings +/- V_p (8 V) above and below the 15 V_{cc}. At the lowest point on the collector waveform the voltage is 7 V or 3 V above the 4 V base voltage, keeping the transistor well above the clipping point.

Vectron oscillator and the PTF distribution amplifier have been chugging along for several months supplying 10 MHz reference signals to my lab equipment. It is most satisfying to set up a frequency on a generator and see the frequency counter report exactly the same frequency to the nearest Hz. Of course for this to be useful, the old Vectron oscillator must stay on frequency. So far, periodic checking against my rubidium frequency standard indicates a frequency offset of -4.57×10^{-10}Hz, and an aging rate of -1.75×10^{-11}Hz / day.

Hopefully some of the ideas and data presented here will be useful in other's projects. However I would be remiss not to point out a couple of virtues and disadvantage of this type of frequency doubler. Of the virtues, it has been shown that the QDMD is simple, operates over a wide range of input powers, and provides very good spur rejection. It was fast and easy to design by using a spreadsheet to develop the phase shift network.

On the other hand, considering only the cost of parts, the QDMD is not the lowest cost implementation of a doubler. There is always a cost tradeoff between the recurring unit cost and the time/cost of designing the circuit. In my case, I needed only one unit. Thus the relatively high cost of the mixer and power splitter could be advantageously traded for high performance and reduced time to design the circuits.

For anyone wishing to duplicate the circuit a parts list is provided in the files on the *QEX* website. There is nothing critical or fussy about the design. It can be implemented using a 2N2222A, with leaded components, and point to point wiring, or on a PCB with surface mounted parts as shown here.

John Roos, K6IQL, was first licensed in 1955 and obtained his BSEE from California State Polytechnic University in 1964 where he specialized in RF and Microwave Engineering. Until recently he has worked in the RF area in various positions from Junior Engineer to Engineering VP while designing a variety of transmitters, receivers, and other RF devices for the Electronic Defense and Aviation Navaids industries. He has two patents in the areas of spread spectrum communications and electronic warfare receiver calibration. Amateur Radio interests have always included precision frequency measurement as well as building VHF low noise receivers and high power transmitters. During the Vietnam conflict he operated an all home brew AM 2 M repeater for Navy MARS on 5000-ft. Mt. Wilson in Southern California. He has published articles in 73 Magazine *and others. He is a member of the IEEE, the ARRL, the NRA, and a former member of the Association of Old Crows. Presently retired, he lives in Spring Hill, Kansas with his wife, Barbara, and is enjoying tinkering with assorted ham radio and machine shop projects.*

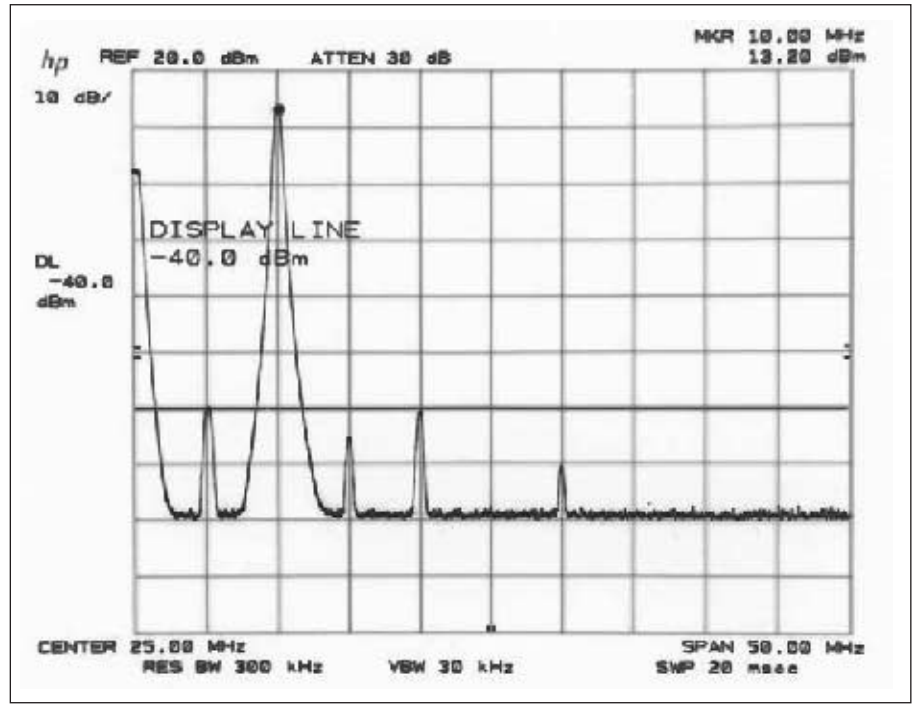

Figure 21 – Performance of the 5 to 10 MHz Doubler installed in the Vectron FS321A-1 Frequency Standard. The spectrum analyzer marker indicates a 10 MHz output of +13.5 dBm. The display line marker is set just above the highest level spurious output; 5 MHz at –40 dBm, or –53 dBc.

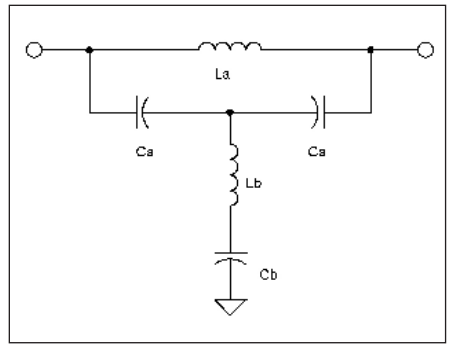

Figure 22 – Second Order All Pass Phase Shift Network. In practical designs C_b may be omitted if the reactance of C_b is very much less than the reactance of L_b. The network is symmetrical; either end may be used as input or output.

NOTES

[1]Vectron Laboratories Inc., Norwalk Connecticut, USA

[2]G. Kamas and M. Lombardi, "Time and Frequency Users Manual", *NIST Special Publication 559*, 1990, **www.tf.nist.gov/general/pdf/461.pdf**

[3]WWVB Station Library, **www.nist/gov/physlab/div847/grp40/lflibrary.cfm** has archived files of the early history of WWV, WWVB, and WWVL to the present day.

[4]Jerry R. Norton, Jim M. Cloeren, and Peter G. Sulzer, "Brief History of the Development of Ultra Precise Oscillators for Ground and Space Applications," *Proceedings of the 1996 IEEE International Frequency Control Symposium*, pp. 45-57. **www.ieee-uffc.org/main/history.asp?file=norton**

[5]Precise Time and Frequency, Inc, 200 Corporate Place, Peabody, MA 01960 USA, **www.ptfinc.com**

[6]1Lt. Gary L. Dieter, Capt. Gregory E. Hatten, "Observations on the Reliability of Rubidium Frequency Standards on Block II/IIa GPS Satellites" US Air Force, Falcon AFB, Colorado Springs, CO 80912

[7] *Precise Time and Frequency Catalog*, Specifications for 1203C RF Distribution Amplifier, Page 7, See also specifications for 2210A and 2211A Quartz Frequency Standards, Page 13. Precise Time and Frequency, Inc, 200 Corporate Place, Peabody, MA 01960 USA. **www.ptfinc.com**

[8]Hewlett-Packard, *1986 Hewlett-Packard Catalog*, Hewlett-Packard Co., 3200 Hillview Ave., Palo Alto, CA. 94304. Page 257, specification for HP 105B Quartz Frequency Standard, see also Page 258, Specification for Model 5087A Distribution Amplifier

[9]Table 1-1 Specifications, *HP8672A Synthesized Signal Generator Operating and Service Manual*, **www.agilent.com**

[10]Phillips Semiconductor, "Application Note AN1983 Crystal Oscillators and Frequency Multipliers using the NE602 and NE5212", Dec 1991

[11]Arthur B. Williams, *Electronic Filter Design Handbook*, Chapter 7, pp. 7-3 through 7-6, McGraw Hill, New York, 1981, ISBN 0-07-070430-9

[12]Data Sheets may be viewed at **www.minicircuits.com**

[13]Motorola Inc. *Radio, RF, and Video Applications*, First Edition 1991, pp. 105-108, Motorola Inc, PO Box 20912, Phoenix, AZ 85036

[14]Mark J. Wilson, Editor, *The ARRL Handbook for Radio Communications 2008*, 85th Edition, pp.14.60, ARRL – the national association for Amateur Radio, Newington, CT 06111 USA. **www.arrl.org**

Designing The Phase Shift Network

A second order L-C all pass network was used to obtain the –90 degree phase shift required for the doubler. Design of these networks is described in Section 7.2, Chapter 7 in *Electronic Filter Design Handbook*. For those unfamiliar with this work, it is a most useful reference for the non-specialist engaged in occasional filter design. The equation numbers below correspond to those in the reference. In Equation 7-10 the phase shift of a second order all pass transfer function is given as

$$7\text{-}10 \qquad B(\omega) = -2 \tan^{-1} \frac{\frac{\omega\,\omega_r}{Q}}{\omega_r^2 - \omega^2}$$

where:
$B(\omega)$ = Phase Shift in Radians at Radian Frequency ω
$\omega = 2\pi \times f$ (Hz), where f is the operating frequency of the phase shifter
$\omega_r = 2\pi \times f_r$ (Hz), where f_r is the resonant frequency of the phase shifter
Q = Q of the network.

In the reference several circuit topologies are presented that will implement the above transfer function. The one I used is presented in Figure 7-6(b) of the text and reproduced here as Figure 22.

Referring to Figure 22, two capacitors having the same value, Ca, are used, so a total of 2 inductor values and 2 capacitor values are required. The following equations give the element values.

$$7\text{-}17 \qquad L_a = \frac{2R}{\omega_r Q}$$

$$7\text{-}18 \qquad C_a = \frac{Q}{\omega_r R}$$

$$7\text{-}19 \qquad L_b = \frac{Q\,R}{2\,\omega_r}$$

$$7\text{-}20 \qquad C_b = \frac{2\,Q}{\omega_r (Q^2 - 1)\,R}$$

To solve for the element values we need Q, R, and ω_r. Q is user specified and must be more than 1. Setting Q to 1.001 will avoid a divide by zero problem in 7-20. R is the specified phase shift network impedance. In this case, R = 50 Ω. That leaves ω_r which must be determined from 7-10. Solving 7-10 for ω_r for a specified B, ω, and Q would make it possible to determine ω_r directly, but a numerical approach using a spreadsheet was faster and a lot less work. The spreadsheet "Second Order All Pass Phase Shifter.xls" is on the *QEX* website. Frequency data is input as f, the operating frequency and f_r, the resonant frequency. For convenience, both are input in MHz and are converted to radian frequency by the spreadsheet.

To design the network, the designer enters the operating frequency, f, the impedance, R, and the Q. A trial value for f_r is entered, converted to ω_r, and the resulting phase shift is computed. It is displayed as both radians and degrees. The phase shift is noted and f_r is manually adjusted until the required phase shift is obtained. Usually only a few tries are required to achieve an acceptable result. The component values, for Figure 22, giving the required phase shift are computed at the same time. Positive or negative phase shifters may be designed. If f_r is above f, the phase shift is negative. If f_r is below f, the phase shift is positive.

This example illustrates some of the math. It assumes that f_r (i.e. ω_r) has been found by iteration using the spreadsheet.

Given:

Operating frequency	5 MHz
Required phase shift	–90 degrees
System Impedance	50 Ω
Network Q	1.001
Resonant Frequency	8.1 MHz (found by iteration)

First compute:

$\omega = 2\pi \times 5.0 \times 10^6 = 3.144 \times 10^7$

$\omega^2 = (3.14 \times 10^7)^2 = 9.870 \times 10^{14}$

$\omega_r = 2\pi \times 8.1 \times 10^6 = 5.089 \times 10^7$

$\omega_r^2 = (5.089 \times 10^7)^2 = 2.590 \times 10^{15}$

and inserting into Equation 7-10

7-10 $$B(\omega) = -2 \tan^{-1} \frac{\frac{\omega\, \omega_r}{Q}}{\omega_r^2 - \omega^2} = -2 \tan^{-1} \frac{\frac{3.144 \times 10^7 \times 5.089 \times 10^7}{1.001}}{2.590 \times 10^{15} - 9.870 \times 10^{14}}$$

$$B(\omega) = -2 \tan^{-1} \frac{1.597 \times 10^{15}}{1.603 \times 10^{15}} = -2 \tan^{-1} (0.996) = -1.567 \text{ Radians}$$

for $\omega_r = 5.089 \times 10^7$ radians/second and

The Phase Shift (degrees) = $B(\omega) \times \frac{180}{\pi}$ degrees

= -1.567 Radians x $\frac{180}{\pi}$ = 89.78 degrees.

Now the element values can be calculated.

7-17 $$L_a = \frac{2R}{\omega_r Q} = \frac{2 \times 50}{5.089 \times 10^7 \times 1.001} = 1.963 \times 10^{-6} \text{ H.}$$

7-18 $$C_a = \frac{Q}{\omega_r R} = \frac{1.001}{5.089 \times 10^7 \times 50} = 3.934 \times 10^{-10} \text{ F.}$$

7-19 $$L_b = \frac{Q\, R}{2\, \omega_r} = \frac{1.001 \times 50}{2 \times 5.089 \times 10^7} = 4.917 \times 10^{-7} \text{ H.}$$

7-20 $$C_b = \frac{2\, Q}{\omega_r (Q^2 - 1)\, R} = \frac{2 \times 1.001}{5.089 \times 10^7 \times (1.001^2 - 1) \times 50} = 3.932 \times 10^{-7}$$

Comparison of the doubler schematic, Figure 15, with the theoretical phase shift network schematic, Figure 22, shows that C_b was not used in my design. Rather L4 (corresponding to L_b) is connected directly to ground. This can be done, if as in this case, the reactance of L_b is many times that of C_b at the operating frequency. The spreadsheet calculates the two reactances and their ratio. For the –90 degree phase shift network used in the doubler, the reactance of the inductor is about 190 times that of the capacitor, so the capacitor was not used.

QEX

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SDR2GO: A DSP Odyssey

Build a SoftRock SDR without the need for a PC

Introduction

This article describes a group project that has resulted in a low cost kit[1,2] that allows an amateur to use popular Software Defined Radio (SDR) kits without having to lug around a Personal Computer (PC) plus Sound Cards. The resulting HF transceiver provides good performance with one-watt power output and may be packaged in a small case with self-contained battery. The SDR2GO board provides for SSB operation with headphones and microphone or digital mode operation such as PSK31 or RTTY with stand-alone modems such as the NUE-PSK Digital Modem.

Let's Cut to the Chase

Here is a brief description of SDR radio technology plus the features of the SDR2GO board. The basic principle underlying SDR technology is that a signal may be demodulated by converting a single received RF signal into two separate signals which have a 90-degree relative phase shift. This function is performed by the SoftRock with the two output signals being in the audio spectrum. These two signals are called the in-phase (I) signal and the quadrature (Q) signal.

However, the SoftRock received IQ output signals contain both sum and difference products. The SDR2GO board provides algorithms for converting the two SoftRock IQ signals into a single, desired audio signal. In order to select between the sum or difference products an additional 90 degrees of phase shift is inserted between the I and Q signals. Then, the I signal is added to the Q signal to produce just the difference products, or the Q signal is subtracted from the I signal to produce just the sum products. The resulting audio signals are filtered to restrict the received audio signal to the desired range of frequencies.

Signal modulation is performed in a similar manner. A single audio signal such as a microphone input is first filtered and then converted into separate audio I and Q signals. This function is performed by the SDR2GO board. These two signals are fed into the SoftRock where translation to the radio frequency is performed and an additional 90 degree phase shift is inserted between the I and Q RF signals. The resulting two signals are combined within the SoftRock to produce the desired modulated RF output signal. The signal processing described has been used since the early 1950s and has long been referred to as the "Phasing" method of SSB modulation and demodulation.

A strong advantage of using DSP to perform signal modulation and demodulation is that the required mathematical functions such as multiplication, addition, subtraction and phase shift are performed with

SDR2GO Project Features

The following list describes the features of the SDR2GO project:
I/Q Signal Demodulation
I/Q Signal Modulation
Headphone Output
Microphone/Line Audio Input
PTT Input
PTT Output for control of SoftRock receive/transmit operation
Effective Receive AGC
Si570 Frequency Control
Backlit 16 X 2 LCD Frequency and Status Display
Main Rotary Encoder for frequency control and Si570 parameter definition
Keyboard Port for Si570 parameter definition and real time frequency control
Secondary Encoder for setting DSP parameters
USB/LSB selection switch input
Microphone/Line selection switch input
Output Audio/IQ Amplitude adjust selection switch input
IQ Phase adjust/Default IQ parameter selection switch input
EEPROM storage for Si570 control and DSP parameters
Onboard mounting of Si570 as an option
Physical access for I2C interface for mounting Si570 on SoftRock RXTX
Five bit data interface between dsPIC and SH32 or other devices for future use
Three bit data interface for controlling a switched band pass filter
Physical access of dsPIC SPI data interface for future interface with other devices
Physical access for programming dsPIC
Physical access for programming SH32 Processor
Five Volt Power Input
Board size identical to SoftRock RXTX Version 6.3 footprint
Board layout and device pads designed to accommodate hand soldering

[1]Notes appear on page 43.

much greater precision than can be achieved using traditional analog circuitry. In the early days of SSB, the phasing method of SSB signal processing was quite popular and produced great sounding signals. However, the unwanted signal rejection was limited to the range of 30-40 dB. This was the result of the RF and audio phase shift networks not being balanced in amplitude and phase over the entire frequency range of operation. With DSP it is possible to match both amplitude and phase shift over a wide range of operation with much greater precision than analog circuits. As a result, it is possible to achieve unwanted signal rejection typically greater than 50 dB. DSP provides filtering which is much better behaved than traditional analog filters. Much steeper skirts may be achieved without ringing than when using crystal or LC filters. Moreover, the pass band ripple is minimal.

The SDR2GO provides for frequency adjustment and display plus typical operator controls such as audio output level adjustment, sideband selection, and input audio type selection. The SDR2GO functions described above are typically performed using a PC with two soundcards and one of several free software applications. The performance is great but the resulting rig is bulky and cumbersome. And unless you use a laptop or netbook with built in battery supply, power becomes an issue when portable operation is desired.

The group effort has produced the SDR2GO kit with the major features listed in the sidebar.

The Design Odyssey

The story of the design evolution is presented below for two reasons. First, we had a great group effort where each member contributed whatever technical skill he could. I am convinced that by working as a group we were able to develop a much more richly featured kit than by one person working alone. Hopefully, by describing the efforts we will encourage others to develop and share such group projects. Second, by describing in gruesome detail the design process we will answer many of the readers' questions regarding why we used one technique or device over another. Undoubtedly, some readers will have their own pet techniques and devices. I hope this article will encourage them to develop their own ideas and share the results with others.

I have enjoyed building battery powered QRP transceivers since the early 1970s. After a long building hiatus, I renewed my interest in building when I realized that we were due an increasing sun spot cycle and retirement was on the horizon. I found an interesting article in *Experimental Methods in RF Design* which described a 17-meter transceiver that used a Digital Signal Processor (DSP) to provide for IQ demodulation and IQ modulation for SSB operation.

The DSP processor used in the article was available from TAPR so I purchased one. It worked but there were a couple of drawbacks. The processor did not have the entire necessary switch IO available for operating the transceiver with the software provided with the article, and the programming software for the processor will run only on a *DOS* platform. Not having the patience to endure *DOS* again, I put this project on the shelf.

At this point other hams in my area were talking about SoftRock receivers. I did not pay much attention since my main interest is with transceivers. Instead, I cruised the Internet looking at available SSB QRP transceiver kits. I also searched for DSP evaluation boards that were supported with programming software that runs under Windows XP. I found quite a few transceiver kits and a number of evaluation boards. Most of the transceiver kits were focused on CW operation using traditional crystal filters, and most of the evaluation boards were quite expensive ($350 to $500).

Then I discovered a relatively new SoftRock kit: the RXTX V6.2. This kit is a full transceiver and allowed me to do SSB and other modes of operation. All that was required besides the RXTX was a PC with two sound cards and software that was available for free. I was very pleased with the results. Having gained some maturity and restraint, I very methodically constructed the SoftRock RXTX kit and took my time. It worked the first time! There was no tuning procedure or extra test equipment required, no birdies, and it sounded great. I was hooked! At that time the RXTX was available as set of kits that allowed the user to operate on a couple of bands such as 30/40 meters or 17/20 meters. So, I built a number of RXTX kits and really enjoyed the building.

I still enjoyed portable operation so I deployed a QRP rig, which included a laptop with PCMCIA soundcard for DSP interface, SoftRock RXTX with self-contained lithium battery, and a simple dipole antenna. I had the fun of taking this lashup on several trips to Europe while still employed. I did attract a number of staring onlookers when I operated from a park bench near the Seine in Paris!

The prospect of using an embedded DSP processor instead of a PC still intrigued me. I kept scouring the Internet looking for low cost DSP boards. Finally, at the end of 2007, Freescale announced a relatively low cost ($150) board called the SoundBite. This board is fairly compact (4 × 5 inches) and has four separate stereo channels. Further, each stereo channel can sample at rates up to 192 kbps and provide 24-bit resolution. The processor is fast with 180 million instructions per second (MIPS). Since this board was just becoming available, the programming software ran on the latest *Windows* platforms, so I purchased one. At this time I was a firm believer that 24 bit analog to digital conversion (ADC) and digital to analog conversion (DAC) was absolutely necessary for obtaining good results with a SDR. This was the main motivation for my purchasing a SoundBite.

The SoundBite board is provided with comprehensive programming software that supports both assembly language and C programming. I opted to write my SoundBite programs in Assembly language because I had an aversion to taking the time to learn C. My initial implementation used one of the four stereo channels for receive signal processing and another channel for transmit. Results were good.

This version of SDR used the Si570 chip along with the microprocessor controller developed by John Fisher, K5JHF, and Kees Talen, K5BCQ, as the VFO. This unit included a rotary encoder for configuration and frequency control along with a nice, wide LCD display. The Si570 chip has been used in several different modes with Soft Rocks to provide frequency control. The unique feature of the Talen/Fisher VFO unit is the very smooth frequency stepping done by the software. This allows the user to adjust the Si570 in a manner very similar to tuning with a variable capacitor and vernier drive.

At this time I moved to my present location near Austin, TX, and I started meeting with the Austin QRP Club. John Fisher, Kees Talen plus Milt Cram, W8NUE, are quite active with this group. During one meeting I brought along my SoundBite based SDR and I timidly showed it to the group. I was astounded by the interest and compliments. It turns out that several of the group had like interest and had done some work on a similar concept using the Microchip dsPIC technology. As a result, several of the group purchased their own SoundBite boards and began experimenting.

After numerous conversations and emails the group decided to build prototypes of a homebrew SDR using the SoundBite Board design to include the same DSP processor and codec. The only difference between our prototypes and the SoundBite board was that the prototypes used a single codec instead of four. The motivation to use a single codec was to reduce current draw. This change required that we employ switching of audio signals for the inputs and outputs so that both

receive and transmit processing could be done using a single codec.

We were able to get the prototypes to work and the results were comparable to the SoundBite version. There were several drawbacks with the prototypes, however. First, we had to add a lot of audio gain in front of the codec and after the codec to get proper audio levels for receive and transmit. We replicated the SoundBite circuitry to implement a JTAG interface for in circuit programming and debugging of the DSP processor. Although we tried a number of third party JTAG interfaces which were advertised as being compatible with the Freescale DSP processor we were never able to get the JTAG port on our prototypes to work. This required that we do programming using a SoundBite board and then burn the program into a DIP packaged EEPROM. Then we would physically move the EEPROM to our prototype boards. This mode of programming proved to be too onerous.

About this time, relatively low priced netbooks began to appear on the market. Kees Talen had the audacity to use one with the built in sound card which provided 48 kHz sampling with 16-bit resolution. It worked well! I also tried this approach using a SoftRock RXTX and a netbook and was well pleased with the 16-bit resolution soundcard processing of the IQ signals.

During this period of group interaction, the prospect of using a dsPIC with 16 bit processing and 16 bit codec continued to bubble to the top of the conversations.

Reviewing the dsPIC technology I learned that the dsPIC family provides 16 bit processing with speeds up to 40 MIPS. This is the same ultimate speed that was available with the DSP processor that I first purchased from TAPR. Calculations based on the examples shown in the *Experimental Methods in RF Design* article revealed that running at 40 MIPS the dsPIC could handle 48 kHz sampling and DSP processing without overloading the DSP processor.

The group had also been looking at codec candidates. The codec of choice was the TI TLV320AIC23BPW. It provides for sampling up to 48 kHz at 16-bit resolution. The typical ADC signal to noise ratio is 85 dB. Further, it provides separate inputs for line input and microphone plus separate line outputs and headphone outputs. There was already a precedent for using this codec with a dsPIC to field a SSB transceiver. Juha Niinikoski, OH2NLT, shared details of his "Cheap DSP" project on his website.[2]

Juha was kind enough to respond to several emails, and he provided source code on his website. In particular, the code included an assembly language program which executes two straightforward Finite Impulse

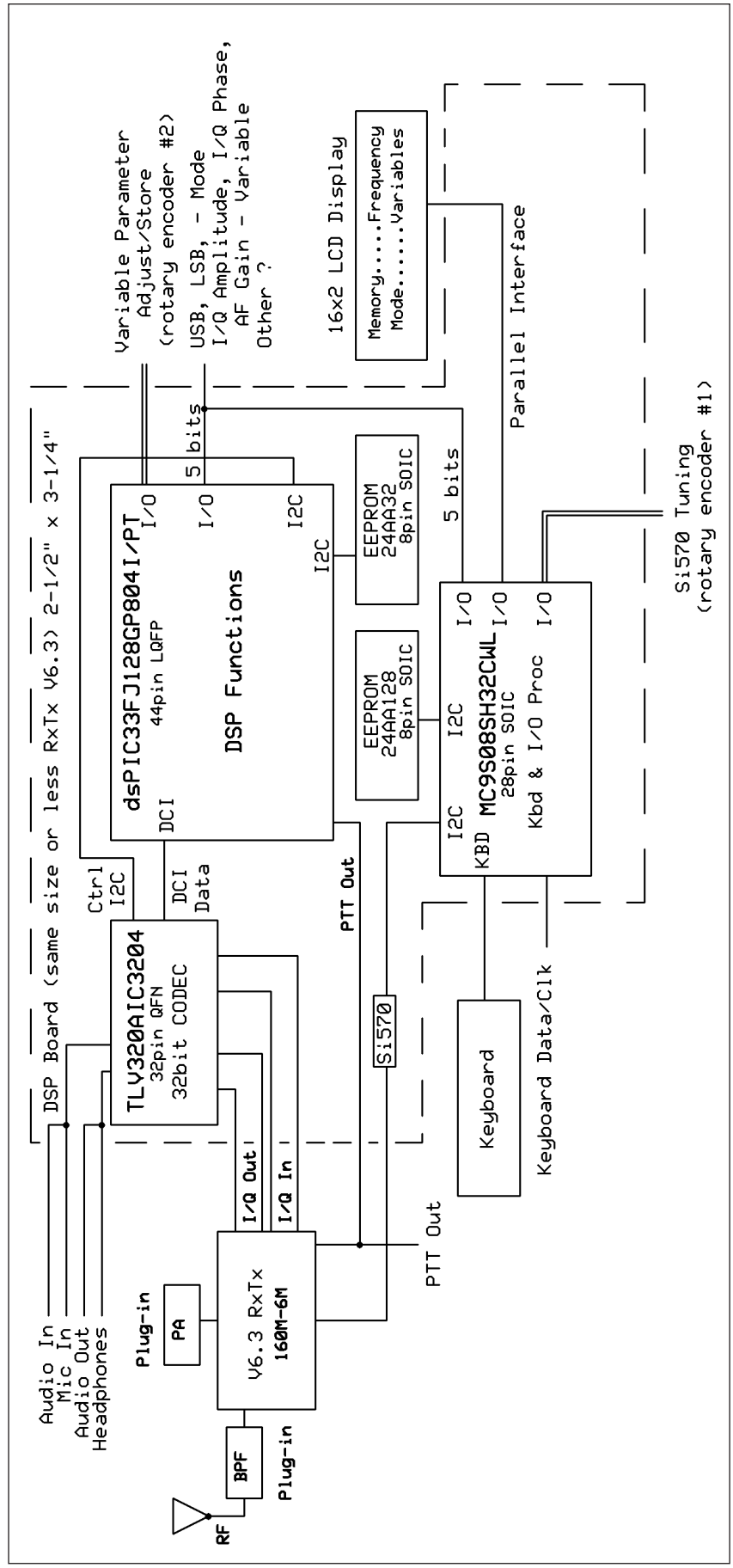

Figure 1 – A block diagram of the transceiver.

Response (FIR) filters. These filters provide two necessary functions. They limit the received and transmit audio to frequencies below 1400 Hz, and they provide a relative 90 deg phase shift between the I and Q channels which is required for signal modulation and de-modulation. Not being familiar with using filters which provide both band limiting and 90 deg phase shift I decided to do some research on this technique. My research led me to the great text written by Marvin E. Frerking entitled *Digital Signal Processing in Communication Systems*. Frerking describes this technique which is called a "Hilbert Transformer". The techniques described were used to modify the Cheap_dsp filters to provide additional low frequency noise rejection.

Prior experience had shown that using the Hilbert Transform method of modulation and de-modulation at base band frequencies does have the drawback of being susceptible to 60 Hz power based emissions. So, instead of using a low pass filter for the Hilbert Transformer, filters with a pass band of 300-3000 Hz are used in the SDR2GO algorithms.

At this point the group decided to build hand wired prototypes using the TLV320AIC23BPW codec with the dsPIC33FJ128GP802. The codec only comes in SMD packaging while the dsPIC is supplied in a DIP package. Fortunately, the codec SMD package is fairly large making hand soldering easy. Kees Talen was kind enough to provide codecs mounted on a convenient carrier board for the team members. John Fisher provided the group with a dsPIC shell C program which provided the basic interface between the codec and dsPIC.

At this point I had to bite the bullet. Although I have been programming (hacking around really) in a number of languages since the 1960s I had always resisted programming in C. So, I took the deep dive and got my feet wet. Thanks to the patience of John and Milt Cram who answered numerous questions and pleas for mercy I was able to modify John's code to include the Hilbert Transformer code embedded in the Cheap DSP Project.

The group was then able to quickly build working prototype SSB/PSK rigs using the DSP board, the K5BCQ/K5JHF Si570 Controller VFO, and a SoftRock RXTX. Results were good. In particular, since the codec is provided with separate dual inputs (microphone and line) plus dual outputs (headphone and line) all transmit/receive audio switching was performed in the codec with the dsPIC application program directly controlling he codec operation via an I2C control bus.

However, overall receive audio output was low. Instead of adding amplification stages between the SoftRock receive IQ signal and the codec ADC input, we provided gain within the DSP algorithm by left shifting the raw analog input data by two to four bits to achieve gains of four to 16. This was crude but effective.

At this point in the design evolution we decided to add user functionality of adjusting IQ signal amplitudes and phase shift between I and Q signals. In order to achieve maximum unwanted signal rejection using IQ processing the amplitude of both I and Q signals must be equal and the relative phase shift must be 90 deg at all frequencies. Each SoftRock will exhibit slight differences in IQ amplitudes and relative phase shift. There are actually two sets of amplitudes and phase shift, one for the SoftRock receive chain and one for the transmit chain.

After implementation of the encoder functionality, unwanted signal suppression of 50 dB was obtained with the SoftRock on both transmit and receive. Further, an EEPROM was added to the DSP board so that the receive and transmit parameters may be stored by depressing a switch on the encoder.

We were pleased with the results but we still viewed the rigs to be lacking in two respects. First, having to use a rude and crude method of signal amplification in the DSP algorithm was not esthetically pleasing. Second, the rig really needed an effective AGC system.

During this period the team was still stalking possible codec candidates. Our attention then focused on the TI TLV320AIC3204. This codec is similar to the TLV320AIC23BPW codec in that it has dual inputs plus dual outputs. The advantage of this codec is that it has gain blocks ahead of the ADC and after the DAC. The gain of each of these gain blocks may be adjusted on the fly using the I2C control bus. So, not only did this codec eliminate the need for external gain blocks, it provided an avenue for implementing AGC for the receive chain.

However, there is one drawback to using this codec. It is only available as a 32 pin QFN package. I decided to build another hand wired prototype. Again, Kees came to the rescue by providing a sample TLV320AIC3204 installed on a header board.

Getting this codec to work required a rewrite of the code that configures the codec. Fortunately, we found a route to plagiarism. TI had just announced the release of their cheap (~$50) TMS320VC5505 eZDSP USB Stick evaluation board that uses the TLV320AIC3204 codec. Unfortunately, this board does not provide physical access to the multiple input ports and output ports so it is not a candidate for a transceiver. But TI provided source code for basic codec configuration which we were able to port to the dsPIC platform.

Getting the newer prototype to work was fairly straightforward and required the normal amount of gnashing of teeth. Once we were able to configure and control the codec all worked well. We were then able to implement AGC!

Again, I relied on Frerking's *Digital Signal Processing in Communication Systems*. Pages 339 through 342 provide a detailed description of a DSP based AGC scheme. This scheme does require calculation of the logarithm of a number. This is a standard feature of the C language. Also, the result of the AGC calculation is a value that represents gain in dB. This is ideal for interface with the codec since the codec control interface requires that the gain be set in dB. The end result is an AGC algorithm which works well. Thanks to input put from Milt Cram, the final AGC is implemented with fast attack and slow decay behavior.

At the beginning of this odyssey I viewed the DSP processor as being the key component with the codec playing second fiddle. However, with this design experience I have come to the conclusion that the codec is really the key item for having excellent DSP performance for a SDR. After reaching the milestone of implementing effective AGC using the TLV320AIC3204 with dsPIC, the group decided it was time to design and fabricate a board. One of the main desired features of the board was to incorporate the DSP processing with the Si570 control and display. This was a firm requirement for replacing a PC with a stand-alone board.

Si570 Control

The Si570 device has been used in a number of ways to provide frequency generation for SoftRock receivers and transceivers. This device first came to my attention as a result of a post made by Tom Holflich, KM5H, in August 2007. Silicon Labs which has headquarters in Austin, TX, developed the Si570. We have been very fortunate in being able to locate the engineer responsible for this great device, and he has attended several of our club meetings. He described the effort to design and manufacture this device.

The Si570 has a frequency range ideal for controlling a SoftRock which requires that the clock run at four times the desired receive or transmit frequency. Moreover, the phase noise of the clock is exceptionally low. The clock is crystal controlled and provides good stability once the device reaches quiescent temperature. Silicon Labs provides a detailed datasheet and a comprehensive application note (AN334: Si57X ANSI C Reference Design). These documents have allowed several amateurs to develop a number of great applications for controlling the Si570 by

using a PC or an embedded microprocessor.

The Si570 is crystal controlled and the characteristics of each device are unique to the crystal. Part of the manufacturing process is to test the device crystal so that a set of configuration parameters may be calculated and stored in the Si570 onboard memory. These parameters are accessed by the controller microprocessor so it may properly control the frequency of the Si570.

The Si570 is controlled via an I2C bus. This is the same protocol used to control the TLV320AIC23BPW codec. During the early discussions of developing the dsPIC solution the idea of controlling an Si570 with the dsPIC instead of using a separate microprocessor was considered. Of course by this time the Kees – Fisher Si570 Controller was well developed and proven. As the development of the dsPIC plodded along, it became evident that it would be best to use two separate processors, the dsPIC for DSP and the Freescale MC9S08SH32CWL (SH32) for Si570 control.

The Si570 is provided with a digitally controlled oscillator (DCO) plus two separate frequency dividers, one with three bit resolution and one with seven bit resolution. The frequency of the DCO may be set with 38 bit resolution within its operating range of 4.85 to 5.67 GHz. The resulting resolution of the Si570 output is 0.09 parts per billion over the range of output frequencies. The SDR2GO SH32 manipulates the DCO frequency plus frequency dividers to provide read out resolution down to 1 Hz. The SDR2GO algorithm takes further advantage of this resolution to provide frequency stepping that is quite smooth.

When ordering an Si570 the user may specify a default startup frequency. A unique feature of the SDR2GO Si570 controller is that simply entering the default startup frequency the controller algorithm will be automatically calibrated. This feature is achieved by the controller algorithm interrogating the Si570 to read the device parameters measured during factory device testing and are stored in the device. The SDR2GO then uses these parameters to perform the control algorithms.

Configuration of the Si570 controller may be done in two ways. One way is to use the rotary encoder which is provided with a pushbutton switch. By manipulating the switch plus encoder the configuration parameters may be set. A keyboard port and interface with the SH32 is provided for keyboard entry of configuration parameters. The following parameters may be configured using the encoder or keyboard:

Startup Memory Location
Startup Cursor Position
Output Frequency Multiplier
Output Frequency Divisor
Display Multiplier
Display Divisor
Tune Rate for Encoder
Tune Direction for Encoder

Twelve characters of alphanumeric display may be programmed by the user. Up to 32 alphanumeric combinations may be stored. The selection of the combination displayed is controlled by five input bits which are accessible by the user.

In addition, up to 958 frequencies may be stored for selection via the encoder or keyboard. Each stored frequency may also have an offset specified (+ or –) in addition to a desired band value. The band value drives three output bits which may be interfaced with a switched band pass filter. The keyboard port may also be used to control the Si570 frequency during normal operation.

Final Design

Figure 1 is a block diagram of the final design for the SDR2GO board. Figure 2 is a photo of the first prototype board. Figures 3 and 4 are photos of Milt's completed SDR2GO prototype. Figure 5 and Figure 6 are photos of my SDR2GO prototype.

We felt the requirement of accommodating hand soldering is key to reaching our goal to get more hams building. Kees Talen took the lead on this design goal since he has had a great deal of experience in putting together the popular Si570 VFO Kit. The board was designed as a double layer board with the DSP portion laid out along one side and the Si570 portion along the other side. Of particular note, Kees made sure that all of the mounting pads for SMD devices were sized to accommodate hand soldering and that there is adequate physical access to all mounting locations.

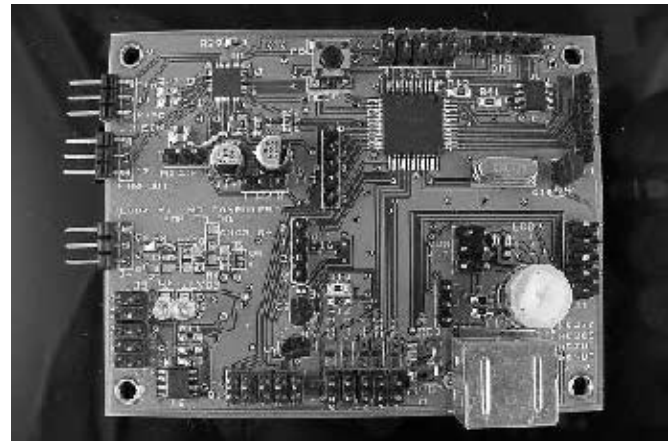

Figure 2 -- The populated printed circuit board.

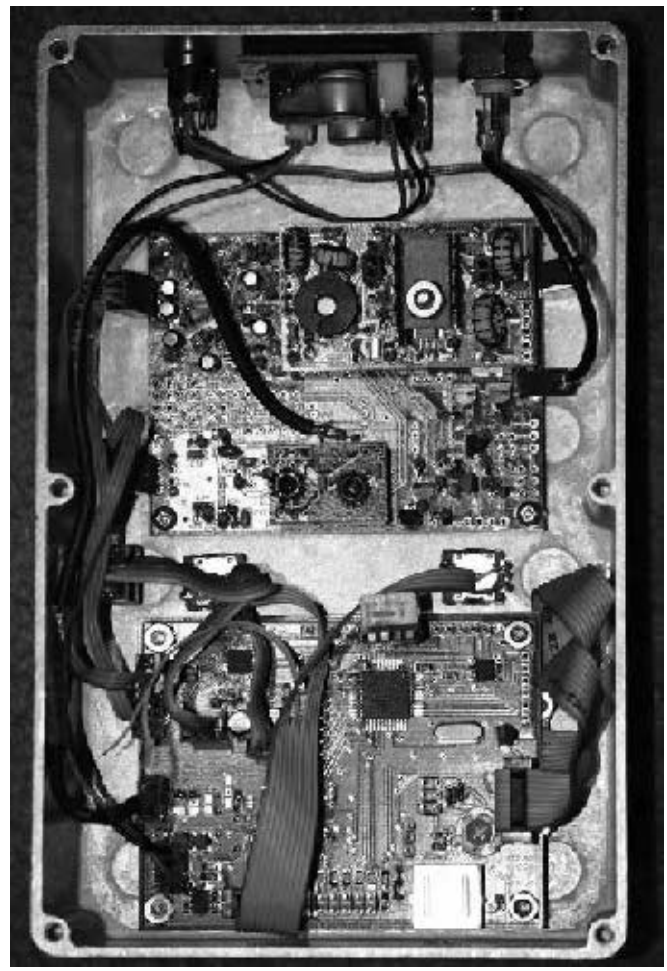

Figure 3 – Top view of the inside of a complete transceiver built by W8NUE.

Hilbert Transformer Design

Experience had shown that using the Hilbert Transform method of modulation and de-modulation at base band frequencies has the drawback of being susceptible to 60 Hz power based emissions. So, instead of using the 69 tap low pass filter included in the Cheap_dsp project as the basis for the Hilbert Transformer, a pair of band pass filters were designed using *Signal Wizard* Version 1.7. *Signal Wizard* allows the user to design a filter with a specified phase shift. The band pass chosen was 300 to 3000 Hz with a sampling rate of 12,000 samples per second. One filter was specified with a phase shift of 45 deg and the other with a phase shift of 135 deg. The net phase shift is the required 90 deg shift required for IQ modulation and demodulation. Figure 7 is a screen shot from *Signal Wizard*. At the 12,000 sample rate, a filter with 128 tap size was chosen to yield the desired band pass response as shown.

Figure 4 – View of the completed transceiver showing the simplicity of the user interface.

Receive Performance

A Hewlett Packard 8640A Signal Generator was used to produce a calibrated test signal from –130 dBm (0.1 µV) to –30dBm (10 mV) for evaluating receiver performance. A 24 bit Soundcard was used to interface received audio with a software application for signal processing and display. The screenshots in Figures 8 and 9 show the audio spectra of the SDR2GO headphone output signal using the audio analysis application entitled *Goldwave*. The horizontal axis represents audio frequencies between 0 and 12 kHz. The vertical axis represents amplitudes between 0 and –100 dBm.

The receive signal results at –110 dBm and –130 dBm with AGC applied are shown in Figures 8 and 9 respectively. The SDR2GO is configured so that the received signal is ported to both the left and right headphone output driver. So, each of the two stereo channels are handling the same received signal. Further testing shows that with AGC applied the SDR2GO is useable with signals up to –30 dBm, giving

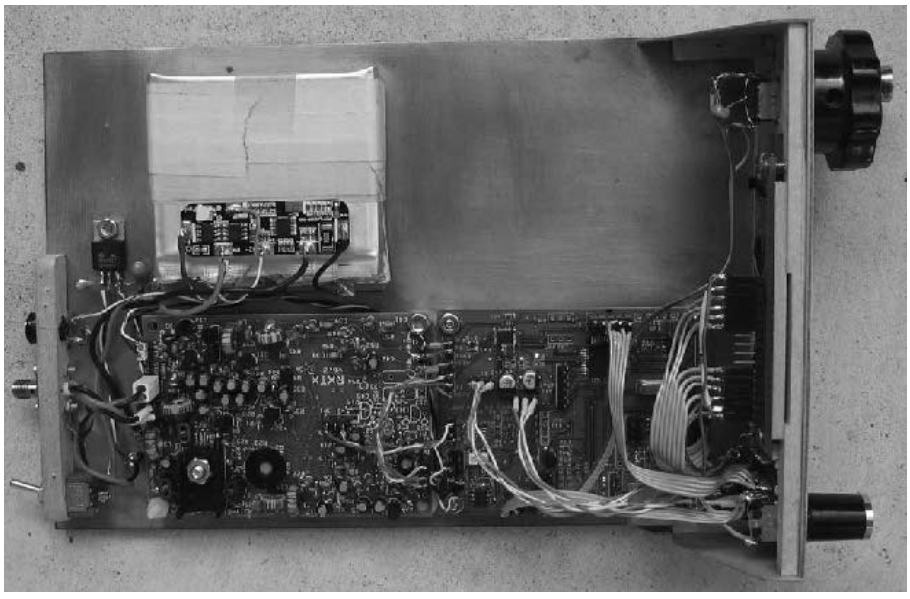

Figure 5 – View of the author's simpler complete transceiver showing the lithium battery pack

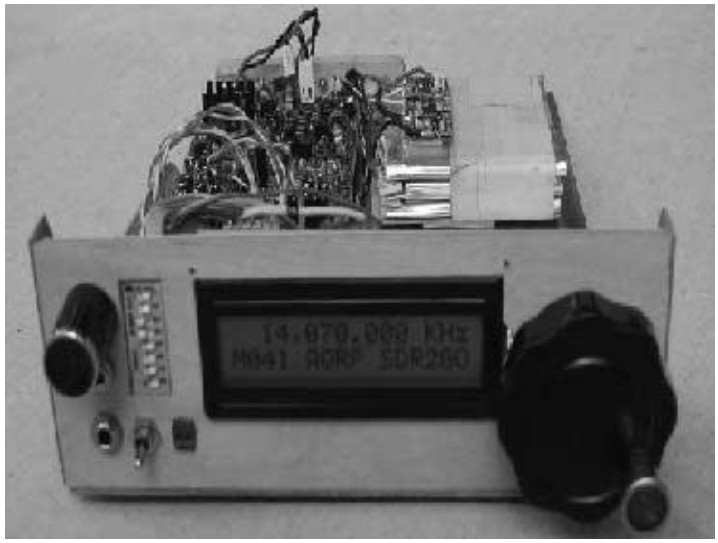

Figure 6 – Front panel of the author's transceiver

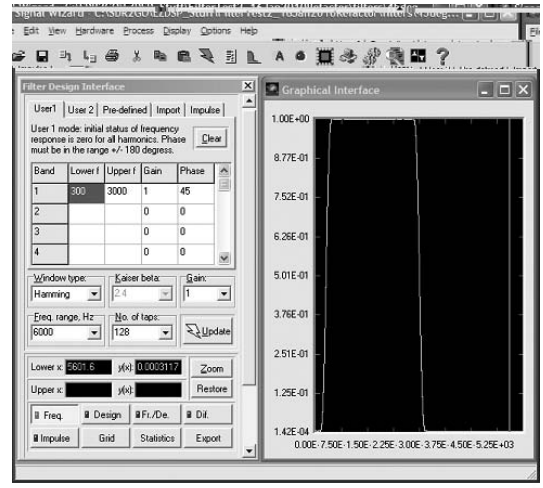

Figure 7 – A screen shot of the *Signal Wizard* filter design program.

receive dynamic range of 100 dB. In both cases, please note that the received audio is restricted to a 300 to 3000 Hz band as indicated by the noise pedestal. Also, there is no evidence of unwanted audio artifacts in the headphone audio output. For this testing, headphone gain was set to 0 dB.

Likewise, a series of tests were run over the same range of input signals with AGC applied and without AGC applied. In the cases where AGC was not applied, the receiver gain was held at 0, 20 and 48 dB. The results of this testing are shown in Figure 10. The point charts show responses without AGC while the single line chart shows receiver response with AGC applied.

Unwanted Receive Signal Rejection

The screen shot in Figure 11 demonstrates the receiver unwanted signal rejection. The DSP algorithm was placed in a test mode where the undesired signal was routed to the left headphone output and the desired signal was routed to the right headphone output. The unwanted signal rejection shown approaches 70 dB. To achieve this degree of rejection, however, the DSP software must account for the amplitude and phase shift imbalance inherent with each individual SoftRock. Although the SoftRock imbalances are on the order of 0.01 to 0.1 dB and 1 to 2 degree, they are enough to limit non-compensated signal rejection to 30 dB or so.

The software compensates for amplitude by simply multiplying the I receive audio channel by 0.85 and then multiplying the Q audio channel by a fraction that may be set between 0.5 and 0.999. Phase shift compensation is a little trickier. To compensate for phase shift a small fraction of the Q signal is added to the I signal. This technique may be used with good results to compensate for phase shift imbalance between – 5 degree to +5 degree.

The SDR2GO software allows the user to use a separate rotary encoder to adjust both receive IQ amplitude balance and IQ phase

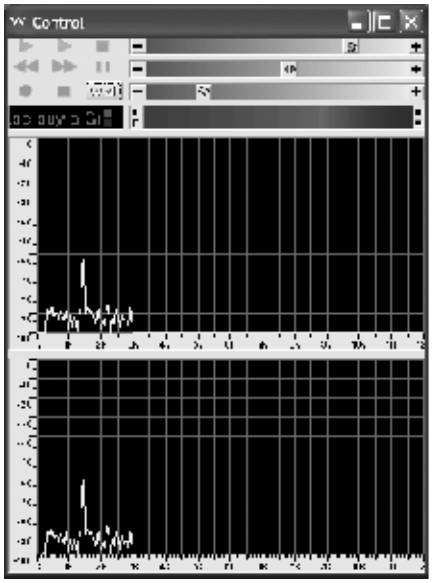

Figure 8 — Spectrum of the audio output with –110dBm input.

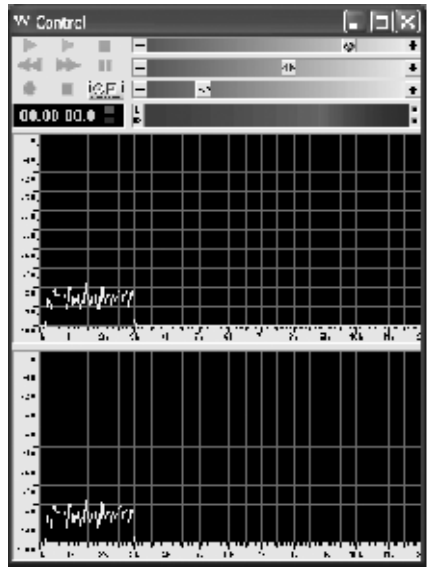

Figure 9 — Spectrum of the audio output with –130dBm input.

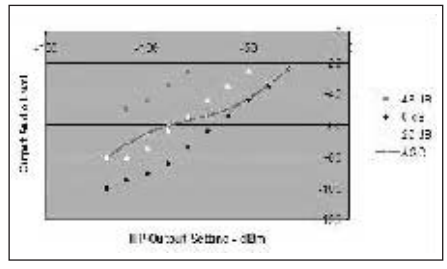

Figure 10 – Plots of the receiver response with AGC

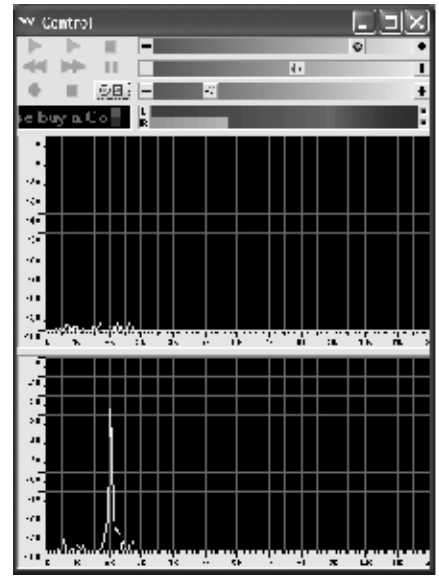

Figure 11 – Plots of unwanted signal suppression. The top waveform is the opposite sideband and the bottom is the desired sideband audio output.

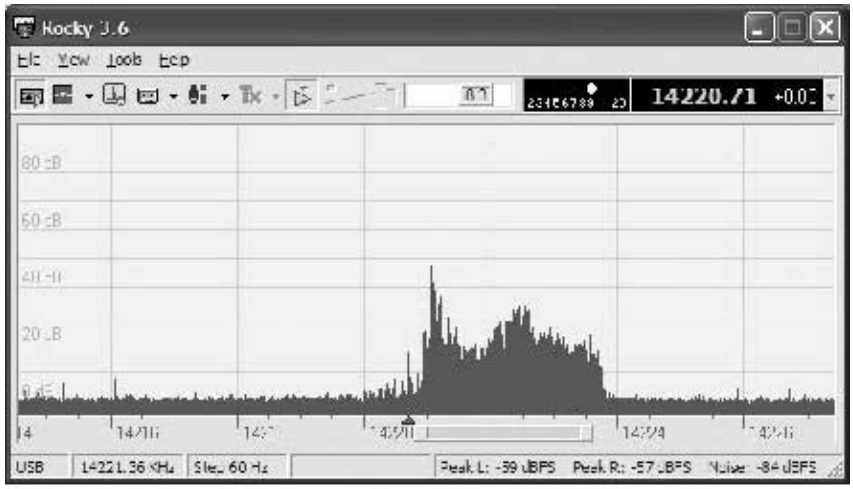

Figure 12 – Spectrum display of the transmitter using a second SoftRock running the Rocky program.

shift. Switch inputs are provided so that the encoder controls either the amplitude fraction or the phase fraction. Further, the software monitors the receive/transmit mode of operation so that a set of receive parameters may be set as well as a set of transmit parameters.

Transmit Performance

Transmitter performance was evaluated using a separate SoftRock RXTX and the same 24 bit Soundcard referenced above. In this case, Rocky Version 3.6 was used as the software application for signal processing and display. The transmit performance with voice SSB modulation is shown in Figure 12. The transmit frequency is 14220.71 kHz and the mode is upper sideband.

Input Current Draw

The input current draw measurements were made with 13.8 V dc applied:

Receive Current Draw	200 mADC
Transmit Current Draw without modulation	300 mADC
Transmit Current Draw at 1 W RF output	400 mADC

Building Your Own SDR2GO Board

There are several advantages to building a DSP project and there is a disadvantage. We have found that by using the dsPIC, Si570 technology plus the SH32 control processor that very repeatable results are achieved. So far, two of the SDR2GO boards have been completed and packaged. The physical layouts of these two packages are significantly different, but the results are identical. Only a few changes of cable routing and board grounding were required to achieve the performance reported above.

The disadvantage is obviously the requirement to use surface mount devices. I suspect that most amateurs are as frightened of mounting SMD devices as I was several years ago. However, over time I collected a number of simple tools and developed skills that make SMD doable. The other group members have had the same experience. I have become convinced that if you want to continue building using currently available devices you will inevitably have to contend with SMD devices. So, the next installment of this article will cover SMD construction using hand soldering in detail.

Other than the SMD issue there are not any major hurdles to building the SDR2GO kit. The board has legible labels and all parts will be provided. The dsPIC and SH32 processor will have their respective applications already programmed so there is no need to purchase programming interfaces. The board schematics plus building notes will be available on the AQRP Web site.

The only equipment required for testing is a voltmeter and a PC with one Soundcard to check audio levels. The later will make setting amplitude and phase parameters quite easy.

I hope we have hooked you into building an SDR2GO kit!

Notes

[1]Please see Kees' website at **www.qsl.net/k5bcq/Kits/Kits.html**.

[2]Builder's notes and latest SDR2GO program code are in the SDR2O Archive at **groups.yahoo.comgroup/AQRP/files/SDR2GO%20Archive/**.

Charley Hill has been licensed as W5BAA since 1959. He graduated from University of Houston in 1968 with a BSEE and is a registered professional engineer in the State of Texas. He served with the 409th Radio Research Detachment in Viet Nam. He worked for Brown & Root/Halliburton for 35 years specializing in automation, telecommunications and petroleum engineering. Besides ham radio he is active in building and flying free flight model airplanes and full-scale glider flying.

QEX

Maynard Wright, W6PAP

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Octave for L-Networks

Maynard provides another installment in his series of tutorials on the use of the free Octave mathematics program.

Overview of L networks

When we build reactive networks to match impedances for various reasons, we are stuck with using lossy inductors and capacitors in the implementation, even if we ignore the losses while designing the network. For that reason, among others, the L-network is popular as it minimizes the number of required elements to match impedances over a wide range of values.

The use of the L-network as an antenna tuner is described on pages 25-6 and 25-7 of *The ARRL Antenna Book*.[1] Some design methods are presented there and also in *The ARRL Handbook*. [2] These methods have been around for a long time and are described in a slightly different form by Frederick Terman.[3]

These design methods, though, assume that the impedances to be matched are resistive. When we deal with antennas that require impedance matching, the reactive component is often much larger than the resistive component of impedance, especially for short mobile or portable antennas.

As noted in *The ARRL Antenna Book*, it's possible to include the reactive portions of the source and/or load impedances in the reactive elements of the L-network. This may, though, be a little cumbersome when we must combine a paralleled network reactance with a series source or load reactance and when the source and/or load reactances are considerably larger than the corresponding resistive components.

Using Octave for calculations

We'll use GNU Octave to design an L-network for which both the source and/or load impedances can be either real or complex. We could do this by using the circle diagram,[4,5] but it will be simpler to write some Octave code to synthesize the network directly. In addition, we'll be able to obtain more precision from our Octave code than we can by using graphical methods. We'll use the conventions in Figure 1 for labeling the components of our network. We've used inductors for the series reactive elements and capacitors for the shunt elements in Figure 1, but this is purely arbitrary at this point. Several different geometries for L-networks that use a variety of combinations of inductors and capacitors are shown on page 5.25 of *The ARRL Handbook*. In order to design the L-network, we could write current loop equations using Kirchhoff's Voltage Law as we did in "More Octave for Transmission Lines".[6] We'll take a different approach here, though, because it will help us to understand some of the benefits and limitations of the L-network.

We'll first calculate the impedance of the network looking to the right toward *jxnp* and *rt + jxt*, leaving out for the present *jxns* and the source elements.[7] We calculate that impedance as:

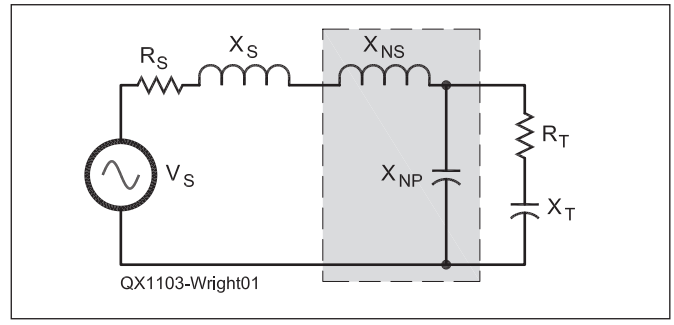

Figure 1 — L-Network

$$r1 + jx1 = (rt + jxt) * jxnp / (rt + jxt + jxnp) \quad [1]$$

Since the series arm that we'll add later can't adjust the value of *r1*, we'll set *r1* equal to *rs*, the resistive value of the source impedance and solve for values of *jxnp* and *jx1*, the two unknowns, that will produce that value of *r1*.

Note that we have two unknowns, *jxnp* and *jx1*, in one equation here. Well, not exactly: when we eliminate the parentheses and the denominator by multiplying terms, we end up with an equation with both real (resistive) and imaginary (reactive) terms. The sum of all the real terms on one side of the equation must equal the sum of the real terms on the other side and likewise for the imaginary terms. We can therefore separate our single equation into two, one of which contains only real terms and one of which contains only imaginary terms. We can also divide each term in the imaginary equation by *j*, the imaginary operator, to simplify that equation.

Once we've done this, we have two equations in two unknowns, *x1* and *xnp*. We could use determinants to solve the simultaneous equations as we did in "More Octave for Transmission Lines," but it will be easier here to solve the imaginary equation for *x1* and substitute it out of the real equation so that the only unknown there is *xnp*. When we've done that, we'll find that we have a quadratic equation in *xnp*, with the form:

$$ax \wedge 2 + bx + c = 0 \quad [2]$$

where

$a = rs - rt$

$b = 2 * rs * xt$

$c = rs * rt \wedge 2 + rs * xt \wedge 2$

We'll use the quadratic formula to solve this equation. Since the equation is quadratic, we'll find that there are two real[8] solutions for

[1]Notes appear on page 46.

xnp and we'll calculate them separately in our Octave script. We'll use the quadratic formula[9]:

*xnp = (-b +/- sqrt(b^2 - 4 * a * c)) / (2 * a)* [3]

where *a*, *b*, and *c* are as defined above.

Although most references state that the lower of the two impedances to be matched must be connected to the series-arm side of the L-network[1], this is true only when we want to build the network using only reactive elements and when both the source and the load are resistive. If we allow positive resistances (resistors) or negative resistances (synthesized using op amps) in series with our L-network elements, we can match a wider range of impedances without so much concern about the orientation of the network. Since we probably don't want to do that in any common amateur radio application, we'll disallow such solutions by flagging an error and printing a diagnostic message when such a solution would result. That will happen when the quantity under the radical in equation 2 is negative. We can keep it positive by ensuring that:

*0 < rt^2 + xt^2 - rs * rt* [4]

When the source and load are resistive, xt drops out and equation 4 reduces to:

0 < rt - rs [5]

This is equivalent to saying that the impedance connected to the series arm, for the L-network geometry in Figure 1, must be the lower of the two as most references require.

Each of the two solutions to the quadratic equation will produce an *r1* that equals *rs*, so that the resistive portion of the match we're after is accomplished. We'll then solve the reactive equation for *x1*. We'll use *x1* to determine *xns*, the series arm of the L-network, to satisfy the matching requirement for *xs*:

xns = xs - x1 [6]

Our Octave script is listed in Table 1. Comments have been omitted from the listing as they are covered in the text of this article. We could add an extra input statement to accept a frequency of interest and then calculate the capacitance or inductance that would yield the series and parallel reactances for that particular frequency, but that's omitted from the code in Table 1 for simplicity.

We'll try our code by solving the problem on pages 148 through 152 of Griffith. In this antenna coupling network problem, we have the following conditions:

rs = 230 ohms
xs = 0
rt = 16 ohms
xt = -96 ohms

When we run the script, we get the following outputs, the numbers being in units of ohms reactance:

*** FIRST OPTION ***
SERIES ELEMENT REACTANCE = 288.548
PARALLEL ELEMENT REACTANCE = 124.751
*** SECOND OPTION ***
SERIES ELEMENT REACTANCE = -288.548
PARALLEL ELEMENT REACTANCE = 81.6039

Except for some slight differences in the less significant figures, these results agree with those shown in Figure 19.4 of Griffith.

Now let's try something different. We'll reverse the two sides and use the L-network "backwards." We are led to try this by noting that the larger of the two impedances in Griffith's example is connected to the series arm of the L-network. That would be a violation of the rule to positioning the L-network if the source and load were resistive. We'll reverse the network by swapping the source and load impedances:

rs = 16 ohms
xs = -96 ohms
rt = 230 ohms
xt = 0 ohms

Table 1

```
#!/usr/bin/octave
rs = input("\n\n              ENTER SOURCE RESISTANCE: ");
xs = input("               ENTER SOURCE REACTANCE: ");
rt = input("   ENTER TERMINATING RESISTANCE: ");
xt = input("   ENTER TERMINATING REACTANCE: ");
a = rs - rt;
b = 2 * rs * xt;
c = rs * rt ^ 2 + rs * xt ^ 2;
if ((b ^ 2 - 4 * a * c) < 0)
   printf("\n  CONFIGURATION OF L-NETWORK INVALID\
 FOR SPECIFIED IMPEDANCES: TRY REVERSING\
 THE NETWORK.\n\n");
else
   xnp = (-b + sqrt(b ^ 2 - 4 * a * c)) / (2 * a);
   zn = (1j * xnp * (rt + 1j * xt)) / (1j * xnp + rt + 1j * xt);
   xns = -imag(zn);
   printf("\n\n         *** FIRST OPTION ***");
   printf("\n    SERIES ELEMENT REACTANCE = %g", (xns + xs));
   printf("  PARALLEL ELEMENT REACTANCE = %g", xnp);
   xnp = (-b - sqrt(b ^ 2 - 4 * a * c)) / (2 * a);
   zn = (1j * xnp * (rt + 1j * xt)) / (1j * xnp + rt + 1j * xt);
   xns = -imag(zn);
   printf("\n\n        *** SECOND OPTION ***");
   printf("\n    SERIES ELEMENT REACTANCE = %g", (xns + xs));
   printf("  PARALLEL ELEMENT REACTANCE = %g", xnp);
   printf("\n\n");
endif
```

When we do this, we get

*** FIRST OPTION ***

SERIES ELEMENT REACTANCE = -37.485

PARALLEL ELEMENT REACTANCE = -62.8899

*** SECOND OPTION ***

SERIES ELEMENT REACTANCE = -154.515

PARALLEL ELEMENT REACTANCE = 62.8899

Here we've reversed an L-network and we've been able to achieve a match in either direction, with different values in each case, of course. This is because of the non-zero value of *xt* in equation 4. With *xt* considerably higher in magnitude than *rt*, as is often the case for short antennas, we can match over a fairly wide range of impedances with the shunt reactance situated in either direction, unlike the case when the source and load are both resistive.

Griffith discusses this matter in terms of the locus of a circle diagram. He points out that we can use an L-network to match his terminating impedance to a source resistance of from 0 to 590 ohms. We can check this by substituting values for our source and load into equation 4:

$0 < rt \wedge 2 + xt \wedge 2 - rs * rt$ [4]

$0 < 16 \wedge 2 + (-96 \wedge 2) - rs * 16$

$0 < 256 + 9216 - 16 * rs$

$0 < 591.375 - rs$

$rs < 591.375$

Since Griffith is using a graphical technique to obtain the 590 ohm limit, this is good agreement.[10]

We see that we can use an L-network to match complex impedances with a bit more latitude toward the positioning of the network than is the case when the source and load are both resistive.

We also used the definition of the quadratic formula to advantage. We solved for *a*, *b*, and *c* and plugged them directly into the formula in the Octave code. Expanding the formula by substituting all the values from our quadratic equation in *xnp* into the formula would have led to a longer, more complicated expression in Octave code that would have been more prone to error while setting up and coding the equation.

Maynard Wright, W6PAP, was first licensed in 1957 as WN6PAP. He holds an FCC General Radiotelephone Operator's License with Ship Radar Endorsement, is a Registered Professional Electrical Engineer in California, and is a Life Senior Member of IEEE. Maynard has been involved in the telecommunications industry for over 45 years. He has served as technical editor of several telecommunications standards and holds several patents. He is a Past Chairman of the Sacramento Section of IEEE. Maynard is Secretary/Treasurer and Past President of the North Hills Radio Club in Sacramento, California.

NOTES:

[1] *The ARRL Antenna Book,* 21st Edition, The American Radio Relay League, 2007, pages 25-6 and 25-7

[2] T*he ARRL Handbook for Radio Communications*, 2011, The American Radio Relay League, Inc. 2010, Sections 5.6.1 and 20.4.2

[3] Frederick E. Terman, *Radio Engineers' Handbook*, McGraw-Hill, 1943, page 209

[4] M. Wright, "Octave for Circle Diagrams," *QEX*, Sept/Oct, 2007

[5] B. Whitfield Griffith, Jr., *Radio-Electronic Transmission Fundamentals,* McGraw-Hill, 1962: reprint available from ARRL at www.arrl.org.

[6] M. Wright, "More Octave for Transmission Lines," *QEX*, Jan/Feb, 2008

[7] We'll add the resistive and reactive components of impedance here using a "+" sign. If the reactance is negative (capacitive) in sign, we'll take care of that when we input the data to our Octave script.

[8] The reactance of the paralleled element is *jxnp*, where the *j* (imaginary) operator denotes the ninety degree phase shift between voltage and current that is characteristic of reactive circuit elements. We're solving here for *xnp*, the magnitude of *jxnp*.

[9] *CRC Mathematical Tables*, 21st Edition, CRC Press, 1973, page 103

[10] As a slide rule and Smith Chart enthusiast, I don't want to discourage the use of graphical methods. They can be very useful in visualizing a problem and can often yield useful results that are sufficiently precise for practical purposes.

QEX

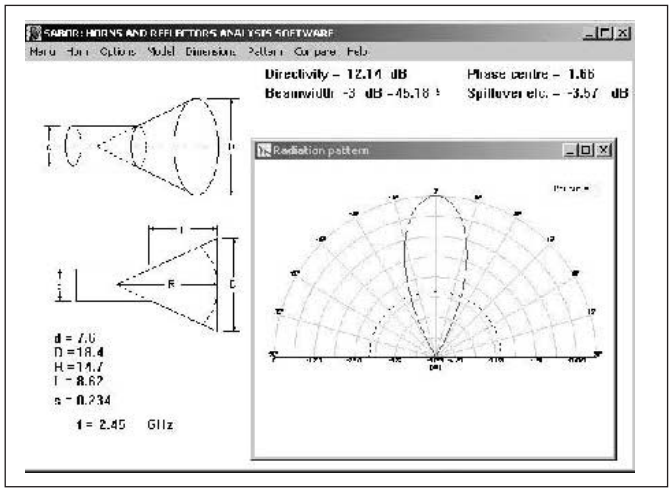

Figure 21 — Polar Plot of the radiation pattern from the *SABOR* program.

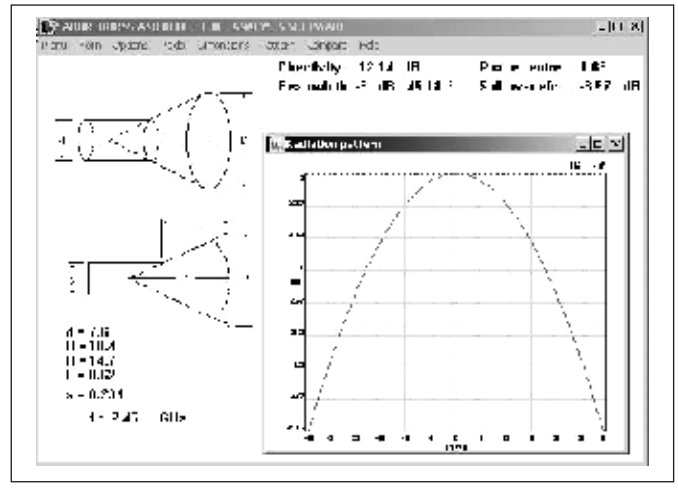

Figure 22 — SABOR X-Y Plot of the pattern. Gain is 12.14 db and the 3 db beam width is 45 degrees.

OPTIONS. The drop down menu will show frequency on top. Click on FREQUENCY and enter the operating frequency. In our example, the author chose 2.45 GHz. Move over on the top menu to DIMENSIONS. Several parameters are requested but we have already determined two of the three. *SABOR* asks for Wave-g, Horn radius and a radius value for R1. Knowing our example hood dimensions, D1 = 76 mm, D = 184 mm, will be all that is necessary to utilize *SABOR*.

Wave-g is half the cylinder diameter (d = 76 mm). In our case, 76 mm/2 = 38 mm or 3.8 cm. Horn Radius is half of the hood diameter (D = 184 mm) and in our case 184/2 = 92 mm or 9.2 cm. R1 is found by D/1.25, so it is 184/1.25 = 147 mm or 14.7 cm. Enter waveg = 3.8 cm. (Refer to the left side of Figure 21 to see these values in *SABOR*.) Given this information, the pattern and gain figures can now be calculated. Move back to the OPTIONS drop down menu and click AUTOMATIC and xy. Now move to the PATTERN icon and click. This is the X-Y plot of your antenna. The gain for our example is over 12 db and the beam width is 45 degrees. To see a polar plot of your antenna, go back to the OPTIONS drop down menu and click POLAR. The display will now change to the familiar directional pattern. (See Figures 21 and 22.)

Applications.

This antenna is currently in use to link the author's radio shack with the home, a distance of 600 feet. A pair of these horn antennas can easily link data services using 10 mW access points. The antenna can be used for any 2.4 GHz point to point communication. A 1W Amateur television signal has been sent over a pair of these horn antennas at a distance of six miles with good A5 results.

Table 1

Standard Type L Copper Pipe Dimensions (Inches)

Nominal Size	*Actual Dimensions*	
Inside Diameter	*Outside Diameter*	*Wall Thickness*
¼	0.375	0.035
⅜	0.50	0.049
½	0.625	0.049
⅝	0.750	0.049
¾	0.875	0.065
1	1.125	0.065
1¼	1.375	0.065
1½	1.625	0.072
2	2.125	0.083
2½	2.625	0.095
3	3.125	0.109
3½	3.625	0.120
4	4.125	0.134
5	5.125	0.160
6	6.125	0.192
8	8.125	0.271

This horn antenna could be utilized to illuminate a dish antenna. Polarization is a function of the direction of the probe. Up and down is vertical and 90 degrees to that is horizontal. Your imagination is the limiting factor in applications for this antenna.

Here are dimensions for a 2.40 GHz version of this horn antenna using a 76 mm diameter copper pipe. The cut off frequencies remain the same since the diameter is 76 mm.

Design Frequency is 2.40 GHz
¼ = 125 mm
Lg = 470 mm
Cylinder length = 352 mm
Probe distance from closed end = 118 mm
Probe depth = 31 mm
Hood dimensions D = 188 mm, D1 = 78 mm

There are potential designs for 5 GHz utilizing 38 mm (1.5 inch) diameter copper pipe and 3.4 GHz using 2 inch diameter pipe. Let's experiment. You get a lot of gain for a small amount of effort and the horn antenna is very directional with a clean pattern. To aid in the hunt for copper tubing, Table 1 shows typical ID and OD sizes for commercial plumbing pipe.

The author would like to express his gratitude to Dustin Larson who fabricated prototypes of this antenna during the development and testing phases and Jeremy Vogel for his assistance in the graphing programs.

Notes

[1]John Kraus, *Antennas*, McGraw-Hill, 1988, pp 644-653.
[2]Gershon Wheeler, *Introduction to Microwaves*, Prentice-Hall, 1963, pp 60-63.
[3,4]Jessop, G. R., *VHF-UHF Manual*, 4th edition, Radio Society of Great Britain, 1985, p 9.27.
[5]Barter, Andy, *International Microwave Handbook*, Radio Society of Great Britain, 2002, p 58.
[6]Norm Foot, "Cylindrical Feed Horn," *Ham Radio*, May 1976, p18.
[7]Richard Kolbly, "Low Cost Microwave Antenna," *Ham Radio*, November 1969, p 52.

Photos by the author

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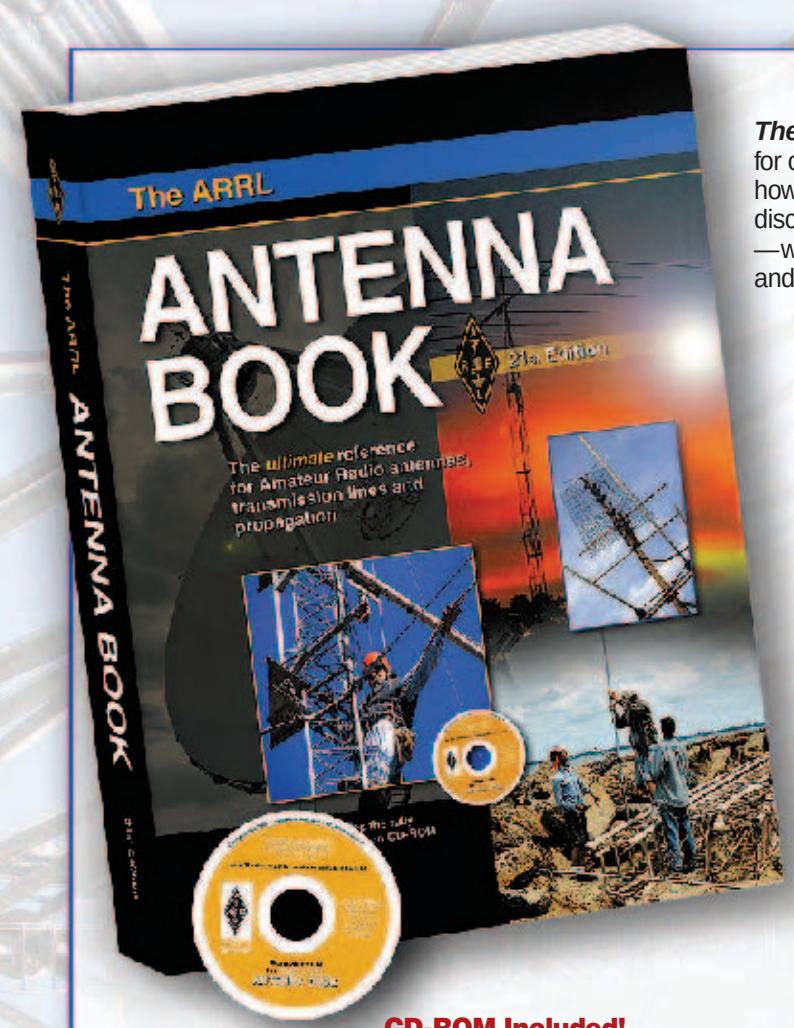

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