



QEX

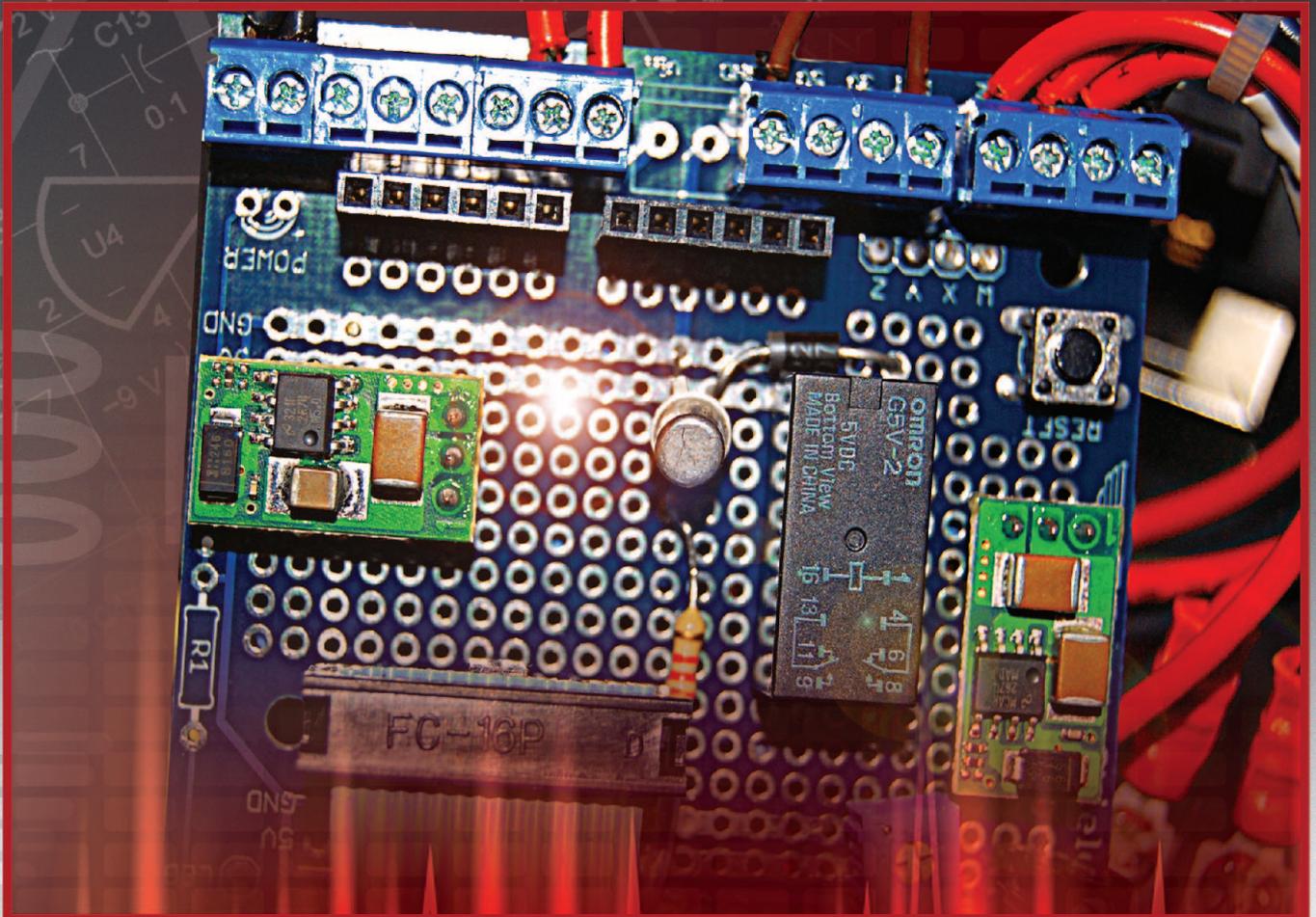
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A Forum for Communications Experimenters

Issue No. 289



W5HEU used this Adafruit Proto-Screwshield prototyping board and an Arduino Uno processor to add voltage and current readout and overcurrent protection to his autotransformer variable voltage ac supply. This would be a handy addition to just about any workbench.

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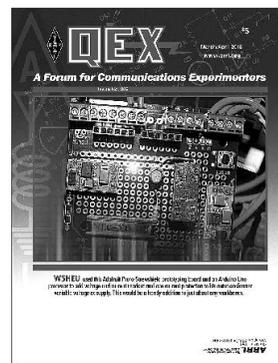
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About the Cover

Ted Drell, W5HEU, matched an old-time workbench standby with the latest microprocessor control — an autotransformer and an Arduino Uno processor and Proto-Screwshield prototyping board — to create a variable voltage ac supply with voltage and current readout as well as overcurrent protection; a handy addition to just about any workbench.



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The purpose of QEX is to:

- 1) provide a medium for the exchange of ideas and information among Amateur Radio experimenters,
- 2) document advanced technical work in the Amateur Radio field, and
- 3) support efforts to advance the state of the Amateur Radio art.

All correspondence concerning *QEX* should be addressed to the American Radio Relay League, 225 Main Street, Newington, CT 06111 USA. Envelopes containing manuscripts and letters for publication in *QEX* should be marked Editor, *QEX*.

Both theoretical and practical technical articles are welcomed. Manuscripts should be submitted in word-processor format, if possible. We can redraw any figures as long as their content is clear. Photos should be glossy, color or black-and-white prints of at least the size they are to appear in *QEX* or high-resolution digital images (300 dots per inch or higher at the printed size). Further information for authors can be found on the Web at www.arrl.org/qex/ or by e-mail to qex@arrl.org.

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Larry Wolfgang, WR1B

Empirical Outlook

Warm Weather Plans

It seems especially difficult to imagine warmer weather and starting to work on antenna projects as I write this editorial. Here in the Northeast US, we are in the midst of one of the coldest and snowiest winters in recent memory. The forecast for tomorrow is record-breaking-cold low temperatures. The snow has been piling up for weeks, with little chance for any melting. I haven't even seen any signs of sublimation, which should start to be evident by this time of year. Maple farmers will soon be lamenting the fact that temperatures have not been rising to the upper 30s or warmer, as needed for the maple sap to begin flowing. That normally happens by early February.

A few evenings ago I overheard a conversation on a local 2 meter repeater, though. Two hams were talking excitedly about their antenna plans, "as soon as I can get into the back yard." One talked about a wire antenna with an end that had fallen, either because of a broken tree branch or a broken support rope. He was still using the antenna to make some contacts, but it was definitely compromised. The snow was piled too deep, and he was unable to get to the antenna to string it up again. The other operator was also talking about some antenna work he wanted to begin as soon as he could get outside into his yard as well. He was planning a change to one of his antennas, and was anxious to see how much the performance would be improved.

I smiled, because I also have some antenna work to do, and almost had started on it before the snow started piling up. There are a couple of tree limbs (or whole trees) that need to come down, in one case partly because the limbs are starting to hang over the house roof and dropping leaves and pieces of dead limbs on the roof, and partly to make room for an improved 160/80 meter wire antenna. In another case, a tree that was much shorter and farther from my tower when I first put that up has now grown to the point that when the leaves are on the tree, a couple of limbs reach the ends of the Yagi elements when I try to turn the antenna through its full range. We like nice tall, strong trees to serve as antenna supports, but sometimes those same properties can cause problems. I definitely need to trim these trees before the leaves are fully grown this spring, but this winter has not been the best time to attempt such work.

How about you? Have you been dreaming about your next antenna project? Perhaps standing at a window, looking longingly at your antenna farm, and thinking about what changes you want to make. Maybe you live in a warmer climate and are able to get outside and start working on those projects now. In any case, if you are an active, on-the-air ham, you are probably thinking about some changes to your antennas. We all know that the single most effective improvement we can make to our station is to our antenna system.

This issue brings you a couple of antenna articles that may help spark some ideas for you to try. Al Christman, K3LC, describes some "Wire Antennas for 80 Meter DXing." While you may not have a 180 foot tower just waiting to support a few more wires, Al presents some interesting wire configurations. If you scale one or more of these ideas for a higher frequency band you won't need as much height, so they may become more practical for your antenna farm.

You might find "A Triband Dipole for 30, 17, and 12 Meters" by Zack Lau, W1VT, to be more practical for your station. We have had access to these bands for long enough that we have stopped calling them "WARC Bands" or even "the new bands." Just about every Amateur Radio operator with an HF radio can at least listen on the 30, 17 and 12 meter bands. There is a lot of activity, and some great DX to be had. Yet I know plenty of General and Extra Class operators who either don't have an antenna for any of those frequencies, or who are using an antenna cut for other bands, with an antenna tuner. That works, but here is an idea for an antenna built specifically for these bands. If all you have is a "classic" triband Yagi, Zack has something to try.

Antenna articles are always popular, so if you have other ideas or an innovative antenna project, consider sharing it with your fellow *QEX* readers.

While we wait out the rest of this winter season, I hope you stay warm and find some Amateur Radio projects to work on, and some operating time to enjoy the many aspects of our hobby. If you spent some time over the last few months developing a new project or accessory for your shack, how about sharing that with our readers as well? We are always happy to hear from readers, and learn about those projects that interest you.

An Experimenter's Variable Voltage Transformer

Here is a modern twist to controlling an old workbench essential.

I am an old antique radio buff, and as anyone playing with such old toys as these will tell you, you must have a variable voltage transformer (autotransformer) to work on them. (One brand name of such an autotransformer is Variac.) I had one that I put together from excess parts; a “Bud” box, a panel mounted autotransformer, fuse holder, switch, and a panel mounted AC receptacle. This was a neat unit that would handle 3 A and fit nicely on my workbench. It did a good job until it was overloaded and I let the smoke out. The problem was that there was no way to monitor the voltage and current without using external meters and that was messy. Oh well. I needed to add meters to the unit, but panel space was at a premium so the unit sat there with the top off taking up space.

Then along came the May 2013 issue of *QST* and the article on page 39 touting the merits of the Arduino Uno processor. I immediately ordered two of these little guys to play with. I got the complete experimenters kit with prototype board, LCD display, and so on. It did not take long to realize that this could be the answer I've been looking to use for a number of projects. I have several going on in parallel, but one is now finished. It is an instrumented version of my Autotransformer, and the details follow.

The Circuit

The May 2013 article in *QST* gives the basics to get started with the Arduino, and there are books from ARRL as well as lots of free stuff on the Internet that will give you most of what you need for the Arduino itself,

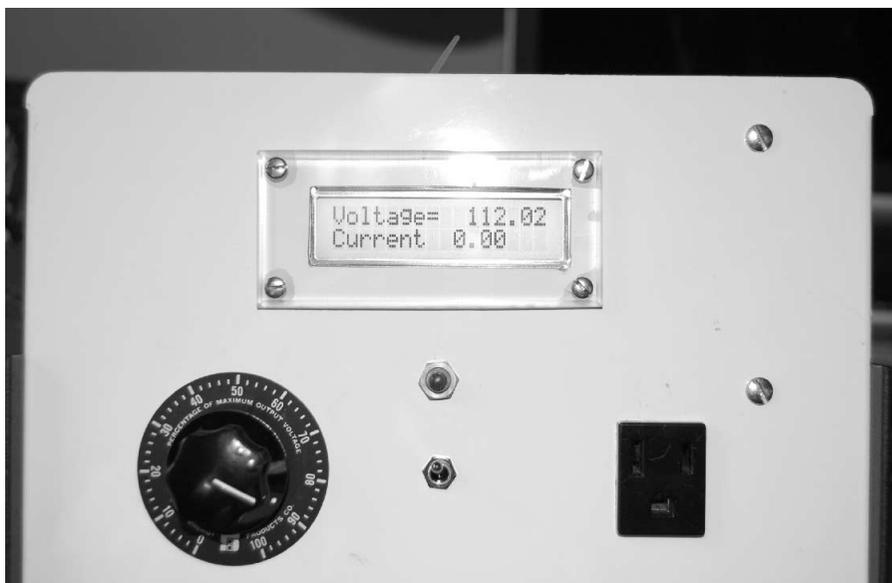


Figure 1 — Front panel layout.

so I won't take up space with that. It became obvious that I need some sort of interface for the processor. More searching revealed multiple prototype “shields” available in the range of \$15.00 to \$25.00. I chose the Proto-Screwshield (Wingshield) kit from Adafruit (\$16.00) because it has screw type terminal blocks for all of the Arduino connections and a large prototyping area.

The first interface was to the LCD readout. For that, I used a dual row, 8 pins per row header. The LCD also has a dual row header, so a 16 conductor ribbon cable with IDC connectors was used to connect the proto board to the LCD. The only component needed for the LCD was the contrast potentiometer.

All that was needed to complete the project was a voltage and current transducer and the project was done. I think my “junk box” is better than the average ham's, because I design and build a lot of small portable test systems. I had a current transducer that was self excited and would output 0 to 5 V DC for 0 to 10 A. Since the autotransformer was a 3 A unit, two turns of wire through the current transducer made it 0 to 5 V DC for 0 to 5 A. No scaling is necessary because the Arduino analog input is 0 to 5 V DC; Perfect! The voltage transducer is also self excited and puts out 0 to 5 V DC for 0 to 600 V AC input. I multiplied the 5 V output by 120 in the software and I now read line voltage perfectly.

¹The author's software code for the Arduino is available for download from the ARRL QEX files web page. Go to www.arrl.org/qexfiles and look for the file **3x13_Drell.zip**.

Table 1**Software Code Listing for the Arduino**

```
/* Variac Voltage and Current Monitor
   Set for a 24x2 LCD display.
   The circuit:
   * LCD RS pin to digital pin 7
   * LCD Enable pin to digital pin 6
   * LCD D4 pin to digital pin 5
   * LCD D5 pin to digital pin 4
   * LCD D6 pin to digital pin 3
   * LCD D7 pin to digital pin 2
   * LCD R/W pin to ground
   * 10K resistor:
   * ends to +5V and ground
   * wiper to LCD VO pin (pin 3)
   Library originally added 18 Apr 2008 by David A. Mellis  library modified 5 Jul 2009
   by Limor Fried (http://www.ladyada.net)
   */

// include the library code:
#include <LiquidCrystal.h>
//#include <OneWire.h>
//#include <DallasTemperature.h>

// initialize the library with the numbers of the interface pins
LiquidCrystal lcd(7, 6, 5, 4, 3, 2);

//const int busPin = 10;
//OneWire bus(busPin);
//DallasTemperature sensors (&bus);
//DeviceAddress sensor;

int voltage=A0; // select the input pin for the voltage sensor
int currentI=A1; // select the input pin for the current sensor #1

int voltageValue = 0; // variable to store the value coming from the voltage sensor
int currentIValue = 0; // variable to store the value coming from the current sensor #1

float curtrip = 3.00;
int ledPin = 9;
int relayPin = 8;

void setup() {

//  pinMode(busPin, INPUT);
//  sensors.begin();
//  sensors.getAddress(sensor, 0);

  pinMode(ledPin, OUTPUT);
  pinMode(relayPin, OUTPUT);
  // set up the LCD's number of columns and rows:
  lcd.begin(24, 2); // initialize the lcd
  lcd.clear(); // clear lcd
  lcd.setCursor(3,0);
  lcd.print("TDA LLC");
  lcd.setCursor(1,1);
  lcd.print("Variac Monitor");
```

```

digitalWrite(ledPin, LOW);
digitalWrite (relayPin, LOW);

delay(3000);

}

void loop() {

// sensors.requestTemperatures();

// float tempF = sensors.getTempF(sensor);

voltageValue = analogRead(voltage);
current1Value = analogRead(current1);

float vol = (voltageValue * (5.00/1023.0))*30;
float curl = current1Value * (5.00/1023.0);

// set the cursor to column 0, line 0

if (curl < curtrip){

digitalWrite(ledPin, LOW);
digitalWrite (relayPin, HIGH);
lcd.clear();
// read and display the voltage
lcd.setCursor(0,0);
lcd.print("Vol=");
lcd.setCursor(5,0);
lcd.print(vol);

// lcd.setCursor(13,0);
// lcd.print("Temp=");
// lcd.setCursor(19,0);
// lcd.print(tempF);

// read and display the current
lcd.setCursor(0, 1);
lcd.print("Cur=");
lcd.setCursor(7, 1);
lcd.print(curl);

delay(500);

}
else{
while(1){
digitalWrite(ledPin, HIGH);
digitalWrite(relayPin, LOW);
lcd.clear();
lcd.setCursor(0,0);
lcd.print("Tripped Over Cur");
lcd.setCursor(0,1);
lcd.print("Press Reset");
delay(1000);
}
}
}
}

```

Since I smoked the first autotransformer, I wanted over-current protection. With a microprocessor now working, adding a little software to protect the unit was no problem. I did have to add a transistor driver and a relay for this to work. The software allows the unit to operate until the current reaches 3.0 A, at which point it disconnects the power, thereby protecting the autotransformer from overload. Once the system is tripped, you have to manually reset it. When tripped, the LCD display says “Tripped on over current; Press reset.” If the overload is removed, the system will reset and resume operation.

The low current relay on the prototype board was not large enough to switch line voltage, so I used an external relay. I had an open frame power supply that I used to power the Arduino and relays. Since the recommended power for the Arduino

is nominally 12 V DC, I used a neat little DC-DC converter from Murata. It does not get hot and is small so that it fits on the proto board with no heat sink needed. Rounding it out, I included an LED to provide trip indication if desired.

A complete parts list is included as a guide. My sensors are expensive and cheaper ones are available. This article is intended to show the flexibility of the processor and how I applied it. With a little software modification, it can do a multitude of things.

Figure 1 shows the completed project, with the main display showing the adjusted voltage as well as the current. The LCD display is a 24 × 2 (or 2 × 24) which means there are 2 lines each with 24 characters. This limits the dialog. Other displays can be used if defined in the software. I also have another project where I can select multiple pages to

display by switch selection, so anything is possible.

Figure 2 is the wiring of the protoshield and Figure 3 is the wiring of the autotransformer.

The software is available for download from the ARRL QEX files web page.¹ It is open source so you are free to use it as is, or change it to suit your needs. The language is basically C++ so anyone familiar with C++ will not have any problems using it. The programming guides and libraries are available for free download from the Arduino web site.

The software was originally written for another project and had the ability to add the Dallas Semiconductor “One Wire” temperature sensor. Since this was not used in this project, the code for this is commented out.

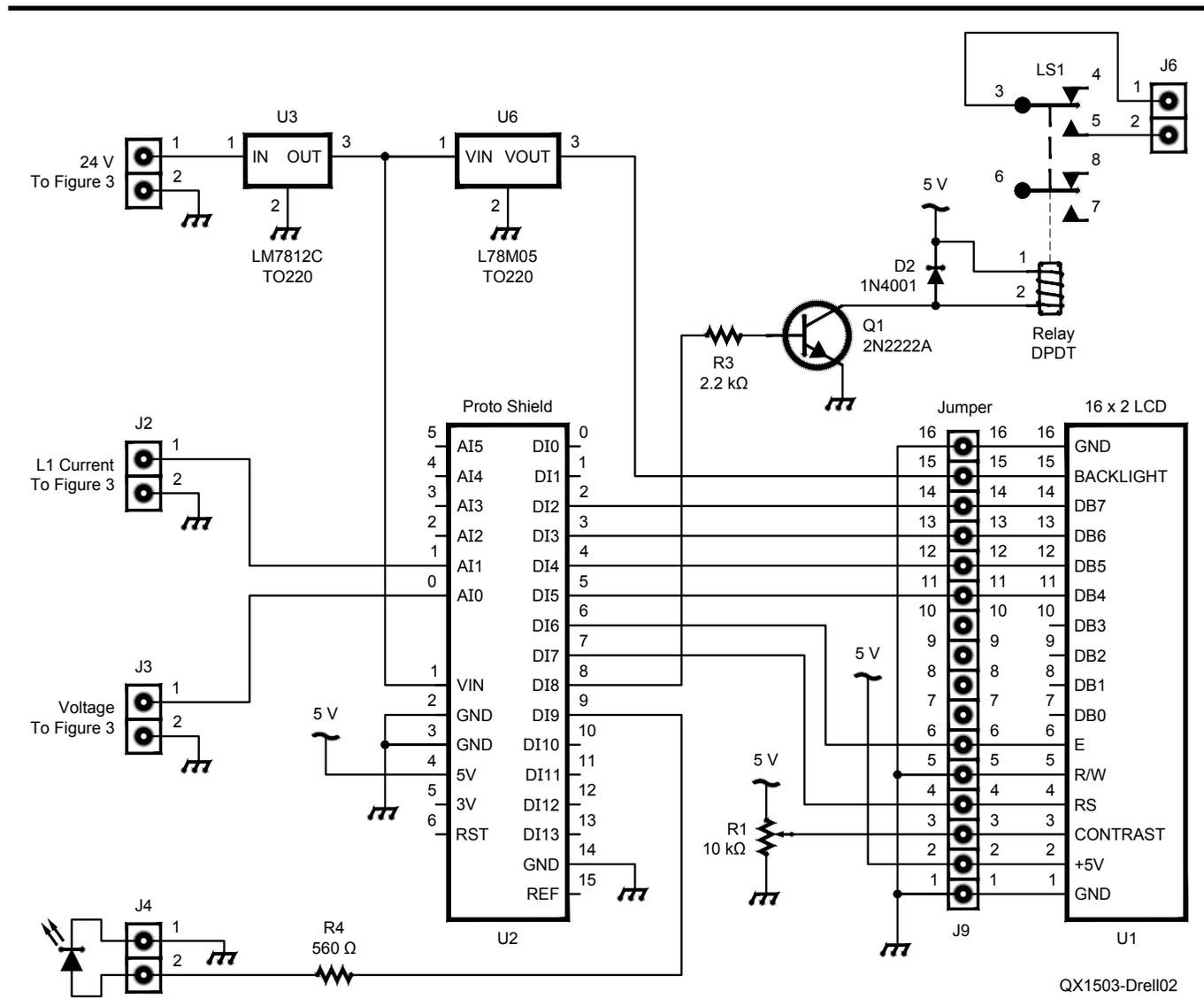


Figure 2 — The schematic diagram of the Arduino protoshield.

Construction

The unit is assembled in a standard Bud cabinet with components placed as shown in Figure 4. The only critical wiring was the routing of the ribbon cable from the protoshield to the LCD readout. It needs to be dressed well away from the AC components as AC transients caused the readout to reset and display junk.

The LCD cover glass was made from clear acrylic material available at most home building supply houses. I cut it to size and used my router table to bevel the edges.

Parts layout in the enclosure is not critical and was guided by the fact that all of the controls were added on to the original "simple" autotransformer. The Arduino Uno and protoshield were mounted on the rear panel with the power supply, voltage sensor and power relay mounted on the bottom plate. The current transducer is mounted on the front panel next to the display.

Figure 5 is a close up of the protoshield showing parts layout. The 12 V converter is on the right side while the 5 V converter for the backlight is on the left side.

Ted Drell was first licensed in 1954 as WN5HEU, and obtained his General class license 1 year later, when his call sign changed to W5HEU. His license expired in 1968 while he was overseas, and he was out of ham radio until 2006, when he earned his Amateur Extra class license.

Ted studied Electrical Engineering at Tulane University and The University Southwestern Louisiana. He also studied computer science at Houston Community College, where his primary focus was on "C" and machine language programming.

Ted worked for AT&T Long Lines, supporting

carrier and microwave systems, and Bendix Field Engineering, supporting Stadan and Man Space Programs during the Apollo Space Program (Missions 7-11). He has also been self-employed in Metrology and as a design engineer and engineering manager in multiple areas of energy production.

Ted retired in 2007, although he continues with design and fabrication of one-off products for oil field production control systems. He enjoys antique radios (especially Collins, Drake, National, and other brands from that era) and using microprocessors.

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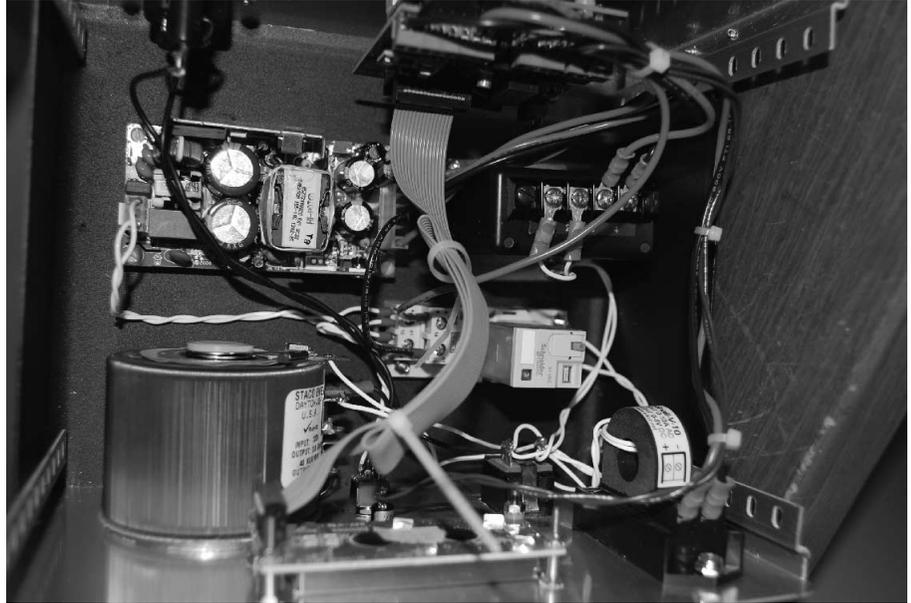


Figure 4 — Top View showing the parts layout.

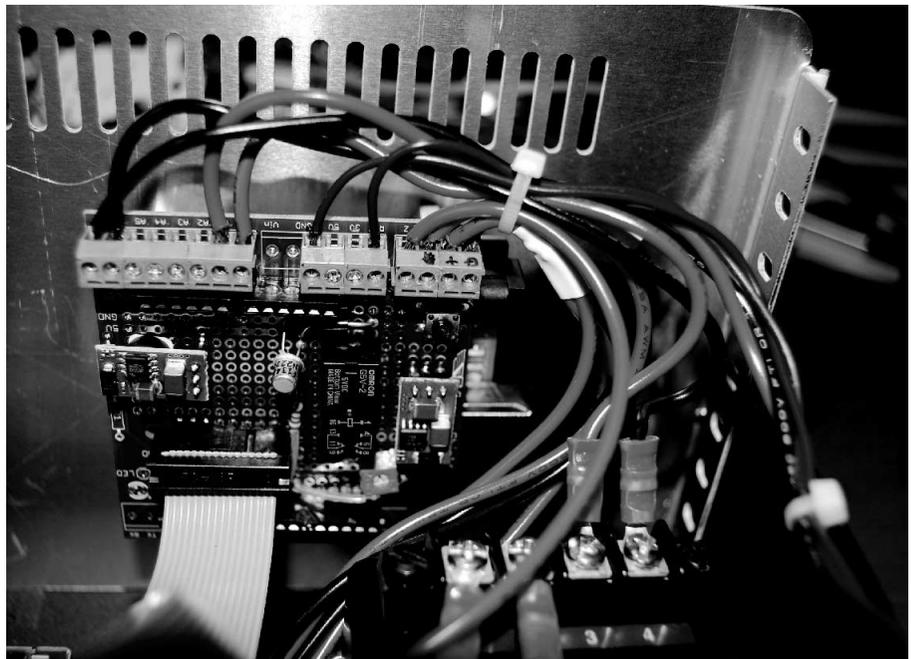


Figure 5 — This is a close-up view of the Arduino protoshield.

Hands On SDR

In this installment we take a look under the hood of a stand-alone software defined radio field programmable gate array (FPGA), to see just how logic gates and registers build a useful radio.

In this second column, I will show you how to set up an FPGA coding environment with free development tools, walk you through the code of an SDR design example and show you how to compile the example code and run it on real hardware. All of this will be very hands-on. We will, of necessity, cover some SDR theory, but we will be taking the background mathematics as a given and instead focus on how we implement the math functions inside the FPGA. We will be reviewing the design at what is called the RTL (register-transfer level) in an HDL (hardware description language) known as *Verilog*. The other main language used by FPGA designers is called *VHDL*, but we will not cover that here. Don't be intimidated by all of these TLAs (three letter acronyms); professionals use these by the boatload to make themselves SMK (sound more knowledgeable). Okay, Okay, so I made up that last one, but you get the idea. Don't I SMK already?

Is this for me?

As with each of these columns, limited space begs the questions: "What do I need to know?" and "What equipment do I need?"

You will need a basic working knowledge of the *Verilog* hardware description language. You should be able to pick this up easily by following one of the many on-line tutorials.¹ I will try to keep the code explanations as simple as possible, but it is beyond the scope of a few pages to describe *Verilog* in any detail. As with most programming languages, a few basic constructs go a long way. If you learn these few constructs, you can at least read and understand the code snippets. Also keep in mind that *Verilog* is used, among other things, to define the behavior of many different types of FPGAs or other hardware, write simulation code and design test benches. (A test bench is a virtual environment built to test the functionality of a piece of software or hardware.) Any *Verilog* skill that you pick up will be useful in understanding other FPGA programs that you encounter.

For hardware, you will need some kind of Altera FPGA development kit. To actually run the code that we are going to compile in this column, you will need a BeMicroSDK FPGA development kit and a UDPSDR-HF1 Receiver, (see Photo A) both available from Arrow Electronics.^{2,3} Even if you do not have the hardware, you can still follow along with the text and learn about

FPGA coding for SDRs. Note that, while you will need some *Verilog* programming knowledge, advanced math skills and RF design experience are still absent. We are *analyzing* an existing SDR, not *designing* one from scratch.

For design software, we are in luck. Altera offers their *Quartus II* FPGA design software as a free download from the Internet for the FPGAs in their Cyclone® family of parts. Both *Linux* and *Windows* versions are available. The BeMicroSDK board contains an EP4CE22F17C7 part from the Altera Cyclone® IV E family of FPGAs, so we can use the free version of *Quartus II* design tools.

Software Installation

After you have read up a bit on *Verilog* (or already grasp at least the basics), the next task is to download and install the *Quartus II* software. Go to the Altera web site (www.altera.com) under the **Design Tools & Services** tab and select **Design Software**.⁴ Click on **Quartus II Web Edition Software** and then the **Download Web Edition Software – Free** button. Select release **14.0**, pick your operating system and download method (**Akamai DLM3 Download Manager** is faster, but is only available for *Windows* users) and make sure that you have selected the **Combined Files** tab. When you are sure that you have made your

¹Notes appear on page 18

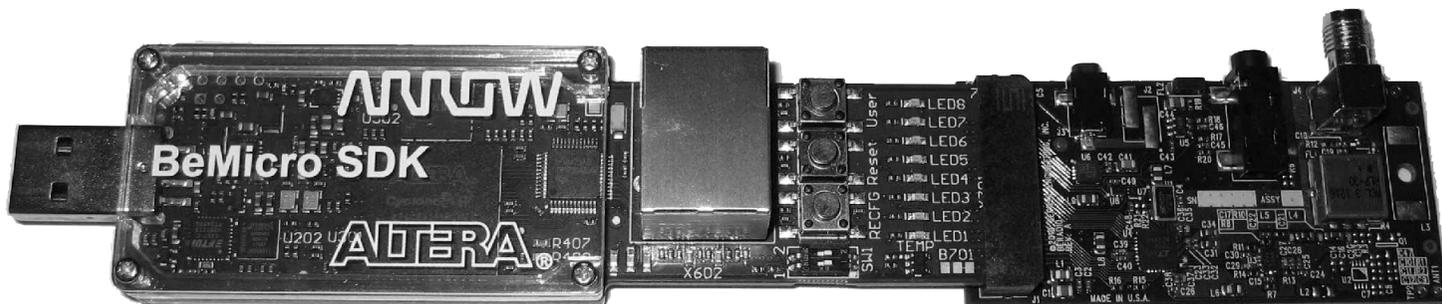


Photo A — The BeMicroSDK data engine together with the HF1 RF front-end board.

selections correctly, click on the blue down-arrow to begin the download. Be patient, the download is large at about 2.1 GB (*Windows*) or 4.0 GB (*Linux*), and may take some time if your connection is slow.

Note that the 14.0 (and newer) releases of *Quartus II* require a 64-bit operating system, *Windows 7* or later or *Red Hat Linux*. (I have successfully installed and run *Quartus II* 14.0 on 64-bit *Ubuntu Linux* 14.04LTS. If you are a *Linux* expert and are willing to read the Altera forums, you can likely make it work; it is beyond the scope of this column to help you with this!) If you do not have a 64-bit operating system, then you must download and install the previous version (13.1) of *Quartus II*. To run *Quartus II* version 13.1, you need *Windows XP SP2* or later, 32- or 64-bit version. Simply select **13.1** in the **Select Release** dialog box before you begin your download. Don't worry if you need to run the older *Quartus II* version; the enhancements made to the newer 14.0 version do not really affect us when using the older Cyclone® IV parts.

A few notes on PC hardware are in order. Pretty much any PC that will run the SDR software (see the Sep/Oct 2014 *QEX Hands On SDR* column) will run the *Quartus II* software.⁵ The most important hardware your *Quartus II* PC must have is memory. At least 2 GB is a minimum. Slower processors are okay (if you are willing to wait longer for compiles to finish), but stability

of the software is not as good with less memory. Even simple FPGA compiles are significantly more compute intensive than compiling a “Hello World” program in *C*.

For help on getting *Quartus II* set up, and more hardware information on the BeMicroSDK, please take a look at the BeMicroSDK Embedded System Lab, modules 1, 2 and 3, available on line.⁶ Don't worry that it was written for *Quartus II* version 12.1; with a few obvious adjustments, it is a good Lab to follow to gain more experience before we jump into our real SDR code.

To get a copy of the FPGA source code, download a copy of the *Quartus* archive from the SDRstick website.⁷ The archive not only contains the source files (with a .v extension), but the pin assignment file (.qsf extension), timing constraints file (.sdc extension) and many other files needed to successfully compile the complete project. Once you have downloaded the archive file, start the *Quartus II* software and click on <file><open project...>. Navigate to the .qar file that you downloaded and click on it. From the dialog box that opens, select the destination folder (usually the default is fine) and click **OK**. *Quartus* will extract all of the files from the archive and set up the project, all ready to go.

Quartus II Quick Tips

While a *Quartus* tutorial is beyond the scope of this column, here are a few quick

tips to get you started.⁸ When you open *Quartus II*, you see a tool bar across the top of the window, and four “panes” within the window. See Figure 1. The upper left pane is the **Project Navigator** pane, below that is the **Tasks** pane, and across the bottom is the **Messages** pane. If you look closely, you will see these exact names in the title bar of each pane. The remaining upper right-hand pane is the **Workspace** area, where we will look at source code and report files, among other things.

At the bottom of the Project Navigator pane, there are several tabs: **Hierarchy**, **Files**, **Design Units** and so on. Click on the **Files** tab to see a list of all of the files in the project. You will see many *Verilog* source files (.v), a few ROM data files (.hex), a timing constraints file (.sdc) and a few others. Double-click on a Verilog source file in the **Project Navigator** pane and *Quartus* opens the file in the **Workspace** for you to view or edit. You can open as many files as you like; *Quartus* will make a tab in the **Workspace** for each file so you can switch quickly between them. Before we dig into specific sections of the code, let's take a look at the overall architecture of the FPGA firmware.

High-Level Overview

The FPGA RF processing is shown in Figure 2 and the audio processing is shown in Figure 3. The overall topology closely follows that of an analog direct conversion

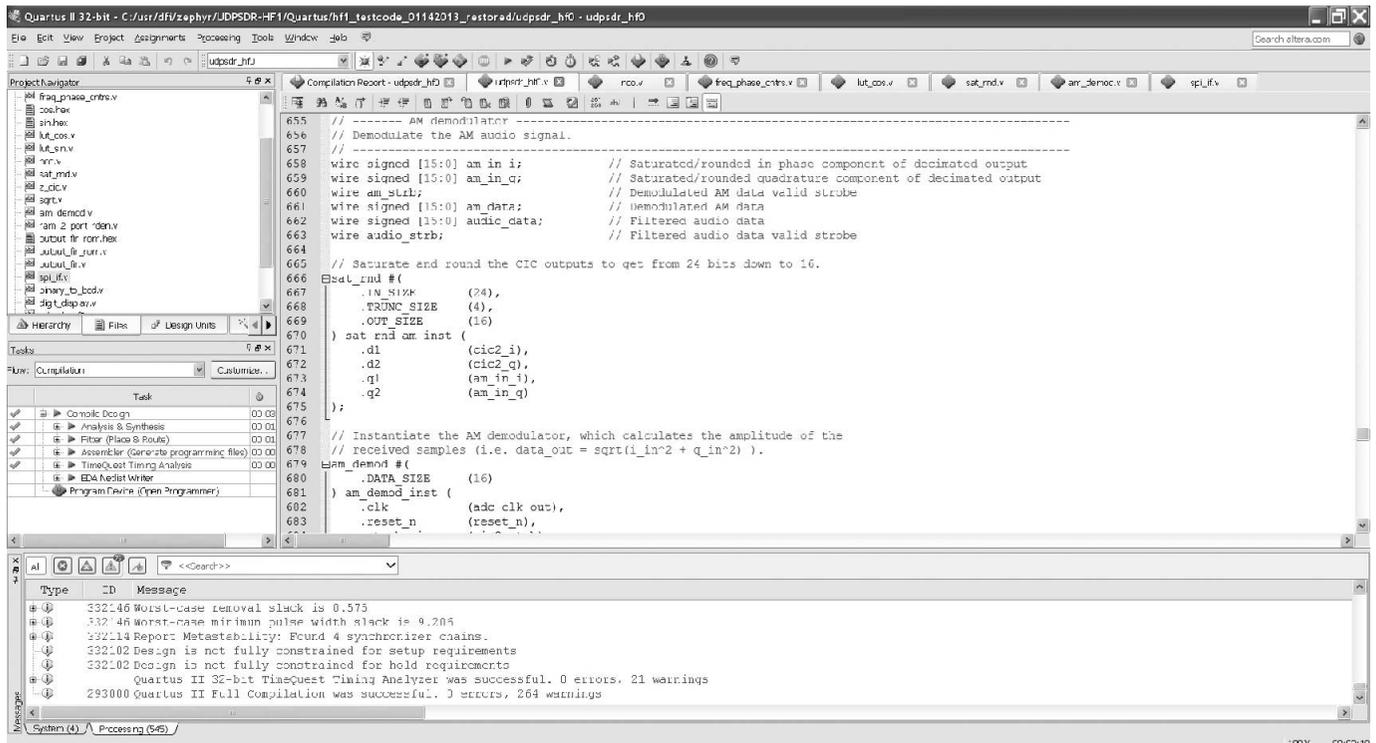


Figure 1 — This screen shot shows the *Quartus II* design software.

receiver. We start with two multipliers (quadrature mixer) fed by a Numerically Controlled Oscillator (NCO) acting as a digital local oscillator. The result is then filtered by two Cascaded Integrator-Comb (CIC) filters, demodulated by calculating the magnitude (square root of the sum of the squares), filtered again by a Finite Impulse Response (FIR) low-pass filter and scaled to provide a variable audio gain. The processed data is then clocked out to an audio DAC via a Serial Peripheral Interface (SPI) port. The SAT/RND blocks perform a saturation and rounding function to prevent overflow when we reduce the number of bits in the data path.

We will take an in-depth look at four of these blocks (multiplier, NCO, CIC and demodulator) and a cursory look at the rest of them. If you study the complete source code, you will discover that there are many more housekeeping and control functions that we do not cover. I have to leave something for you to figure out for yourself after you become a *Verilog* expert!

Even though I have reproduced small pieces of code here, you will find it helpful to open the “real thing” in the *Quartus* Workspace because the color formatting will make things easier to follow. To get started, open the *Verilog* source file `udpsdr_hf0.v` by double-clicking it. This file is the top-level file in the design. How do we know this? Take a quick look at the **Hierarchy** tab in the **Project Navigator**, and you will see it listed at the top level.

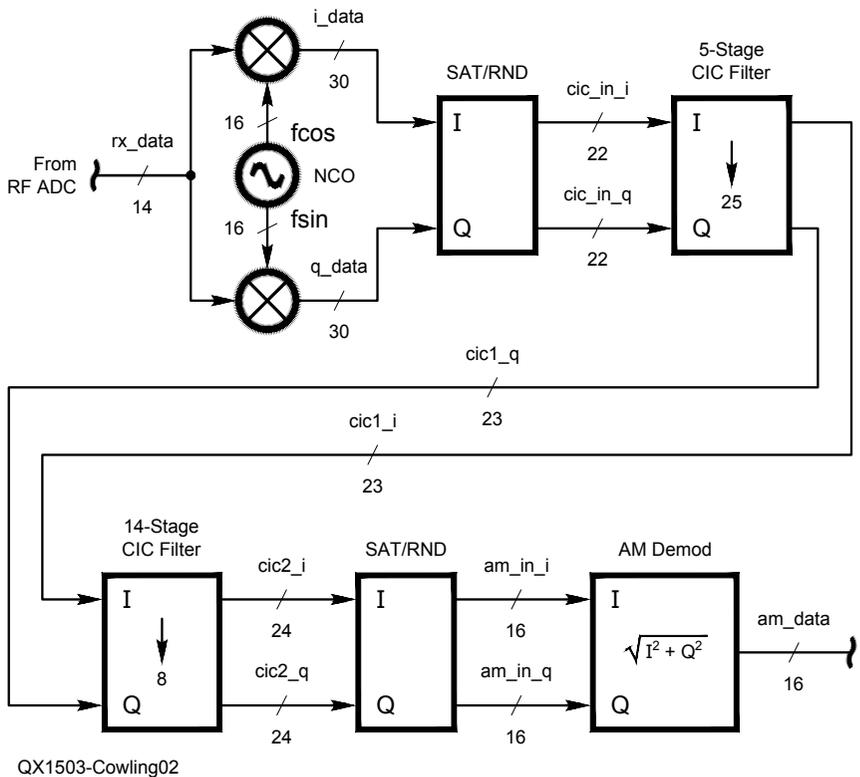


Figure 2 — HF1 FPGA test code RF section block diagram.

Quadrature Mixer

Scroll down to about line 570 in the `udpsdr_hf0.v` file that you just opened, or look at Figure 4 (line numbers in the file may be slightly different than in the figure). Anything after the “//” on a line is a comment, so lines 568 and 569 just document the function of the block. Lines 570 to 579 are called an “always block”; this block is a wrapper that contains some circuitry. In our case, this circuitry consists

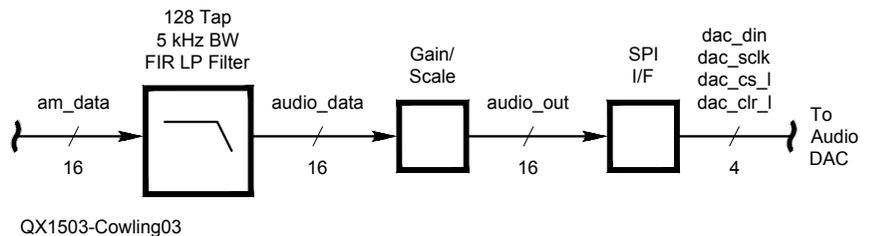


Figure 3 — HF1 FPGA test code AF section block diagram.

Sidebar: HF0, HF1 and BeRadio

Throughout the *Verilog* code, you will see references to BeRadio, HF0 and HF1. While they seem to be interchangeable, they are not quite synonymous. Here is the 5-minute explanation of these terms. The SDRstick series of receivers originally consisted of three boards with three ascending performance levels: HF0 (12 bits at 10 Msps), HF1 (14 bits at 80 Msps) and HF2 (16 bits at 122.88 Msps). Since the HF0 was designed as a low-cost SDR demonstrator board to be used with BeMicroSDK, and other boards (such as the BeInMotion motor control board) already made use of the “Be” prefix, the name BeRadio was coined. BeRadio and HF0 are thus the exact same board.

BeRadio/HF0 was marketed by Arrow Electronics for only a limited time, and is no longer available. HF0 and HF1 are almost identical designs, however. They are so close, in fact, that they are built on the same base circuit board and differ only in the components that are soldered to the board. Such close hardware design kinship is the reason that HF0/BeRadio and HF1 can share large portions of their FPGA firmware. If you look closely, you can see that the *Quartus HF1_testcode* project was made from only slight modifications to the **HF0** project code.¹⁵

of two registers, one named **i_data** and the other named **q_data**. The width of these registers is defined in the code on lines 493 and 494 (not shown), but we can get a clue as to their width by looking at the widths defined in the initialization assignments on lines 572 and 573. The term **30'h0** means a value that is 30 bits wide, with a hexadecimal value of zero.

The list of edges and signals in parentheses immediately following the @ on line 570 is called the **sensitivity list**. In our case, whenever **adc_clk_out** rises from 0 to 1 or **reset_n** falls from 1 to 0, all of the statements within the always block are evaluated. The

```

568 // Shift received signal to zero by multiplying (mixing)
569 // with the local oscillator.
570 always @(posedge adc_clk_out or negedge reset_n) begin
571     if (!reset_n) begin
572         i_data <= 30'h0;
573         q_data <= 30'h0;
574     end
575     else begin
576         i_data <= fcos * rx_data;
577         q_data <= fsin * rx_data;
578     end
579 end

```

Figure 4 — This is a piece of the Verilog code for a quadrature mixer.

```

25 module z_nco (
26     input  wire clk,                // System clock
27     input  wire reset_n,           // System reset
28     input  wire [31:0] phase_inc,  // Phase increment
29     output wire [15:0] fcos,       // Cosine output
30     output wire [15:0] fsin       // Sine output
31 );
32 // -----
33
34 // ---- Phase Accumulator -----
35 reg [31:0] accum;                // Phase accumulator
36
37 // Accumulate the current phase increment every clock cycle
38 always @(posedge clk or negedge reset_n) begin
39     if (!reset_n) begin
40         accum <= 32'h0;
41     end
42     else begin
43         accum <= accum + phase_inc;
44     end
45 end
46 // -----
47
48 // ---- Lookup Tables -----
49 // Cosine lookup table.
50 lut_cos lut_cos_inst (
51     .address ( accum[31:20] ),
52     .clock ( clk ),
53     .q ( fcos[15:0] )
54 );
55
56 // Sine lookup table.
57 lut_sin lut_sin_inst (
58     .address ( accum[31:20] ),
59     .clock ( clk ),
60     .q ( fsin[15:0] )
61 );
62 // -----
63 endmodule

```

Figure 5 — This piece of Verilog code is for a numerically controlled oscillator (NCO).

begin keyword is used to define the boundary of the always block, and is matched with the **end** keyword on line 579. Every **begin** must have a matching **end**; they are paired just like parentheses. Note that the **end** statements are all indented to start in the same column as the beginning column of the line containing the matching **begin** keyword: line 574 aligns with line 571, line 578 aligns with line 575 and line 579 aligns with line 570. This is an example of good, easy to read *Verilog* coding style.

This always block defines the operation of the two 30-bit registers, **i_data** and **q_data**. The falling edge of **reset_n** (which is the assertion of reset, since **reset_n** is active low) causes both registers to be cleared (lines 571 to 574). Note that the **or** in the sensitivity list means that this happens irrespective of the **adc_clk_out** clock state, therefore making this reset an asynchronous one. The rising edge of **adc_clk_out** (as long as **reset_n** is de-asserted) will cause **i_data** to be updated with the value of the product of **fcos** and **rx_data**, while **q_data** is updated with the value of the product of **fsin** and **rx_data** (lines 575 to 578). This is our quadrature “mixer”: two numerical multipliers.

Note the widths of the inputs to each multiplier. (You can look in the code on lines 444, 488 and 489 or look on the block diagram in Figure 2.) When we multiply, the bit width of the output is the sum of the widths of the inputs, so we must make sure that the variable that is assigned the product is defined to be wide enough. This is a signed multiply because both inputs and outputs are declared as signed numbers. If you forget to declare these as signed numbers, the *Verilog* compiler will implement an unsigned multiplier, which is a common *Verilog* coding error to be avoided. One other thing to note is the order of the assignments in the always block. The reset code is implemented as the first part of an **if...else** construct to ensure that the asynchronous reset takes precedence over the

synchronous multiply operation. However, all variable values within the block are updated at the same time, regardless of the order of the assignment statements. All 60 bits of **i_data** and **q_data** are updated simultaneously in parallel (whether set to zero by **reset_n** or to the products of other variables by **adc_clock_out**). I have reviewed this simple block of code in detail because it is the first one. We will move a bit faster on the next blocks, focusing more on what the block does rather than how *Verilog* works.

Numerically Controlled Oscillator (NCO)

The next block that we will analyze is the numerically controlled oscillator, or NCO. The NCO is a bit different than a simple oscillator in that it produces two sine wave outputs that are 90° out of phase. The first output is named **fcos** and will be used to calculate **i_data** values. The other output is named **fsin** and will be used to calculate **q_data** values. These variable names should already be familiar, as they are used by the quadrature mixer discussed earlier.

The behavior of the **z_nco** module is defined in the **nco.v** file, the majority of which is reproduced in Figure 5. The module is *instantiated* in the main file (see lines 560 to 566 of **udpsdr_hf0.v**) in much the same way a component is placed on a schematic: call out the module name, give it a unique instance name (like a reference designator on a schematic, for example R22 or U3) and connect up inputs and outputs to the module. The direction, type, width and name of module I/O signals are defined on lines 26 to 30.

The NCO outputs are derived from two lookup tables, **lut_cos** and **lut_sin**. A phase accumulator named **accum** is used as an address into the lookup tables. The accumulator is incremented on every clock

cycle by a number of counts determined by the value of the module input, **phase_inc**. The larger the value of **phase_inc**, the faster the lookup tables are “scanned,” and therefore the higher the NCO output frequency. You can take a look at the 16-bit values in the lookup tables by opening the **cos.hex** and **sin.hex** files in the **files** tab of the *Quartus* Project Navigator pane (make sure you specify 16 bits as the width when asked). You might ask, “How did you create the two look up table files?” Well, that is a very good question. We actually wrote a small program in *Python* to calculate the values in the two hex files. We then used a *Quartus* memory generator wizard to use the hex files to initialize two 4096 × 16 SRAM blocks as read-only memories (ROMs). The two ROMs become our look-up tables. Take a look at the wizard-generated **lut_cos.v** and **lut_sin.v** files and you can probably figure out how we did it.

The astute reader is probably wondering why we used two ROMs instead of just offsetting the address into one ROM to achieve the desired 90° phase shift. (You sure are full of good questions today!) The answer is that the logic is simpler and we are lazy. Remember that both lookup tables are accessed every clock cycle. If you want two 16-bit numbers (one for sine and one for cosine) every clock cycle from the same ROM, then you have to read it twice as fast as the clock. While this is possible, it is not as simple as just using more memory. After all, that 16 K bytes of memory is not being used for anything else... (Now I am talking like a software guy.)

Saturate and Round Module

If you would like to explore this function in detail, open the **sat_rnd.v** file by double-clicking it in the *Quartus* Project Navigator **files** tab. This is a *parameterizable* module,

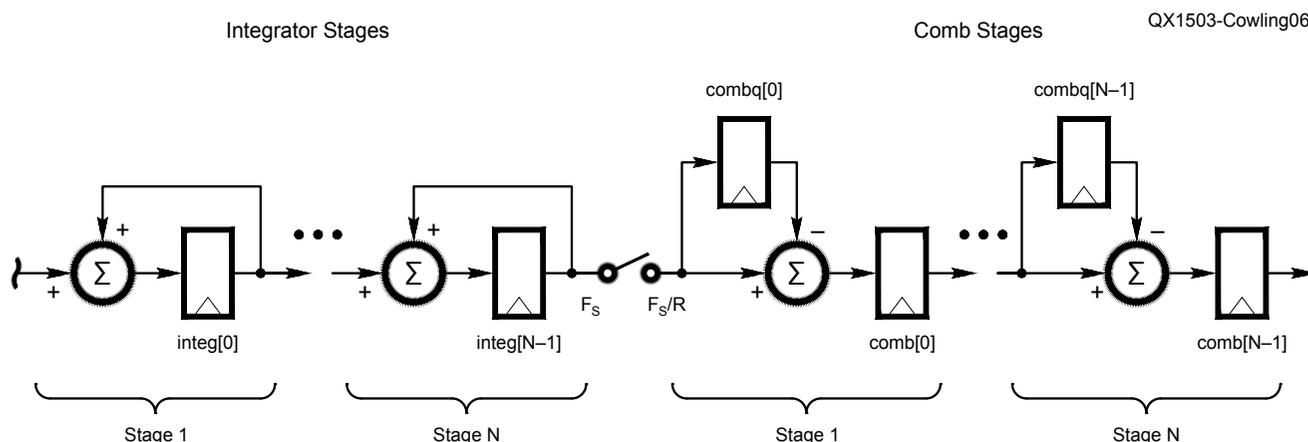


Figure 6 — Here is a pipelined CIC decimating filter block diagram.

```

17 module z_cic
18 #(
19     parameter IN_SIZE = 16,                // Input data width
20     parameter OUT_SIZE = 16,              // Output data width
21     parameter N_STAGES = 5,              // Number of stages
22     parameter DEC_RATE = 10              // Decimation rate
23 ) (
24     input wire clk,                        // System clock
25     input wire reset_n,                   // System reset
26     input wire instrobe,                  // Input sample valid strobe
27     input wire signed [IN_SIZE-1:0] in1_data, // Channel 1 input sample
28     input wire signed [IN_SIZE-1:0] in2_data, // Channel 2 input sample
29     output wire outstrobe,                // Output sample valid strobe
30     output reg signed [OUT_SIZE-1:0] out1_data, // Channel 1 output sample
31     output reg signed [OUT_SIZE-1:0] out2_data // Channel 2 output sample
32 );
33 // -----
34
35 // ---- Function Definitions -----
36 // Function to calculate ceiling of Log base 2 of a value.
37 function integer clog_b2;
38     input [31:0] value;
39     integer tmp;
40     begin
41         tmp = value - 1;
42         for (clog_b2 = 0; tmp > 0; clog_b2 = clog_b2 + 1) tmp = tmp >> 1;
43     end
44 endfunction
45 // -----
46
47 // ---- User Parameters -----
48 // Derive internal parameters from input parameters using the Log2 function.
49 // -----
50 localparam CNTR_SIZE = clog_b2(DEC_RATE); //Size of sample decimation counter
51 localparam ACC_SIZE = IN_SIZE + (N_STAGES*CNTR_SIZE); //Width of integration accumulators
52// -----
53
54 // ---- Module Control -----
55 reg [CNTR_SIZE-1:0] sample_count; // Sample decimation counter
56 reg combstrobe; // Strobe for activating comb stages
57 reg [1:0] del_strobe; // Pipelined comb strobe to match
latency
58
59 // Generate internal strobe for every DEC_RATE input strobes.
60 always @(posedge clk or negedge reset_n) begin
61     if (!reset_n) begin
62         sample_count <= {(CNTR_SIZE){1'b0}};
63     end
64     else begin

```

Figure 7 — Part 1 of the Verilog code for a cascaded integrator-comb filter.

```

65     del_strobe <= {del_strobe[0] , combstrobe};
66     if (instrobe) begin
67         if (sample_count == DEC_RATE - 1) begin
68             sample_count <= {(CNTR_SIZE){1'b0}};
69             combstrobe <= 1'b1;
70         end
71         else begin
72             sample_count <= sample_count + 1'b1;
73             combstrobe <= 1'b0;
74         end
75     end
76     else begin
77         combstrobe <= 1'b0;
78     end
79 end
80 end
81 // -----
82
83 // ---- Integrator Stages -----
84 reg signed [ACC_SIZE-1:0] integ1 [N_STAGES-1:0];           // Array of integrators for channel 1
85 reg signed [ACC_SIZE-1:0] integ2 [N_STAGES-1:0];           // Array of integrators for channel 2
86 integer i;                                                  // FOR loop variable
87
88 // For each integration stage, integrate the value of the previous stage. The
89 // first stage integrates the input data.
90 always @(posedge clk or negedge reset_n) begin
91     if (!reset_n) begin
92         for (i = 0; i < N_STAGES; i = i + 1) begin
93             integ1[i] <= 0;
94             integ2[i] <= 0;
95         end
96     end
97     else begin
98         if (instrobe) begin
99             integ1[0] <= integ1[0] + {(ACC_SIZE-IN_SIZE){in1_data[IN_SIZE-1]}},in1_data};
100            integ2[0] <= integ2[0] + {(ACC_SIZE-IN_SIZE){in2_data[IN_SIZE-1]}},in2_data};
101            for (i = 1; i < N_STAGES; i = i + 1) begin
102                integ1[i] <= integ1[i] + integ1[i-1];
103                integ2[i] <= integ2[i] + integ2[i-1];
104            end
105        end
106    end
107 end

```

meaning that certain characteristics of the module can be defined when it is instantiated by setting values of pre-defined parameters. These parameter values are used by the code to modify the way the module behaves. Take a look at the block diagram in Figure 2. Notice that the SAT/RND module is used twice, once before the first CIC filter and once after the second CIC filter. In the former case, it reduces the data width from 30 to 24 bits and in the latter case, from 24 to 16 bits. (See `udpsdr_hf0.v` lines 605 to 617 and 666 to 675 for the two instantiations.) I will explain how it does this after I describe the function of this module.

The SAT/RND module performs three operations on its input data. First it truncates the data to a specific bit width by removing a number of least-significant bits from the input data. Next it rounds the result to the nearest value based on the discarded bits. Finally, it checks to make sure that the rounded value can be represented properly in the output bit width (in other words, there is no overflow or underflow). Note that the input and output data are signed numbers. If overflow is detected, the output is set to the maximum positive value (sign bit is 0, all other bits are 1). If underflow is detected, the maximum negative value is used instead (sign bit is 1, all other bits are 0). These numbers are called saturation values.

When the module is instantiated, parameters `IN_SIZE`, `OUT_SIZE` and `TRUNC_SIZE` are specified corresponding to the input bit width, output bit width and the number of bits to remove, respectively. The same module is used in both places in our block diagram, but each is instantiated with different values for the three parameters. This is useful, since we save ourselves the work of writing two different modules. Of course, TANSTAAFL (yes, it is more than three letters, and yes, I am going to make you turn to the end of the column to look it up),⁹ so we end up with a slightly more complex module as a result. This sure seems like a lot of trouble just to reduce the number of bits in the data stream, but it is essential to minimize overflow and underflow discontinuities.

Cascaded Integrator-Comb (CIC) Filters

I have deliberately given you less and less assistance in analyzing the *Verilog* code in the last three sections. The goal is for you to eventually be able to read and digest new sequences of code on your own. This next section will test your skill (and perhaps your patience, too) with yet more complexity. Take a look at Figure 6, the block diagram of the CIC filter. Each circle containing a Σ represents an adder and each block is a register. An adder-register pair is called an

accumulator. I have shown only two stages of the filter (first and last) for brevity, but the ellipsis shows where additional stages are inserted. The switch symbol shown between the integrator stages and the comb stages represents a reduction in the clock rate by a factor equal to the decimation rate, *R*. Thus, the left-most CIC filter shown in Figure 2 (5-stages) consists of ten accumulators and five registers for each data path (*i* and *q*), along with the register clocking circuitry, which I will explain shortly.

This is a parameterized design, with input and output bit widths, number of stages and the decimation rate set at instantiation time. The numbers given on lines 19 to 22 of Figure 7 are the defaults that are used if one or more parameters are not set at instantiation. You can look in `udpsdr_hf0.v` lines 621 to 624 and 638 to 641 for the instantiated values for the 5-stage and 14-stage CIC filters, respectively. The 5-stage filter uses an `IN_SIZE` of 22, `OUT_SIZE` of 23, `N_STAGES` of 5 and `DEC_RATE` of 25.

Let's look at the register and accumulator structure in the code before we see how the registers are clocked. The integration stage accumulator register arrays `integ1` and `integ2` are defined on lines 84 and 85 of Figure 7. The bit range (register width) is defined in the left-hand set of square brackets. The array index range is defined in the right-hand set of brackets. Notice that the number of bits in these accumulator registers is wider than the input bit width since we need to hold the sum of many input samples. (See line 51 for the definition of `ACC_SIZE`.) The number of registers in each array is equal to the number of stages in the filter. The behavior of the accumulators is defined within the always block on lines 90 to 107 of Figure 7. The first accumulator adds the sign-extended input data to its current value on each clock. The remaining accumulators each sum the output from the previous accumulator and their own current value on each clock using the `for` loop on lines 101 to 104.

The `comb` and `combq` registers are defined on lines 111 to 114 of Figure 8. The `comb` registers are used as registers in the accumulators (they each directly follow an adder), while the `combq` registers store the value of each accumulator's (+) input, to be used one clock cycle later at the accumulator's (-) input. The always block on lines 151 to 162 performs one last function that is not shown in the block diagram of Figure 6: it truncates the output to the number of bits specified by the `OUT_SIZE` parameter and rounds to the nearest bit.

Notice that every one of the four always blocks in Figures 7 and 8 are clocked by the `clk` input clock. It is much easier to analyze the register timing of this synchronous design

than it would be if the output registers were clocked by a different clock signal. So where does the decimation occur, then? Remember that the output data rate is equal to the input rate divided by the decimation rate. If you look at Figure 8, line 130 you will see that while the always block is evaluated on every `clk` edge, the `if` condition will be true only when `combstrobe` is true. Take a look at the always block in Figure 7, lines 60 to 80; this is where `combstrobe` is generated. With a bit of study, you can see that one `combstrobe` is generated for every `DEC_RATE instrobe` assertions. The output rate will therefore be slower than the input rate by a factor equal to the decimation rate.

Altera's AN455 application note is an excellent place to start for more information on CIC filters in FPGAs.¹⁰

AM Demodulator

The AM demodulator code is in the `am_demod.v` file, most of which is reproduced in Figure 9. The magnitude of the AM demodulator output is equal to the square root of the sum of the squares of the *i* and *q* input components. The always block on lines 40 to 51 squares the incoming *i* and *q* values. The assign statement on line 55 then adds them together, while the always block on lines 76 to 83 takes the square root of the sum. Note that we delay the `strobe_in` signal to account for the number of clock cycles that are required to calculate the magnitude, and then assign the delayed signal to the `strobe_out` of the module on line 86. This is called *pipelining* the signal.

Finite Impulse Response (FIR) Low-pass Filter

While explaining the coding of an FIR filter is beyond the scope of this column, there are good references on the Internet.^{11, 12} Basically, the FIR filter is just a digital low-pass filter consisting of a series of multipliers and registers feeding a large adder tree. The FIR filter requires a table of coefficients that are typically supplied by a ROM, in much the same way that the numerically controlled oscillator stores its lookup tables. Altera provides a software wizard to assist you in calculating the coefficients. The number of multipliers, called taps, plus the values of the coefficients, determines the LPF cutoff frequency and its slope. The FIR filter code is in the file `output_fir.v`, which also uses the three files `output_fir_rom.v`, `output_fir_rom.hex` and `ram_2_port_rden.v`.

Audio Gain, Scaling and Serial Peripheral Interface (SPI)

The filtered audio is multiplied by an audio gain coefficient to set the desired

```

110 // ---- Comb Stages -----
111 reg signed [ACC_SIZE-1:0] comb1 [N_STAGES-1:0]; // Array of comb stages for channel 1
112 reg signed [ACC_SIZE-1:0] comb1q [N_STAGES-1:0]; // Array of delayed comb values for channel 1
113 reg signed [ACC_SIZE-1:0] comb2 [N_STAGES-1:0]; // Array of comb stages for channel 2
114 reg signed [ACC_SIZE-1:0] comb2q [N_STAGES-1:0]; // Array of delayed comb values for channel 2
115 integer j; // FOR loop variable
116
117 // For each comb stage, subtract the previous value of the previous stage from
118 // the current value of the previous stage. The first stage subtracts from the
119 // value of the final integration stage.
120 always @(posedge clk or negedge reset_n) begin
121     if (!reset_n) begin
122         for (j = 0; j < N_STAGES; j = j + 1) begin
123             comb1[j] <= 0;
124             comb1q[j] <= 0;
125             comb2[j] <= 0;
126             comb2q[j] <= 0;
127         end
128     end
129     else begin
130         if (combstrobe) begin
131             comb1[0] <= integ1[N_STAGES-1] - comb1q[0];
132             comb1q[0] <= integ1[N_STAGES-1];
133             comb2[0] <= integ2[N_STAGES-1] - comb2q[0];
134             comb2q[0] <= integ2[N_STAGES-1];
135             for (j = 1; j < N_STAGES; j = j + 1) begin
136                 comb1[j] <= comb1[j-1] - comb1q[j];
137                 comb1q[j] <= comb1[j-1];
138                 comb2[j] <= comb2[j-1] - comb2q[j];
139                 comb2q[j] <= comb2[j-1];
140             end
141         end
142     end
143 end
144 // -----
145
146 // ---- Output -----
147 // Assign final element of delayed comb strobe as the output strobe.
148 assign outstrobe = del_strobe[1];
149
150 // Round off LSBs of final comb output to get filter output.
151 always @(posedge clk or negedge reset_n) begin
152     if (!reset_n) begin
153         out1_data <= 0;
154         out2_data <= 0;
155     end
156     else begin
157         out1_data <= comb1[N_STAGES-1][ACC_SIZE-1:ACC_SIZE-OUT_SIZE] +
158             comb1[N_STAGES-1][ACC_SIZE-OUT_SIZE-1];
159         out2_data <= comb2[N_STAGES-1][ACC_SIZE-1:ACC_SIZE-OUT_SIZE] +
160             comb2[N_STAGES-1][ACC_SIZE-OUT_SIZE-1];
161     end
162 end
163 // -----
164 endmodule

```

Figure 8 — Part 2 of the Verilog code for a cascaded integrator-comb filter.

volume. Selected bits of the result are formatted and serially shifted out to match the serial peripheral interface (SPI) of the audio DAC on the HF1 board. The bits are selected to provide the loudest volume while still preventing DAC overload.

Perceptive readers will note that this code actually contains a NIOS II soft-core CPU to control some functions. We have deliberately avoided adding the complexity of an embedded CPU to our discussion, leaving that topic instead for another day. If you are ambitious, the entire source for the NIOS II CPU is included in the *Quartus* Archive (.qar file) for your amusement.

What's Next?

Now that you have a working knowledge of FPGA techniques for SDR, what can you do next? The openHPSDR project is open source, so why not take a look at the FPGA code for the Mercury receiver, Pennylane transmitter, Metis Ethernet interface or even the Hermes transceiver? Each one of these boards has an on-board FPGA and *Verilog* code to match. It is all available from the openHPSDR repository, and you are now qualified to download it, read it, understand it and even modify, compile and run it on your own HPSDR hardware if you like.^{13, 14} The tools that you have used today are the very same tools that the developers use when they write or update the code.

Next time we can cover how to compile, download and execute code in the BeMicroSDK FPGA, or we can go off in another direction, such as GNU Radio. Please drop me an e-mail if you have any suggestions for topics you would like to see covered in future Hands-On-SDR columns or even just to let me know whether or not you found this discussion useful.

Notes

¹Many *Verilog* tutorials and references are available by searching "Verilog tutorial" with your favorite search engine. Here are a few links:

Tutorial: doulos.com/knowhow/verilog_designers_guide/.

Tutorial: vol.verilog.com/VOL/main.htm.
Reference: sutherland-hdl.com/online_verilog_ref_guide/vlog_ref_top.html.

Reference: see.ed.ac.uk/~gerard/Teach/Verilog/manual/.

²The BeMicroSDK development kit circuit board is available from Arrow Electronics: parts.arrow.com/item/detail/arrow-development-tools/bemicrosdk.

³The UDPSDR-HF1 development kit circuit board is available from Arrow Electronics: parts.arrow.com/item/detail/arrow-development-tools/udpsdr-hf1.

⁴You can download the free Altera Web Edition software from the Altera website: altera.com/products/software/quartus-ii/web-edition/qts-we-index.html.

⁵Scotty Cowling, WA2DFI, "Hands On SDR,"

QEX, Sep/Oct 2014, pp 31 – 38.

⁶Download the Altera BeMicroSDK embedded system lab document: download.silicon-expert.com/pdfs/2013/5/20/12/17/55/611/arrowd_/manual/bemicro_sdk_embedded_system_hw_lab_qsys_v12_1.pdf.

⁷The source code is available from the SDRstick SVN at svn.sdrstick.com under the <[sdrstick-release/BeMicroSDK/udpsdr-hf1/firmware/source](http://svn.sdrstick.com/sdrstick-release/BeMicroSDK/udpsdr-hf1/firmware/source)> directory. The file name is <[hf1_testcode_11182014.qar](http://svn.sdrstick.com/sdrstick-release/BeMicroSDK/udpsdr-hf1/firmware/source/hf1_testcode_11182014.qar)>

⁸Introduction to *Quartus II* Software: <altera.com/literature/manual/quartus2_introduction.pdf>

⁹TANSTAAFL, or "There ain't no such thing as a free lunch" has several popular usages, including in science fiction and economics. See <en.wikipedia.org/wiki/There_ain't_no_such_thing_as_a_free_lunch>

¹⁰Altera AN455, "Understanding CIC Compensation Filters," <altera.com/literature/an/an455.pdf>

¹¹FIR Filter Design from Altera Wiki: <alterawiki.com/wiki/FIR_Filter_Design_in_Arria_V/Cyclone_V_DSP_Block_Using_VHDL_Infering>

¹²Implementing FIR Filters and FFTs, Altera white paper: <altera.com/literature/wp/wp-01140-fir-fft-dsp.pdf>

¹³Look in the TAPR repository svn.tapr.org in <main/trunk> under the board name

¹⁴The openHPSDR hardware is available from TAPR at tapr.org/hpsdr_index.html

¹⁵The HF0 source code can be found at svn.sdrstick.com in the <[sdrstick-release/beradio/beradio-firmware/source](http://svn.sdrstick.com/sdrstick-release/beradio/beradio-firmware/source)> directory. The file name is <[BeRadio_lab_01232013.qar](http://svn.sdrstick.com/sdrstick-release/beradio/beradio-firmware/source/BeRadio_lab_01232013.qar)>

```

15 module am_demod
16 #(
17     parameter DATA_SIZE = 16                // Bits in data path
18 ) (
19     input  wire  clk,                          // System clock
20     input  wire  reset_n,                      // Asynchronous system reset
21     input  wire  strobe_in,                   // Input data valid strobe
22     input  wire  signed [DATA_SIZE-1:0] i_in, // In-phase input data
23     input  wire  signed [DATA_SIZE-1:0] q_in, // Quadrature input data
24     output wire  strobe_out,                  // Output data valid strobe
25     output wire  signed [DATA_SIZE-1:0] data_out // Output data
26 );
27 // -----
28
29 // ---- AM Demodulator -----
30 reg [2:0] strb_sr; // Shift register to pipeline input strobe
31 reg signed [2*DATA_SIZE-1:0] i_sqrq; // Squared in-phase data
32 reg signed [2*DATA_SIZE-1:0] q_sqrq; // Squared quadrature data
33 wire [2*DATA_SIZE:0] sqrsum; // Sum of squares of in-phase and quadrature data
34 reg [2*DATA_SIZE-1:0] sqrsumq; // Registered sum of squares
35 wire [DATA_SIZE-1:0] sqrt_data; // Amplitude of received data
36 reg signed [DATA_SIZE-1:0] sqrtq; // Registered amplitude of received data

```

Figure 9 — Here is a sample piece of *Verilog* code for an AM demodulator.

```

37
38 // Square the in-phase and quadrature components of the input.
39 // Pipeline the input strobe to match latency.
40 always @(posedge clk or negedge reset_n) begin
41     if (!reset_n) begin
42         strb_sr    <= 3'h0;
43         i_sqrq    <= {(2*DATA_SIZE){1'b0}};
44         q_sqrq    <= {(2*DATA_SIZE){1'b0}};
45     end
46     else begin
47         strb_sr    <= {strb_sr[1:0], strobe_in};
48         i_sqrq    <= i_in * i_in;
49         q_sqrq    <= q_in * q_in;
50     end
51 end
52
53 // Sum of the squares plus one to implement rounding. If bit 0 is set, this
54 // rounds up (more positive).
55 assign sqrsum = i_sqrq + q_sqrq + {(2*DATA_SIZE-1){1'b0}},1'b1};
56
57 // Register the sum of the squares after rounding off the LSB.
58 always @(posedge clk or negedge reset_n) begin
59     if (!reset_n) begin
60         sqrsumq    <= {(2*DATA_SIZE){1'b0}};
61     end
62     else begin
63         sqrsumq    <= sqrsum[2*DATA_SIZE:1];
64     end
65 end
66
67 // Calculate the amplitude of the received signal as the square root of the
68 // sum of the squares.
69 sqrt sqrt_inst (
70     .radical (sqrsumq),
71     .q (sqrt_data),
72     .remainder ()
73 );
74
75 // Register the square root output.
76 always @(posedge clk or negedge reset_n) begin
77     if (!reset_n) begin
78         sqrtq <= {DATA_SIZE{1'b0}};
79     end
80     else if (strb_sr[1]) begin
81         sqrtq <= sqrt_data;
82     end
83 end
84
85 // Assign output strobe and data.
86 assign strobe_out = strb_sr[2];
87 assign data_out   = sqrtq;
88 // -----
89 endmodule

```

Noise Power Ratio (NPR) Testing of HF Receivers

The author uses notched noise to evaluate dynamic receiver performance.

(An earlier version of this article appeared in the Sep/Oct 2013 issue of NCJ.)

Noise-power ratio (NPR) testing is a performance test technique in which a notched noise band is applied to the input of the device under test (DUT), and the output of the DUT is connected to a selective level meter whose bandwidth is less than that of the notch in the noise spectrum. The idle-channel noise (ICN) is measured with the noise band not notched and notched.^{1,2}

The theory behind the NPR test is that the incident noise outside the notch will cause reciprocal mixing noise and multiple IMD products, which will appear in the idle channel (the passband of the selective level meter) and raise the idle-channel noise. This test method is used in characterizing multi-channel frequency division multiplexing/frequency modulation systems (terrestrial microwave and satellite communications), where a notched noise band of equal bandwidth to the baseband is applied at the transmit end, and a receiver with a channel filter as wide as (or narrower than) the notch is used to measure idle-channel noise with and without the notch inserted in the noise band.

When testing an HF receiver, the receiver itself serves as the selective level meter. The test requires the IF bandwidth to be no wider than the bottom of the notch; the IF filter must not be wide enough to allow noise outside the notch to spill over into the IF. A bandpass (band-limiting) filter following the noise generator determines the total noise bandwidth. Figure 1 illustrates a typical noise band as defined by the band-limiting filter, with inserted notches as defined by the bandstop filters.

¹Notes appear on page 27

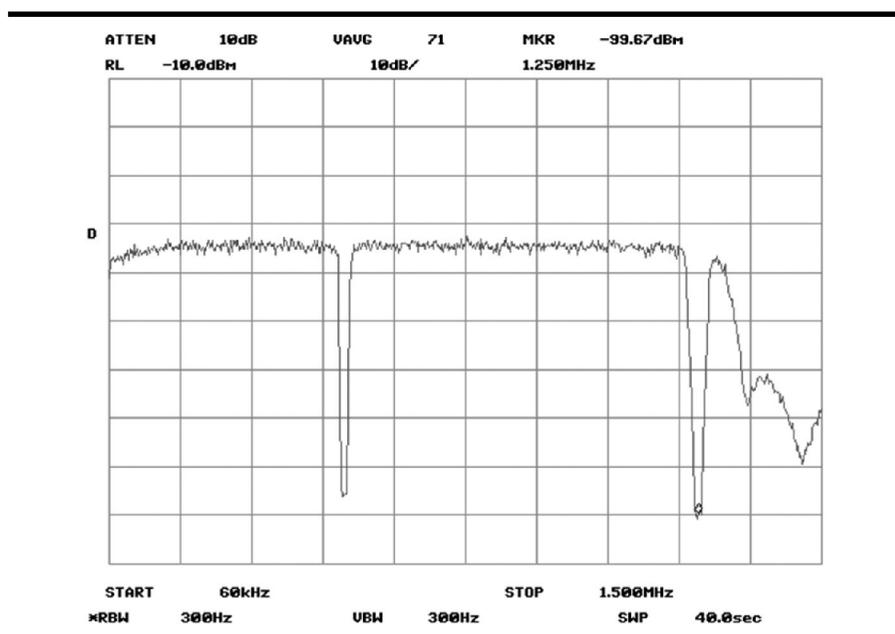


Figure 1 — Band-limiting filter response, including notches.

Advantages of NPR Testing

Standard receiver test methods involve applying single-tone or two-tone test signals to the receiver input, and measuring the degradation caused by these signals. This degradation may take the form of noise, IMD products, spurious responses and blocking (desensing). As these tests are performed under laboratory conditions, where the test signals are the only signals present, the effects of heavy band occupancy can be missed. Typical narrowband tests do not accurately reflect weak-signal performance degradation due to multiple strong signals

and the numerous undesired products they generate. As a result, a given receiver may have excellent narrowband “numbers,” yet may miss a weak signal on a crowded band.

The NPR test technique emulates a band filled with many strong signals by stressing the receiver with white noise. Thus, all possible combinations of carrier frequency spacing are taken into account — a true worst-case test. The test engineer can “zero in” on potential trouble spots by comparing NPR readings for various configurations such as RF preamplifier in/out, different IF filters, different preselectors, and so on. The NPR test will reveal passive IMD in filters and other components; narrowband tests

often do not apply sufficient power to the DUT to provoke passive IMD. In general, the higher the NPR value, the better the receiver's strong-signal handling.

When testing direct-sampling software defined radios, the NPR test has two additional advantages: first, it is possible to derive mathematically the theoretical maximum NPR value for an ADC having a given word length (number of bits). This is discussed in more detail later in the article. Second, the noise loading will be more than sufficient to dither the ADC, thus improving its IMD performance. This is especially useful when testing an SDR employing a high-speed ADC without on-chip dither.

It is felt that a combination of the NPR test and an interference-free signal strength (IFSS) test, in which the absolute power of IMD products generated by a two-tone test signal over a range of input power levels is compared to the band noise level at the DUT site, can be a very powerful tool for evaluating the performance of a direct-sampling SDR. A receiver in which the measured NPR approaches the calculated theoretical value can be viewed as performing optimally under heavy band occupancy.

Derivation of NPR; Noise-Bandwidth Considerations

NPR for a given noise bandwidth (or equivalent number of channels) is the ratio of the noise power in the notched band to the power in an equal bandwidth adjacent to the notch.

Gianfranco Verbana, I2VGO, has shown that for a given noise bandwidth, and at the optimum noise-loading point (see the **Determination of Optimum Noise Loading** section), Equation 1 describes the NPR.³

$$\text{NPR} = P_{\text{TOT}} - \text{BWR} - \text{MDS} \quad [\text{Eq 1}]$$

where:

P_{TOT} = total noise power in dBm in the noise bandwidth B_R

$$\text{BWR} = 10 \log_{10} (B_{\text{RF}}/B_{\text{IF}})$$

B_{RF} = RF bandwidth or noise bandwidth in Hz (RS-50 band-limiting filter)

B_{IF} = receiver IF filter bandwidth in Hz

MDS = minimum discernible signal (specified at B_{IF}). *This is a special case in which MDS is specified at the B_{IF} value used in the NPR test.*

This relationship can also be expressed as follows:

$$\text{NPR} = D_N + 10 \log_{10} B_{\text{IF}} - \text{MDS} \quad [\text{Eq 1A}]$$

where:

D_N = noise density in dBm/Hz = $P_{\text{TOT}} - 10 \log_{10} B_{\text{RF}}$

Note that noise density D_N is independent of RF bandwidth. The band-limiting filter selected for each test case should be *wider* than the front end of the DUT, to ensure that the NPR test subjects all stages of the receiver to noise loading, including any front-end filter or preselector. Thus, any effects

(such as passive IMD) that the incident noise generates in the front-end filter will be taken into account in the NPR measurement. These effects will show up as a *decrease* in NPR, as opposed to the increase expected if the preselector is narrower than the band-limiting filter in the instrument.

To put the impact of the NPR test into perspective, a -9 dBm P_{TOT} level at 5.6 MHz B_{RF} is equivalent to 1200 simultaneous SSB signals at -43 dBm each, or $S9 + 30$ dB!

Notch (Bandstop) Filter Design Considerations

1) The stopband width (notch width) at maximum attenuation must be greater than the IF bandwidth at which the receiver will be tested. It should also be wide enough to allow for any possible frequency drift in the filter.

2) The attenuation required in the stopband must be sufficient to prevent any direct transfer of noise to the receiver under test at its tuned frequency. Thus, if D_{TOT} is power spectral density (PSD) of the applied noise band in dBm/Hz, B_n is stopband width in Hz and A_n is stopband attenuation in dB, and MDS is the receiver's minimum discernible signal in dBm, the measuring system must satisfy Equation 2.

$$(D_{\text{TOT}} + 10 \log_{10} B_n) - A_n \leq \text{MDS} \quad [\text{Eq 2}]$$

Katz and Gray give a correction factor which should be applied if the measured NPR is close to the notch depth of the bandstop filter.⁴

$$\text{NPR} = -10 \log_{10} \left\{ 10^{-(\text{NPR}_m/10)} - 10^{-(A_n/10)} \right\} \quad [\text{Eq 3}]$$

where:

NPR_m is the measured NPR

A_n is the stopband attenuation of the bandstop filter.

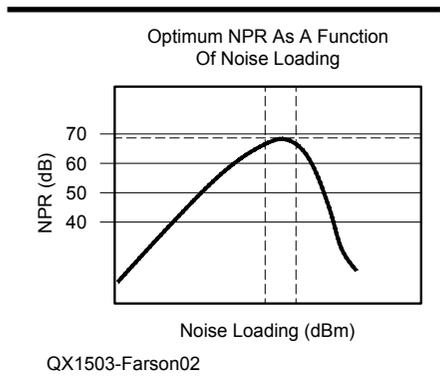


Figure 2 — Optimum NPR as a function of noise loading (embedded in image).

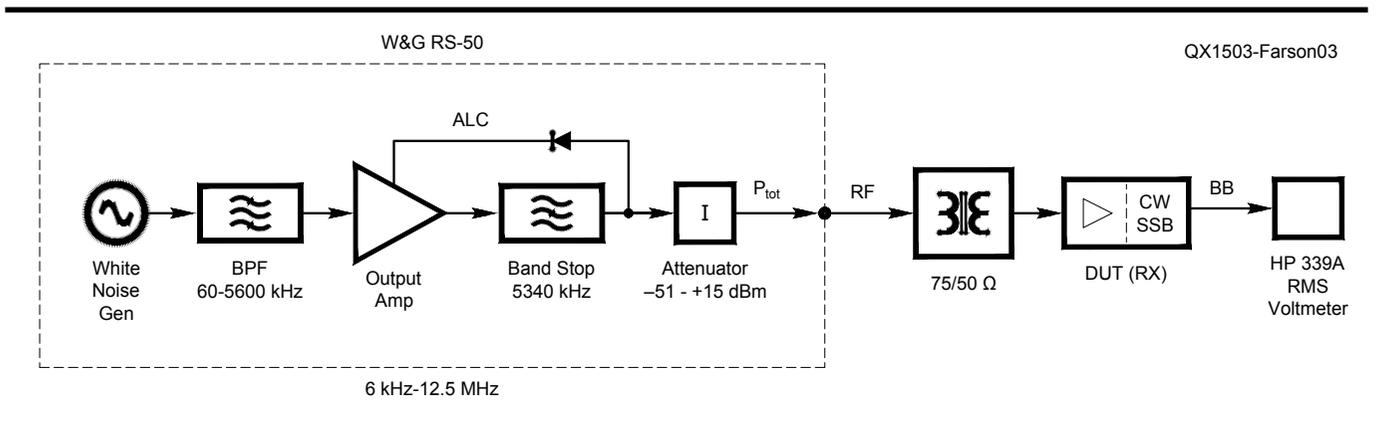


Figure 3 — Noise power ratio (NPR) measuring setup (embedded in image).

Determination of Optimum Noise Loading

Section 7.1 of the Marconi Instruments OA 2090 White Noise Test Set Operation and Maintenance Manual describes the NPR curve of a typical multi-channel transmission system as a function of noise loading.⁵ At low incident noise power levels, thermal noise is dominant, and NPR is roughly proportional to noise loading, where an increase of 1 dB increases NPR by ≈ 1 dB. This curve is also presented in Figure 2, and in Gianfranco Verbana's presentation, Slide 28. (See Note 3.)

As the noise loading level is further increased, the NPR increase is less than that in input power due to the effect of intermodulation (IMD) products. At a certain noise-loading level, IMD products begin to predominate over thermal noise and NPR starts to decrease. The turnover point is the "optimum noise loading level," at which the receiver NPR will be measured. In Verbana's presentation (Note 3), the optimum noise loading level is determined for each test case by increasing noise loading until idle-channel noise is 3 dB above the level when the noise generator is switched off (idle-channel noise at MDS). This greatly simplifies the measurement of NPR on receivers.

The NPR falls off rapidly at very high noise-loading levels. As Figure 2 shows, the slope on the right-hand side of the curve (noise loading > optimum value) is steeper, since the IMD products are dominant in this case.

Any direct transfer of noise due to the limited stopband attenuation of the notch filter will add to the IMD noise, thus reducing the optimum noise loading value. This effect will be negligible if the notch depth satisfies Equation 2, as is the case for the Wandel & Goltermann RS-50 White Noise Generator.

NPR Test Instrumentation

I was fortunate enough to locate a Wandel & Goltermann RS-50 White Noise

Generator on the surplus test-equipment market. This generator, together with its companion RE-50 noise receiver, forms the RK-50 NPR test system used for many years in the telecommunications industry. The RS-50 is illustrated in Figure 5.

The RS-50 generates a 6 kHz to 12.5 MHz noise band. Its output level is adjustable from -51 to $+15$ dBm. The instrument is fitted with three band-limiting filters and six bandstop filters covering CCITT (ITU-T) standard FDM baseband widths and test channel frequencies. In this example, the 5340 kHz bandstop filter is shown; its stopband width and attenuation are 3.3 kHz and ≈ 97 dB respectively. The RS-50 incorporates a precision attenuator (1 and 0.1 dB steps) and an ALC loop that holds the output constant at any level setting, irrespective of which filters are selected. Figure 3 illustrates the test setup for NPR testing of an HF receiver.

NPR Test Procedure for Conventional Receivers

1) Set the receive IF bandwidth/mode to 2.4 kHz SSB. Select SHARP shape factor (if applicable). *The IF bandwidth should be narrower than the stopband width of the notch filter.* Noise Blanker (NB), Noise Reduction (NR), Attenuator (ATT) and Preamp are all OFF. RF GAIN is at maximum. Select the 6 kHz roofing filter (if applicable), and set AGC to MID. Tune the DUT such that the IF passband is centered in the notch. If the DUT has a switchable preselector, this should be ON initially.

2) On the RS-50, set the RF attenuator to minimum (-50 dBm). Press and hold the GENERATOR BLOCKING key and adjust receiver AF GAIN for a 0 dBm reading on the RMS voltmeter connected to the baseband (audio) output.

3) On the RS-50, release the GENERATOR BLOCKING key. Adjust the attenuator for a $+3$ dBm reading on the RMS voltmeter.

Record the attenuator setting: this is P_{TOT} (total noise power).

4) Calculate NPR using Equation 1:

$$NPR = P_{TOT} - BWR - MDS \quad [\text{Eq 1}]$$

5) Repeat the test with different combinations of preselector, roofing filter and preamp, and record the results. Take each reading 2 to 3 times and average them for the highest accuracy. (Note: NPR cannot be read directly off the S-meter, because the S-meter reads S0 before the bottom of the notch is reached. Furthermore, very few conventional receivers have a calibrated S-meter.)

NPR Test Procedure for Direct-Sampling SDR Receivers

When testing NPR on a direct-sampling SDR receiver, the noise loading level required to raise the idle-channel noise by 3 dB may exceed the clipping (0 dBFS) point of the receiver ADC. (Gianfranco Verbana, I2VGO, has confirmed this behavior.) Thus, it is more convenient to increase the noise loading until the onset of clipping is reached, then back off the noise level until no clipping indication occurs for at least 10 seconds. (See Note 3, Slide 36.) NPR can then be read directly off the spectrum scope display or the signal-strength meter.

1) Set the receiver detection bandwidth/mode to 2.4 kHz SSB. Select the SHARP shape factor (if applicable). *The detection bandwidth should be narrower than the stopband width of the notch filter.* Noise Blanker (NB), Noise Reduction (NR), Attenuator (ATT), Dither and Preamp are all OFF. RF GAIN is at maximum. Set AGC to SLOW. Tune the DUT such that the detection channel passband is centered in the notch. If the DUT has a switchable preselector, this should be ON initially. Spectrum scope averaging should be ON, at mid-range.

2) On the RS-50, set the RF attenuator to minimum (-50 dBm). Press and hold the

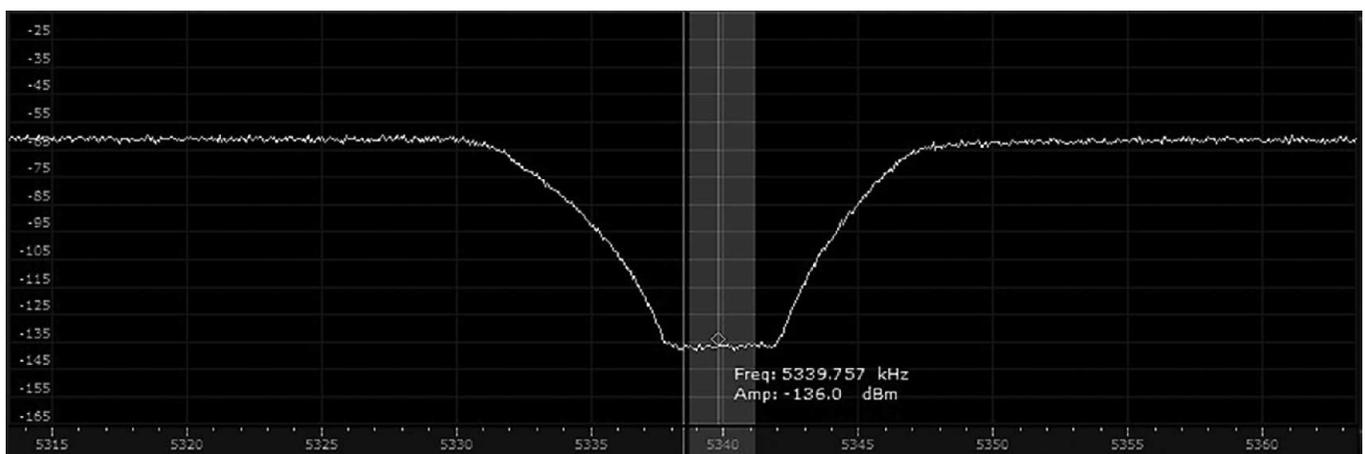


Figure 4 — NPR spectrogram on the Microtelecom Perseus spectrum scope.



Figure 5 — The Wandel & Goltermann RS-50 white noise generator.

GENERATOR BLOCKING key to turn off noise output, and read the MDS from the DUT signal-strength indicator or the bottom of the notch on the spectrum display. Record the MDS reading (in dBm).

3) On the RS-50, release the GENERATOR BLOCKING key. Adjust attenuator until ADC just clips, then back off until no clipping is observed over ≈ 10 seconds. Record the attenuator setting; this is P_{TOT} (total noise power). Read noise power from the DUT signal-strength indicator or the bottom of the notch on the spectrum display. Record the signal-strength reading (in dBm).

4) Now tune the DUT to a frequency well outside the notch and read the noise power on the signal-strength indicator. Record this signal-strength reading (in dBm).

5) NPR equals the difference between the signal-strength readings taken in steps 3 and 4.

6) Repeat the test with different combinations of preselector, dither and preamp, and record the results. Take each reading 2 to 3 times and average them for the highest accuracy.

7) Alternatively, NPR can be read off the spectrum display by positioning the marker well outside the notch and also in the center of the stopband. NPR is the difference between these two readings. See Figure 4.

NPR Test Frequencies and Capability

My Wandel & Goltermann RS-50 White Noise Generator has the following standard CCITT (ITU-T) filter sets:

- 1) 12 to 552 kHz band-limiting with 70, 240 and 534 kHz bandstop (LWBC. MWBC)
- 2) 60 to 1296 kHz band-limiting with 1248 kHz bandstop (MWBC)
- 3) 60 to 2044 kHz band-limiting with 1940 kHz bandstop (160 m)

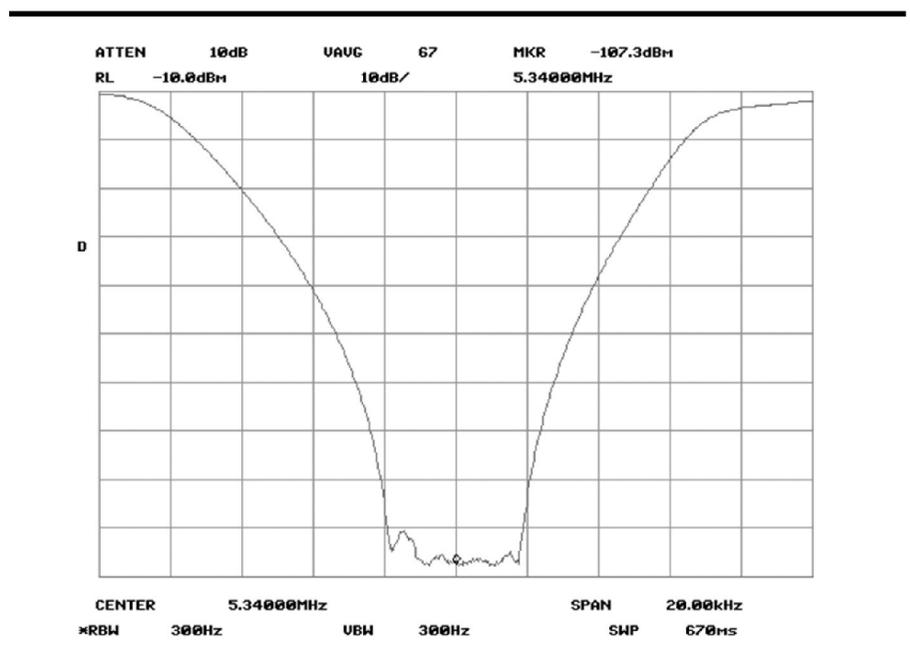


Figure 6 — Wandel & Goltermann 5340 kHz bandstop filter amplitude versus frequency response.

4) 60 to 2600 kHz band-limiting with 2438 kHz bandstop (120 m “tropical”)

5) 60 to 4100 kHz band-limiting with 3886 kHz bandstop (80 m)

6) 60 to 5600 kHz band-limiting with 5340 kHz bandstop (60 m)

7) 316 to 8160 kHz band-limiting with 7600 kHz bandstop (near 40 m)

These filters permit testing on multiple bands. The basic concept driving the choice of telecom-industry surplus NPR test equipment is the use of standard filters, which will ensure that the NPR test is repeatable when performed by other workers with standard test sets. The CCITT band-limiting filters concentrate the noise at and

below the band under test. Another rationale is that this equipment is quite inexpensive on the surplus market. The alternative, requiring a sophisticated digital arbitrary waveform generator, is extremely costly.

Measurement Results

I have made NPR measurements on a number of “analog” and DSP radios. The results of my current tests are presented in Table 1. As time and radios become available, I continue to test more radios, and update the NPR article on my website: www.ab4oj.com/test/docs/npr_test.pdf.

I have also tested a number of direct

Table 1
NPR Test Results, Analog/DSP Radios

<i>DUT</i>	<i>Config</i>	<i>MDS (dBm)</i>	<i>P_{TOT} (dBm)</i>	<i>BWR (dB)</i>	<i>NPR (dB)</i>		
IC-7700¹	Preamp off R15	-124	-11.6	33.6	78.5		
	R6		-4.8		83.3		
	R3		-4.9		83.1		
	Preamp 1 R15	-138	-24.6		79.5		
	R6		-14.8		87.3		
	R3		-14.8		87.3		
	Preamp 2 R15	-142	-29.7		78.4		
	R6		-22.4		83.7		
	R3		-22.5		83.6		
	Digisel R15	-123	-11.8		77.4		
	R6		-4.0		83.0		
	R3		-4.2		82.9		
	IC-7800²	Preamp off R15	-122		-8.7	33.6	79.4
		R6			-4.2		81.9
		R3			-1.2		82.0
Preamp 1 R15		-133	-23.3	75.5			
R6			-14.7	82.4			
R3			-12.1	82.0			
Preamp 2 R15		-137	-28.1	75.0			
R6			-23.5	77.6			
R3			-22.1	76.0			
Digisel R15		-122	-8.8	79.3			
R6			-1.5	84.6			
R3			-0.1	83.0			
TS-590S		Inband					
		Preamp Off	-125	-10.8	32.3		81.6
		Preamp On	-133	-19.5			81.0
TS-590S	High						
	Preamp Off	-126	-16	33.6	76		
	Preamp On	-134	-25.5		74.1		
K3 #1	K3 #1: 2.7 kHz 5-pole roofing filter fitted						
	Preamp off	-124	-9.7	33.6	80.4		
	Preamp on	-128	-14.0		80		
K3 #2	K3 #2: 2.8 kHz 8-pole roofing filter fitted						
	Preamp off	-124	-11.7	33.6	78.4		
	Preamp on	-129	-15.7		79.4		
IC-7600	Preamp off R15	-127	-14		33.6	79	
	R6		-12	81			
	R3		-12	81			
	Preamp 1 R15	-135	-25	77			
	R6		-22	79			
	R3		-22	79			
	Preamp 2 R15	-137	-27	76			
	R6		-25	78			
	R3		-26	77			
IC-7410	Preamp off R15	-129	-18	33.6	77.4		
	R6		-18.3		77.1		
	R3		-17		78.4		
	Preamp 1 R15	-136	-26.1		76.3		
	R6		-26		76.4		
	R3		-22.4		80		
	Preamp 2 R15	-139	-28.1		77.3		
	R6		-29.6		75.8		
	R3		-27.5		77.9		

<i>DUT</i>	<i>Config</i>	<i>MDS (dBm)</i>	<i>P_{TOT} (dBm)</i>	<i>BWR (dB)</i>	<i>NPR (dB)</i>	
IC-9100	Preamp off R15	-129	-17.8	33.6	77.6	
	R6		-17.8		77.6	
	R3		-17.7		77.7	
	Preamp 1 R15	-137	-26.3		77.1	
	R6		-25.9		77.5	
	R3		-25.4		78	
	Preamp 2 R15	-137	-27.8		75.6	
	R6		-26.6		76.8	
	R3		-25.9		77.5	
FT-950	IPO R15	-119	-11	33.6	74	
	R6		-11		74	
	R3		-9.2		76	
	AMP1 R15	-130	-21.4		74.7	
	R6		-19		77	
	R3		-18.4		77.7	
	AMP2 R15	-138	-28.4		75.7	
	R6		-27.4		76.7	
	R3		-26.8		77.3	
FTDX-1200³	IPO R15	-116.5	-7.7	33.6	74.9	
	R6		-8.2		76.4	
	R3		-8.7		77.9	
	AMP1 R15	-129	-22.7		72.4	
	R6		-22.9		74.2	
	R3		-23.5		75.6	
	AMP2 R15	-134	-31.2		68.9	
	R6		-31.6		71.5	
	R3		-31.8		72.3	
IC-7200	Preamp off	-124	-18	33.6	72.1	
	Preamp on	-135	-28		73.1	
FTDX-3000	Preamp off	-119	-12.7	33.6 ⁴	72.4	
	Preamp 1	-131	-27.3		69.8	
	Preamp 2	-134	-30.5		66.6	
FT-897D	Preamp off	-124	-18.7	34.0	71	
	Preamp on	-131	-31.7		65	
IC-703	Preamp off	-125	-21.8	33.6	69.6	
	Preamp on	-134	-30.4		70	
	Preamp off ATU in	-125	-21.8		69.6	
FT-1000	Preamp off	-124	-22	33.6	68	
	Preamp on	-132	-32		68	
IC-718 (#22)	Preamp off	-124	-21.6	33.6	68.5	
	Preamp on	-132	-32.1		66	
IC-706	Preamp off 2.4 kHz	-132	-31.1	33.6	67.4	
	Preamp on 2.4 kHz	-138	-37.3		67.1	
	Preamp off 1.8 kHz	-132	-30.9		34.9	66.2
	Preamp on 1.8 kHz	-138	-37.3		65.8	
IC-7000	Preamp off	-125	-24	33.6	67.0	
	Preamp on	-135	-37		64.3	
IC-7100	Preamp off	-124	-23.5	33.6	66	
	Preamp 1	-133	-35		64	
	Preamp 2	-135	-38		63	
FT-817	Preamp off	-125	-26.6	33.6	64.5	
	Preamp on	-130	-33.5		62.6	

Notes:

¹MDS shown for R15. Correction factors: R6: 2 dB. R3: 2 dB.

²MDS shown for R15. Correction factors: R6: 2 dB. R3: 5 dB.

³MDS shown for R15. Correction factors: R6: 1 dB. R3: 2 dB.

⁴With the 3 kHz 1st-IF roofing filter selected.

sampling SDR receivers, and those results are presented in Table 2. Again, I will test more radios as they become available and time permits. You can check my website for updated measurements.

Notes on the Theoretical Maximum NPR of an ADC

Walt Kester wrote “Noise Power Ratio (NPR) — A 65-Year Old Telephone System Specification Finds New Life in Modern Wireless Applications” as an Analog Devices Tutorial.⁶ In that tutorial, Figure 2, on page 3, gives the theoretical maximum NPR value of 74.01 dB for a 14-bit ADC. This value can be derived at the optimum noise loading point, where $B_{RF} = f_s / 2$, where f_s is the sampling frequency of the ADC, and assuming a perfect, noiseless ADC whose noise floor N_0 is given by Equation 4.

$$N_0 = (6 \times \text{no. of bits}) + 1.76 \quad [\text{Eq 4}]$$

$$N_0 = (6 \times 14) + 1.76 = 85.8 \text{ dBFS}$$

The noise floor of the LTC2206-14 ADC in the Microtelecom Perseus is 77 dBFS, which

is 8.8 dB worse than the theoretical maximum value. For the Perseus, $f_s = 80 \text{ MHz}$. An NPR test with $B_{RF} = f_s / 2 = 40 \text{ MHz}$, $B_{IF} = 2.4 \text{ kHz}$ (SSB mode) and the 5340 kHz bandstop filter yielded $\text{NPR} = 64.75 \text{ dB}$. This is 9.26 dB worse than the theoretical value, and is attributable to the finite noise floor of the ADC. This difference is comparable to the 8.8 dB difference in noise floor between the theoretical and “real-world” values.

Let us now derive the process gain, G_p , due to the presence of the band-limiting filter during the original NPR test.

$$G_p = 10 \log_{10}(f_s / (2 \times B_{RF})) = 10 \log_{10}(80 / (2 \times 5.537)) = 8.6 \text{ dB} \quad [\text{Eq 5}]$$

We can now predict NPR for the Microtelecom Perseus, as described above and presented in Table 2:

$$\text{NPR} = (\text{NPR for } B_{RF} = f_s / 2) + G_p = 64.75 \text{ dB} + 8.8 \text{ dB} = 73.55 \text{ dB} \quad [\text{Eq 6}]$$

Table 2 shows that the first measured NPR for the Perseus was 72 dB, well within the margin of error.

General Discussion of Results

In a conventional receiver, the effect of the high noise power outside the notch is twofold and most likely impacts the first and second mixers more than any of the downstream sections of the receiver. First, the incident noise mixes with the noise pedestal of the LO to cause reciprocal mixing, which shows up as increased noise in the IF passband (idle-channel noise). Second, the noise components mix with each other, the LO, any LO spurs and the LO phase noise to produce a very large number of IMD products — much closer to the effect of a heavily occupied band than a two signal test. Some of these IMD products will fall into the IF passband, further degrading idle-channel noise.

Secondary effects due to passive IMD in RF filter components, semiconductor filter switches, roofing filters, and other factors under the high noise loading will cause a further slight degradation in NPR. Slight passive IMD has been observed in some roofing filters under high noise loading.

In several of the conventional receivers

Table 2
NPR Test Results, Software Defined Radios (SDR)

DUT	SW Ver.	PreSel	Preamp	Dither	MDS (dBm)	Clip (dBm)	PTOT (dBm)	NPR (dB) ¹
ANAN100D	3.2.17	1		0	-123	-13	-22	76.5
				1	-123	-13	-21.5	73
ANAN200D Flex-6700	3.2.17 1.3.8	1 0 ²	0dB +10dB +20dB +30dB	0/1	-128	-16	-22	73
					-111	0	-1	75
					-118	-12	-13	71
					-130	-22	-23	71
					-134	-32	-33	68
Perseus	4.0b	0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0	-122	-3.6	-16.5	72
				1	-120	-3.6	-19.4	70
				0	-124	-7.1	-19.9	69
				1	-120	-7.1	-19.5	68
				0	-121	-1.5	-8.5	75
				1	-120	-1.5	-8.8	73
				0	-123	-5.0	-12.2	73
				1	-121	-5.0	-12.9	72
QS1R Rev. D	5.0.1.1		0 1	0 ³	-113	+11	-1	71
					-118	+7	-5	72
KX3	FW Ver. 1.10	BB Flt 0 1 0 1	Preamp 0 0 1 1		MDS dBm	BWR dB	P _{TOT} dBm	NPR dB ⁴
					-117	32.8	-11.5	72.4
					-116	33.7	-8.5	73.5
					-131	32.8	-25	72.9
				-130	33.7	-21.3	74.7	
ELAD FDM-S2	SW Ver. FDM-SW2		ATT 0		MDS dBm	BWR dB	P _{TOT} dBm	NPR dB ⁴
					-130	33.4	-19.5	71
SDR-IQ	SW Ver. 3.32		IF Gain +12dB +0dB					
					-103	33.6	-4.5	70
					-100		-4.5	64
Flex-1500	SW Ver. 2.7.2		Preamp 0 1		MDS dBm	BWR dB	P _{TOT} dBm	NPR dB ⁴
					-100	33.6	-16	55
					-111		-25	60

Notes

¹NPR value measured by observation.

²No preselector fitted for 5 MHz range.

³Enabling Dither and/or Random does not affect NPR.

⁴NPR calculated from P_{TOT} and BWR.

tested, the NPR improvement with narrower first IF roofing filters suggests that the second mixer is a significant contributor of IMD and/or reciprocal mixing noise when subjected to the higher noise loading with the 15 kHz roofing filter selected.

In a typical direct-sampling SDR, the best-case NPR was measured with preselector on, preamp off and dithering off. This suggests that the preselector is preventing the noise loading from driving the ADC input circuit into its non-linear region at levels approaching 0 dBFS.

If we apply the notched noise loading to a perfect (ideal) DUT which adds no noise, the notch depth at the DUT output will be the same as that shown in Figure 6. Any noise generated in the DUT will fill the notch with added noise, reducing its measured depth. Thus, the actual measured NPR is a measure of the amount of degradation due to reciprocal mixing and IMD noise generated by the notched noise load.

From Figure 6, assuming no added noise, the notch depth at a bandwidth of 3.3 kHz would be ≈ 97 dB. Thus, the NPR of an ideal receiver with <3.3 kHz Hz IF bandwidth would also be ≈ 97 dB. By this yardstick, a 70 to 80 dB measured NPR appears quite respectable. It will be interesting to correlate the results of the NPR test with those of the more familiar two signal IMD3 dynamic range measurement. (The passband curve in Figure 6 was taken using a spectrum analyzer and tracking generator.)

This article is intended as an introduction to the measurement techniques for noise power ratio testing of HF receivers. A lot of additional information has been written about this testing technique. Notes 7 through 12 provide some additional information and resources for interested readers.

Acknowledgements

I am indebted to Gianfranco Verbana, I2VGO, for sharing his research and providing the theoretical basis for the test procedure described in this article, to Henry Rech for his encouragement in embarking upon this project, and to Walter Salden, VE7WRS, for his invaluable assistance in building and characterizing the crystal notch filters used at an earlier stage of the project.

Adam M. Farson, VA7OJ/AB4OJ, was born in the UK, and raised and educated in South Africa. After earning a BSEE from the University of Cape Town, he worked in Racal, South Africa from 1964 to 1967 as an RF design engineer. He was involved in some interesting, advanced projects, such as a VHF FM/SSB tactical ground radio system for the Ministry of Defence, and also with a solid state HF transceiver for LMR ("bush radio") applications. They had a 25 W "man-pack" radio and a 100 W mobile radio, both of which used TV line-output transistors with an F, > 100 MHz in the transmitter PA and driver.

Adam emigrated from South Africa in 1967, and then spent three years at CERN as an RF design engineer, working on a modulation system for a 10 kW 9.5 MHz power generator feeding RF power to a proton accelerator. This project served as the thesis for his Masters degree in EE from the University of Cape Town in 1971.

After his time at CERN, Adam returned to the telecommunications industry and worked for various multinational corporations in the satellite and wireline telecommunications fields, culminating in a 20 year stay as a systems engineer at Siemens. He was based in Boca Raton, Florida, but traveled extensively to North American and International assignments, including a year in Munich and several months in Tokyo. His main responsibilities were systems verification and compliance engineering, mainly in the areas of telephone trunking, signalling, and transmission.

He retired at the end of 1999 and moved to British Columbia. He holds a Canadian Advanced Amateur Radio Certificate (VA7OJ) and a US Amateur Extra class license (AB4OJ) as well as an FCC General Radiotelephone Operator's License. He was first licensed in 1962 as ZS1ZG. He enjoys applying some of his engineering training to Amateur Radio, especially in the area of radio equipment testing. After retiring he started building a comprehensive RF laboratory, and began researching noise power ratio testing of receivers in 2009. You can find more information about Adam and his Amateur Radio interests on his personal webpage: www.ab4oj.com/.

Notes

¹Wes Hayward, W7ZOI, "Oscillator Noise Evaluation with a Crystal Notch Filter," QEX, July/August 2008, pp 6 – 12.

²"Compare Receivers," Microwaves & RF, January 1987, pp 104 – 108.

³Gianfranco Verbana, I2VGO, "Measurement of All Intermodulation Products on HF Receivers, With 24000 CW Tones," 11th RENON Convention, Costalovara (Italy), 26-27 September, 2009. A copy of this paper is available on the Internet: www.woodboxradio.com/download/Final_report_VGO_Renon_2009.pdf.

⁴Allen Katz and Robert Gray, "Noise Power Ratio Measurement Tutorial," Linearizer Technology Inc. This tutorial is available on the Linearizer Technology website: www.lintech.com/PDF/npr_wp.pdf.

⁵Marconi Instruments OA 2090 White Noise Test Set Operation & Maintenance Manual, 1971.

⁶Walt Kester, "Noise Power Ratio (NPR) — A 65-Year Old Telephone System Specification Finds New Life in Modern Wireless Applications," Analog Devices Inc Tutorial MT-005, 2009. This tutorial is available on the Analog Devices website: www.analog.com/static/imported-files/tutorials/MT-005.pdf.

⁷J. N. Dingley (Racal), "An Introduction to White Noise Testing of HF Receivers," IERE Conference on Radio Receivers and Associated Systems, No. 24, July 1972.

⁸M. J. Tant, "Multichannel Communication Systems and White Noise Testing," Marconi Instruments Ltd, July 1974.

⁹Fred H. Irons, "The Noise Power Ratio — Theory and ADC Testing," IEEE Transactions on Instrumentation and Measurement, Vol 49, No. 3, June 2000, pp. 659 – 665.

¹⁰"Improved Methods for Measuring Distortion in Broadband Devices," Application Note 5989-9880EN, December 2008, Agilent

Technologies Inc. This Application Note is available on the Agilent Technologies website: cp.literature.agilent.com/litweb/pdf/5989-9880EN.pdf.

¹¹Adam M. Farson, VA7OJ/AB4OJ, "Noise Power Ratio (NPR) Testing of HF Receivers," Radio Society of Great Britain, RadCom, December 2012, pp 42 – 45.

¹²Adam M. Farson, VA7OJ/AB4OJ, "Noise Power Ratio Testing," presentation to North Shore Amateur Radio Club, North Vancouver, BC, 22 November 2012. A copy of this presentation is available at: www.nsrc.ca/hf/npr.pdf.

Appendix

Suggested NPR test equipment:

1) Wandel & Goltermann RS-25, RS-50 or RS-100 noise generator, with band-limiting and bandstop filters.

2) Marconi TF2091B or C with LPF/HPF pairs, equivalent to Wandel & Goltermann band-limiting and bandstop filters.

These instruments can be found on popular auction sites or at used/surplus test equipment vendors/brokers. The Marconi test sets are generally more plentiful, as they were widely used by the Telecommunications companies and the military.

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Wire Antennas for 80 Meter DXing

The author looks at a variety of antenna configurations with low takeoff angle radiation patterns.

My friend Chuck, KA1PM, lives in the Texas hill country, and he is interested in working DX on 80 meters in order to qualify for 5 Band DXCC. He already has a 200 foot tower, which supports directional antennas for the bands from 40 through 10 meters, but he was looking for a wire antenna that would put out a strong low-angle signal on the 80 meter band. The tower “real estate” above a height of 180 feet was already occupied, but any type of simple antenna (or array) that could be installed at an elevation of 180 feet or less was eligible for consideration.

This article illustrates some of the antennas that we reviewed, along with the performance parameters for each one. Propagation studies carried out by Dean Straw, N6BV, indicate that the optimum arrival and takeoff angles for DX signals to and from the US on 80 meters are probably less than 10° in most cases, although angles up to about 30° are sometimes useful.¹

Each of the antennas described here was simulated on the computer using the EZNEC software package, which is available from Roy Lewallen, W7EL.² For simplicity, I created a “stick” model of a 180 foot tower, which includes an 8 foot ground rod at its base. All conductors are #12 copper, and the ground constants for “average” soil (conductivity = 0.005 Siemens/meter and dielectric constant = 13) were inserted into the model. The operating frequency is held fixed at 3650 kHz.

Single Inverted V Dipole

The first antenna that I analyzed is a classic half-wave inverted V dipole with the apex at H = 180 feet. Each leg has a length of 66 feet, and slopes downward at an angle of 30° below horizontal. The main

operating parameters are listed in Table 1. Figures 1 and 2 display the principal elevation- and azimuth-plane radiation patterns, respectively. This simple antenna generates a lot of gain at low takeoff angles,

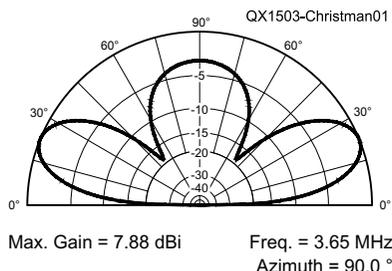


Figure 1 — Elevation-plane radiation pattern of a half-wave inverted V dipole antenna with the apex at H = 180 feet, operating at f = 3650 kHz. Peak gain = 7.88 dBi at a takeoff angle of 22.4°.

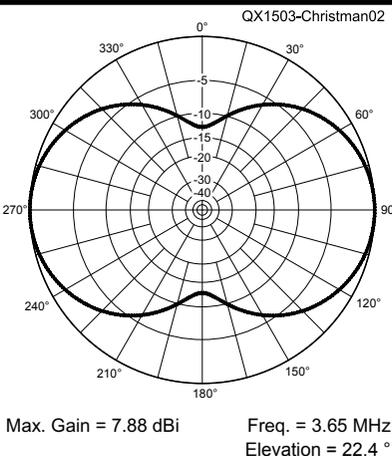


Figure 2 — Azimuth-plane radiation pattern of a half-wave inverted V dipole antenna with the apex at H = 180 feet, when f = 3650 kHz. Peak gain = 7.88 dBi at a takeoff angle of 22.4°, and half-power beamwidth = 85.4°.

but has a large high-angle lobe, which may be undesirable under certain conditions. The half-power beamwidth in the azimuth plane is just over 85°, which means that a second identical inverted V, when installed at right angles to the first one, could provide good coverage of most compass directions.

Pair of Inverted V Antennas Stacked Vertically

One way to reduce the size of the high-angle radiation lobe that is generated by the lone inverted V is to place a second identical antenna directly beneath it, at an apex height of 90 feet, and then feed both of them with equal-magnitude in-phase currents. This strategy yields the radiation patterns shown in Figures 3 and 4, while the performance data is listed in Table 2. Although the high-angle lobe in the elevation-plane pattern is now much smaller than before, the low-angle gain is not as great as previously, being about 1.65 dB lower at a 5° takeoff angle. The azimuth-plane beamwidth has now widened to 90.4°, which is about 5° more than before. Feeding just the upper inverted V (with the input terminals of the lower antenna open-circuited) again produces a radiation pattern that is very similar to that for the system that uses just a single inverted V by itself (peak gain here = 7.84 dBi at a takeoff angle of 22.3°). Figure 5 shows the pattern for this configuration.

Two more feed methods can be employed with this array, as follows. When driving both antennas again, but this time using equal-magnitude out-of-phase currents, a large lobe of radiation directly overhead will result, with a peak gain of 9.20 dBi at a takeoff angle of 90°. Finally, if only the lower inverted V is fed (with the input terminals of the upper antenna open-circuited) this produces a radiation pattern at an intermediate elevation,

¹Notes appear on page 35.

Table 1

Performance of a half-wave inverted V dipole antenna designed for operation on the 80-meter band at a frequency of 3650 kHz. Each leg has a length of 66 feet and slopes downward at an angle of 30° below horizontal. The antenna is constructed from #12 AWG copper wire, and its apex is placed at a height of 180 feet. The soil is “average,” with a conductivity of 0.005 Siemens per meter and a dielectric constant of 13.

Parameter	Value
Input impedance	51.47 + j 0.465 Ω
Peak gain and takeoff angle	7.88 dBi at 22.4°
Gain at 5° takeoff angle	-0.98 dBi
Gain at 10° takeoff angle	4.34 dBi
Gain at 15° takeoff angle	6.78 dBi
Gain at 20° takeoff angle	7.78 dBi
Gain at 25° takeoff angle	7.76 dBi
Gain at 30° takeoff angle	6.87 dBi
Gain at 35° takeoff angle	5.07 dBi
Azimuth-plane	
half-power beamwidth	85.4°
Azimuth-plane gain at 45° away from bore-sight	4.54 dBi (-3.34 dB _{max})

Table 2

Performance of a pair of vertically-stacked half-wave inverted V dipole antennas designed for operation on the 80 meter band at a frequency of 3650 kHz. The upper antenna has its apex at H = 180 feet, while the apex of the lower one is at a height of 90 feet. Both antennas are fed with equal-magnitude in-phase currents.

Parameter	Value
Input impedances	67.86 - j 39.35 Ω (Upper Antenna) 93.07 - j 36.74 Ω (Lower Antenna)
Peak gain and takeoff angle	7.48 dBi at 26.8°
Gain at 5° takeoff angle	-2.63 dBi
Gain at 10° takeoff angle	2.84 dBi
Gain at 15° takeoff angle	5.52 dBi
Gain at 20° takeoff angle	6.90 dBi
Gain at 25° takeoff angle	7.44 dBi
Gain at 30° takeoff angle	7.37 dBi
Gain at 35° takeoff angle	6.80 dBi
Azimuth-plane	
half-power beamwidth	90.4°
Azimuth-plane gain at 45° away from bore-sight	4.51 dBi (-2.97 dB _{max})

Table 3

Performance of a two-element phased array of half-wave inverted V dipole antennas designed for operation on the 80 meter band at a frequency of 3650 kHz. The elements are spaced 45° apart (33.7 feet), one in front of the other, with an apex height of 180 feet. The relative currents into the two feed points are: $I_{front} = 1 \angle -135^\circ$ and $I_{back} = 1 \angle 0^\circ$.

Parameter	Value
Input impedances	20.36 + j 29.69 Ω (Front Antenna) 21.79 - j 31.61 Ω (Back Antenna)
Peak gain and takeoff angle	11.5 dBi at 21.7°
Front-to-back ratio	22.13 dB
Gain at 5° takeoff angle	2.88 dBi
Gain at 10° takeoff angle	8.17 dBi
Gain at 15° takeoff angle	10.54 dBi
Gain at 20° takeoff angle	11.44 dBi
Gain at 25° takeoff angle	11.31 dBi
Gain at 30° takeoff angle	10.27 dBi
Gain at 35° takeoff angle	8.29 dBi
Azimuth-plane	
half-power beamwidth	74.4°
Azimuth-plane gain at 45° away from bore-sight	7.05 dBi (-4.45 dB _{max})

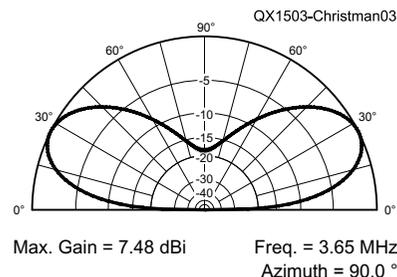


Figure 3 — Elevation-plane radiation pattern for a pair of half-wave inverted V antennas with apex heights of 90 and 180 feet, operating at $f = 3650$ kHz, when both are fed with equal-amplitude in-phase currents. Peak Gain = 7.48 dBi at a takeoff angle of 26.8°.

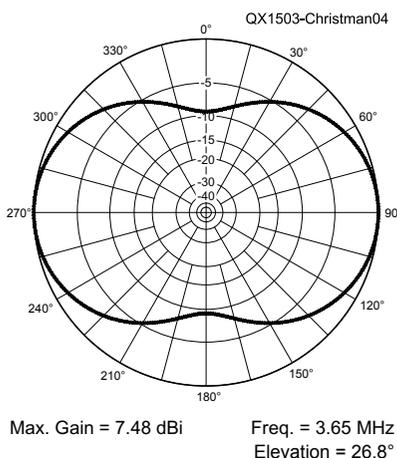


Figure 4 — Azimuth-plane radiation pattern for a pair of half-wave inverted V antennas with apex heights of 90 and 180 feet, operating at $f = 3650$ kHz, when both are fed with equal-amplitude in-phase currents. The elevation angle is 26.8° with a peak gain of 7.48 dBi. The half-power beamwidth = 90.4°.

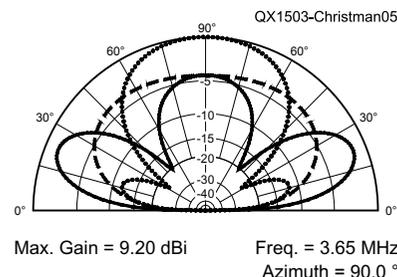


Figure 5 — Elevation-plane radiation patterns for a pair of half-wave inverted V antennas with apex heights of 90 and 180 feet, operating at $f = 3650$ kHz. When the upper antenna is driven, and the lower antenna is open-circuited: Peak Gain = 7.84 dBi at a takeoff angle of 22.3° (solid trace). When both are fed with equal-amplitude out-of-phase currents: Peak Gain = 9.20 dBi at a takeoff angle of 21.7° (dotted trace) When the lower antenna is driven, and the upper antenna is open-circuited: Peak Gain = 5.60 dBi at a takeoff angle of 52.3° (dashed trace)

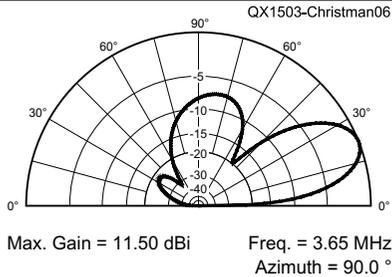


Figure 6 — Elevation-plane radiation pattern for a two-element phased array made from half-wave inverted V antennas designed for operation on the 80 meter band at a frequency of 3650 kHz. The elements are spaced 45° apart (33.7 feet), one in front of the other, with an apex height of 180 feet. The relative currents into the feed points are: $I_{front} = 1 \angle -135^\circ$ and $I_{back} = 1 \angle 0^\circ$. The peak gain is 11.5 dBi at a takeoff angle of 21.7°. Front-to-back ratio = 22.13 dB.

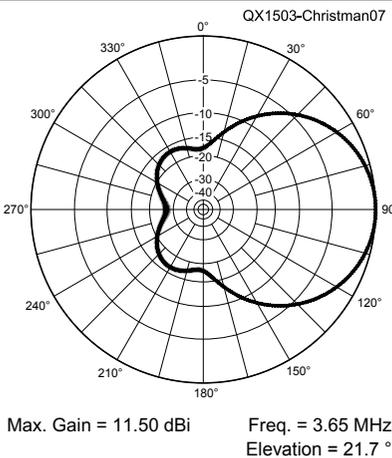


Figure 7 — Azimuth-plane radiation pattern for a two-element phased array made from half-wave inverted V antennas designed for operation on the 80 meter band at a frequency of 3650 kHz. The elements are spaced 45° apart (33.7 feet), one in front of the other, with an apex height of 180 feet. The relative currents into the feed points are: $I_{front} = 1 \angle -135^\circ$ and $I_{back} = 1 \angle 0^\circ$. The peak gain is 11.5 dBi at an elevation angle of 21.7°. The half power beamwidth is 74.4°.

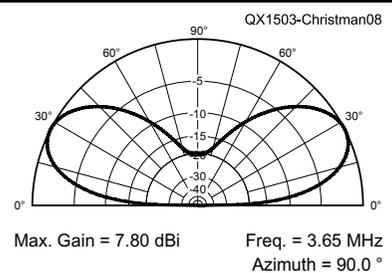


Figure 8. Elevation-plane radiation pattern for a full-wavelength cubical quad antenna designed for operation on the 80-meter band at a frequency of 3650 kHz. Each side has a length of 70.75 feet and all of the interior angles are equal to 90°. The apex is placed at a height of 180 feet, with the lower corner at an approximate height of 80 feet. Peak gain = 7.81 dBi at a takeoff angle of 27.1°.

where the peak gain is 5.60 dBi at a takeoff angle of 52.3°. These two radiation patterns are also included in Figure 5.

Phased Array of Inverted V Elements

To achieve a unidirectional radiation pattern, two identical inverted V s can be placed at the same height, one in front of the other, with both fed in phase to create a simple end-fire array. A spacing of 45° will be used, and the element currents will be equal in magnitude but 135° out of phase ($I_{front} = 1 \angle -135^\circ$ and $I_{back} = 1 \angle 0^\circ$). At an operating frequency of 3650 kHz, the required element spacing is 33.7 feet, which is fairly large but manageable. Of course, wider spacing and smaller current phase-lags could also be used. The apex height is still 180 feet for both inverted Vs, with each element leg having a length of 66 feet and sloping downward at an angle of 30° below horizontal.

Table 3 lists information about the performance of the array, while the radiation patterns are given in Figures 6 and 7. This system has the highest gain of all the antennas that were examined in this study, but it also has the narrowest beamwidth in the azimuth plane. Being unidirectional, provision must be made to swap the drive currents into the feed points of the two elements in order to switch the direction of fire. Two of these arrays could be stacked if desired, with the second one at a height of perhaps 90 feet, in order to suppress the high-angle lobe of radiation (and to provide a selection of takeoff angles).

Cubical Quad Antenna

A large single-element antenna that fits well on this tower is the full-wavelength cubical quad, installed in a diamond

configuration. This one is perfectly square in shape, and each side has a length of 70 feet 9 inches. The apex is at H = 180 feet, with the bottom corner at an approximate height of 80 feet. The quad is fed at the bottom, which produces horizontal polarization. The elevation- and azimuth-plane radiation patterns are displayed in Figures 8 and 9, and the performance parameters are listed in Table 4. Compared to a single inverted V with its apex at the same height, the quad has less gain at very low takeoff angles, but there is no high-angle radiation lobe in the pattern, and most of the signal energy is concentrated below a 45° takeoff angle.

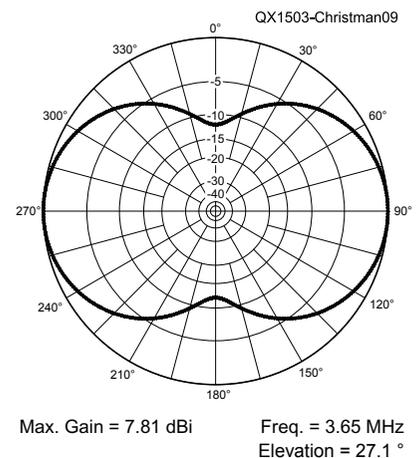


Figure 9 — Azimuth-plane radiation pattern for a full-wavelength cubical quad antenna designed for operation on the 80 meter band at a frequency of 3650 kHz. Each side has a length of 70.75 feet and all of the interior angles are equal to 90°. The apex is placed at a height of 180 feet, with the lower corner at an approximate height of 80 feet. The peak gain is 7.81 dBi at an elevation angle of 27.1°. The half-power beamwidth = 88.0°

Table 4

Performance of a full-wavelength cubical quad antenna designed for operation on the 80 meter band at a frequency of 3650 kHz. Each side has a length of 70.75 feet and all of the interior angles are equal to 90°. The antenna is constructed from #12 AWG copper wire, and its apex is placed at a height of 180 feet, with the lower corner at an approximate height of 80 feet.

Parameter	Value
Input impedance	129.5 - j0.878 Ω
Peak gain and takeoff angle	7.81 dBi at 27.1°
Gain at 5° takeoff angle	-2.43 dBi
Gain at 10° takeoff angle	3.05 dBi
Gain at 15° takeoff angle	5.76 dBi
Gain at 20° takeoff angle	7.17 dBi
Gain at 25° takeoff angle	7.75 dBi
Gain at 30° takeoff angle	7.72 dBi
Gain at 35° takeoff angle	7.17 dBi
Azimuth-plane half-power beamwidth	88.0°
Azimuth-plane gain at 45° away from bore-sight	4.67 dBi (-3.14 dB _{max})

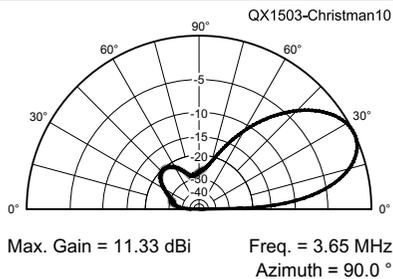


Figure 10 — Elevation-plane radiation pattern for a two-element phased array made from 1 λ quad loops, designed for operation on the 80 meter band at a frequency of 3650 kHz. The elements are spaced 45° apart (33.7 feet), one in front of the other, with an apex height of 180 feet. The relative currents into the feed points are: $I_{front} = 1 \angle -135^\circ$ and $I_{back} = 1 \angle 0^\circ$. The peak gain = 11.33 dBi at a takeoff angle of 25.8°. The front-to-back ratio = 20.20 dB

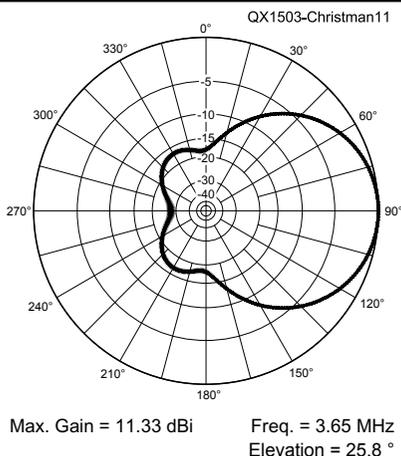


Figure 11 — Azimuth-plane radiation pattern for a two-element phased array made from 1 λ quad loops, designed for operation on the 80 meter band at a frequency of 3650 kHz. The elements are spaced 45° apart (33.7 feet), one in front of the other, with an apex height of 180 feet. The relative currents into the feed points are: $I_{front} = 1 \angle -135^\circ$ and $I_{back} = 1 \angle 0^\circ$. The peak gain = 11.33 dBi at an elevation angle of 25.8°. The half-power beamwidth = 75.7°.

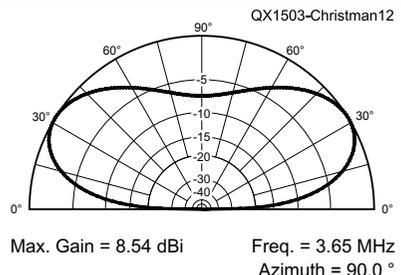


Figure 12 — Elevation-plane radiation pattern for a 2 λ bisquare antenna designed for operation on the 80 meter band at a frequency of 3650 kHz. Each side has a length of 134 feet, and all of the interior angles are equal to 90°. The apex is placed at a height of 180 feet, with the lower corner at a height of 11 feet 4 inches. The antenna is open-circuited at the top and fed at the bottom. The peak gain = 8.54 dBi at a takeoff angle of 31.8°.

Phased Array of Cubical-Quad Elements

Two identical quad elements can easily be combined to create a unidirectional end-fire array, just as was done earlier with a pair of inverted Vs. Once again, a spacing of 45° will be used, with a phase angle of 135° between the two element currents, which are equal in magnitude ($I_{front} = 1 \angle -135^\circ$ and $I_{back} = 1 \angle 0^\circ$). Spacing between the two quad loops is 33.7 feet for an operating frequency of 3650 kHz. The apex height remains at 180 feet for both elements, with all side lengths equal to 70.75 feet.

Details on the performance of this array are shown in Table 5, and the radiation patterns are included in Figures 10 and 11. The peak forward gain at very low takeoff angles is somewhat inferior to that of a

similar phased array that uses inverted V elements, but the antenna has a very clean radiation pattern, with no high-angle lobe in the elevation plane.

Bisquare

This interesting antenna design was suggested to me by Joe Johnson, K3RR, who is an avid low-band DXer. At first glance, the bisquare antenna looks exactly like a diamond-shaped cubical quad, but there are two important differences. First, the distance around the loop is two full wavelengths, instead of just one. Each side has a length of about 134 feet at an operating frequency of 3650 kHz. Second, the loop is not closed, but is open-circuited at the top, with the feed point at the bottom, where the input impedance is quite high.

Table 5

Performance of a two-element phased array of full-wavelength cubical-quad antennas designed for operation on the 80-meter band at a frequency of 3650 kHz. Each loop has a side-length of 70 feet 9 inches. The elements are spaced 15° apart (33.684 feet), one in front of the other, with an apex height of 180 feet. The relative currents into the two feed points are: $I_{front} = 1 \angle -135^\circ$ and $I_{back} = 1 \angle 0^\circ$.

Parameter	Value
Input impedances	129.9 + j 146.2 Ω (Front Antenna) - 25.3 + j6.63 Ω (Back Antenna)
Peak gain and takeoff angle	11.33 dBi at 25.8°
Front-to-back ratio	20.20 dB
Gain at 5° takeoff angle	1.47 dBi
Gain at 10° takeoff angle	6.91 dBi
Gain at 15° takeoff angle	9.55 dBi
Gain at 20° takeoff angle	10.87 dBi
Gain at 25° takeoff angle	11.33 dBi
Gain at 30° takeoff angle	11.13 dBi
Gain at 35° takeoff angle	10.40 dBi
Azimuth-plane half-power beamwidth	75.7°
Azimuth-plane gain at 45° away from bore-sight	7.02 dBi (- 4.31 dB _{max})

Table 6

Performance of a 2 λ bisquare antenna designed for operation on the 80 meter band at a frequency of 3650 kHz. Each side has a length of 134 feet, and all of the interior angles are equal to 90°. The antenna is constructed from #12 AWG copper wire, and its apex is placed at a height of 180 feet, with the bottom corner at an approximate height of 11 feet 4 inches.

Parameter	Value
Input impedance	3486 - j 3.06 Ω
Peak gain and takeoff angle	8.54 dBi at 31.8°
Gain at 5° takeoff angle	-2.80 dBi
Gain at 10° takeoff angle	2.77 dBi
Gain at 15° takeoff angle	5.63 dBi
Gain at 20° takeoff angle	7.27 dBi
Gain at 25° takeoff angle	8.16 dBi
Gain at 30° takeoff angle	8.51 dBi
Gain at 35° takeoff angle	8.47 dBi
Azimuth-plane half-power beamwidth	62.8°
Azimuth-plane gain at 45° away from bore-sight	2.36 dBi (- 6.18 dB _{max})

Figures 12 and 13 present the radiation-pattern plots, and the key performance parameters appear in Table 6. Peak gain for this antenna occurs at a takeoff angle of almost 32° (the feed point is only slightly more than 11 feet above the ground), although there is no high-angle lobe of radiation. The half-power beamwidth in the azimuth plane is smaller than what we're accustomed to seeing (less than 63°), but the

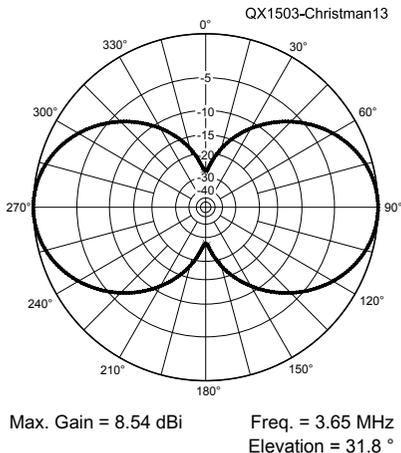


Figure 13 — Azimuth-plane radiation pattern for a 2λ bisquare antenna designed for operation on the 80 meter band at a frequency of 3650 kHz. Each side has a length of 134 feet and all of the interior angles are equal to 90°. The apex is placed at a height of 180 feet, with the lower corner at a height of just over 11 feet. The peak gain = 8.54 dBi at an elevation angle of 31.8°. The half-power beamwidth = 62.8°.

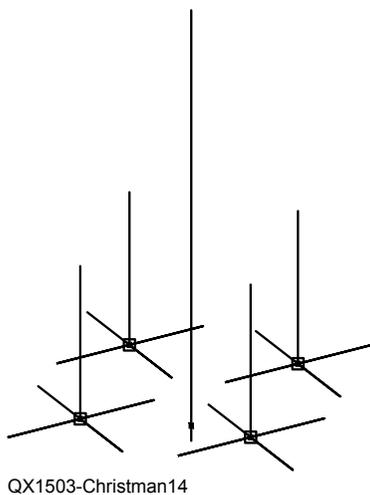


Figure 14 — Computer-generated drawing of the elevated Four-Square wire array, along with the 180 foot tower in the center. There is an 8 foot buried ground rod at the base of the tower. Each element of the array has a vertical monopole that is 66 feet tall, along with four horizontal radials that are 33 feet long. The base-height of each element is 15 feet.

front-to-side ratio is much larger than usual.

Notice that, if the loop was “closed” at the top, then this antenna could also serve as a conventional quad for use on the 160 meter band. Peak gain would occur at a high takeoff angle, however, because of the antenna’s low height above ground.

Elevated Four-Square Array

With 180 feet of tower height available, a number of different phased-vertical arrays could be installed, employing catenary ropes hung from the tower to support the wire

elements of the various antennas. Figure 14 is a computer-generated drawing of an elevated Four-Square array that uses quarter-wave vertical monopoles (length = 66 feet) whose base height is set at 15 feet. Each element has four elevated 1/8 λ radials (length = 33 feet) whose inner ends are connected together in series with an inductor ($L = 6.523 \mu\text{H}$) to provide resonance at 3650 kHz. The square itself has the usual side-length of 1/4 λ, and normal driving-point currents are applied ($I_{\text{front}} = 1 \angle -180^\circ$, $I_{\text{side}} = 1 \angle -90^\circ$ and $I_{\text{back}} = 1 \angle 0^\circ$).

Table 7

Performance of an elevated Four-Square phased-vertical array designed for operation on the 80-meter band at a frequency of 3650 kHz. Each monopole has a length of 66 feet, and includes four 1/8 λ elevated radials (length = 33 feet). The antenna is constructed from #12 AWG copper wire, and the base height of each element is 15 feet. The array utilizes progressive current phase-shifts between the elements, and each side of the square has a length of 1/4 λ (66 feet).

Parameter	Value
Input impedance	55.64 + j 43.41 Ω (Front Element) 37.26 – j 13.73 Ω (Side Elements) 5.65 – j 16.04 Ω (Back Element)
Peak gain and takeoff angle	5.14 dBi at 20.7°
Front-to-back ratio	20.18 dB
Gain at 5° takeoff angle	0.15 dBi
Gain at 10° takeoff angle	3.56 dBi
Gain at 15° takeoff angle	4.78 dBi
Gain at 20° takeoff angle	5.13 dBi
Gain at 25° takeoff angle	4.99 dBi
Gain at 30° takeoff angle	4.49 dBi
Gain at 35° takeoff angle	3.72 dBi
Azimuth-plane half-power beamwidth	98.7°
Azimuth-plane gain at 45° away from bore-sight	2.67 dBi (– 2.47 dB _{max})

Table 8

Performance of an elevated Four-Square phased array of 1/2 λ elements, designed for operation on the 80 meter band at a frequency of 3650 kHz. Each vertical dipole has a length of 132 feet, and is constructed from #12 AWG copper wire. The bottom ends of the elements are at H = 15 feet, with the tops at H = 147 feet. The array uses progressive 90° current phase shifts between the elements, and each side of the square has a length of 1/4 λ (66 feet).

Parameter	Value
Input impedance	143.9 + j 125.9 Ω (Front Element) 92.65 – j 27.3 Ω (Side Elements) 12.7 – j 28.35 Ω (Back Element)
Peak gain and takeoff angle	5.81 dBi at 15.4°
Front-to-back ratio	22.37 dB
Gain at 5° takeoff angle	1.95 dBi
Gain at 10° takeoff angle	5.07 dBi
Gain at 15° takeoff angle	5.80 dBi
Gain at 20° takeoff angle	5.45 dBi
Gain at 25° takeoff angle	4.37 dBi
Gain at 30° takeoff angle	2.69 dBi
Gain at 35° takeoff angle	0.45 dBi
Azimuth-plane half-power beamwidth	98.0°
Azimuth-plane gain at 45° away from bore-sight	3.30 dBi (– 2.51 dB _{max})

The important performance data is given in Table 7, while the radiation patterns are revealed in Figures 15 and 16. This array does not provide as much peak gain as the antennas described previously, but it concentrates most of the signal at very low takeoff angles. In addition, the half-power beamwidth of the main lobe is broad enough to provide good coverage of all compass directions using only four directions of fire. Of course, the input currents can be reconfigured to make the array fire through the sides of the square (instead of through the corners), if desired.

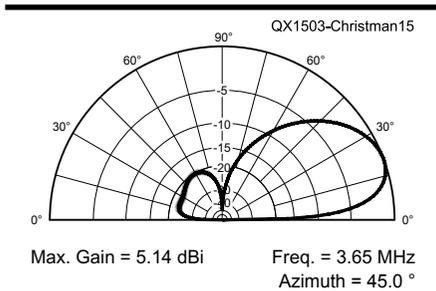


Figure 15 — Elevation-plane radiation pattern for the Four-Square array shown in Figure 14. The antenna is designed for operation on the 80 meter band at a frequency of 3650 kHz. Each side of the square has a length of $\frac{1}{4} \lambda$ (66 feet). The relative currents into the feed points are: $I_{front} = 1 \angle -180^\circ$, $I_{side} = 1 \angle -90^\circ$, and $I_{back} = 1 \angle 0^\circ$. The peak gain = 5.14 dBi at a takeoff angle of 20.7° . The front-to-back ratio = 20.18 dB.

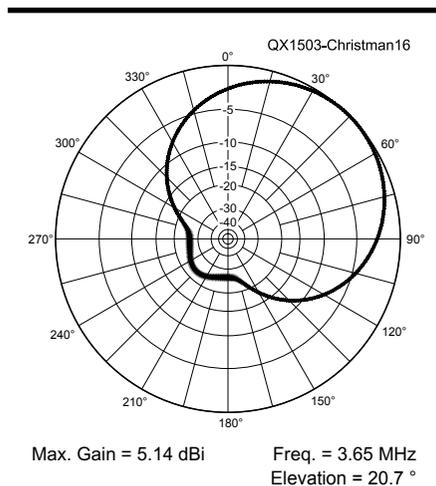


Figure 16 — Azimuth-plane radiation pattern for the Four-Square array shown in Figure 14. The antenna is designed for operation on the 80 meter band at a frequency of 3650 kHz. Each side of the square has a length of $\frac{1}{4} \lambda$ (66 feet). The relative currents into the feed points are: $I_{front} = 1 \angle -180^\circ$, $I_{side} = 1 \angle -90^\circ$, and $I_{back} = 1 \angle 0^\circ$. The peak gain = 5.14 dBi at an elevation angle of 20.7° . The half-power beamwidth = 98.7° .

Four-Square Array of Half-wave Elements

It is also feasible to construct a Four-Square phased array using full-size $\frac{1}{2} \lambda$ vertical wire elements (length = 132 feet), and suspend them using catenary ropes hung from the apex of the tower. If the lower end of each half-wave wire is placed at $H = 15$ feet, then the upper ends would be 147 feet above the ground.

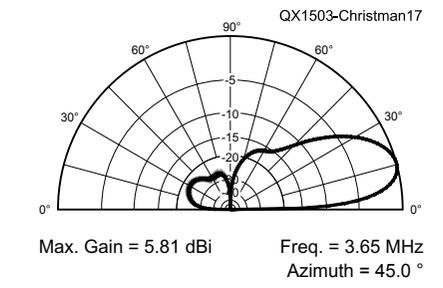


Figure 17 — Elevation-plane radiation pattern for a Four-Square array composed of $\frac{1}{2} \lambda$ vertical dipoles. The antenna is designed for operation on the 80 meter band at a frequency of 3650 kHz. The side length of the square is $\frac{1}{4} \lambda$ (66 feet). Each element has a length of 132 feet, with their bases positioned at a height of 15 feet. The relative currents into the feed points are: $I_{front} = 1 \angle -180^\circ$, $I_{side} = 1 \angle -90^\circ$, and $I_{back} = 1 \angle 0^\circ$. The peak gain = 5.81 dBi at a takeoff angle of 15.4° . The front-to-back ratio = 22.37 dB.

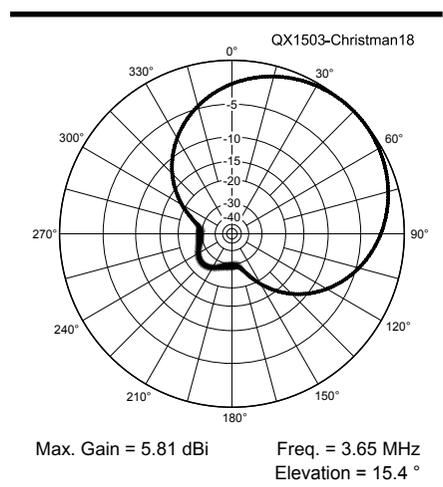


Figure 18 — Azimuth-plane radiation pattern for a Four-Square array composed of $\frac{1}{2} \lambda$ vertical dipoles. The antenna is designed for operation on the 80 meter band at a frequency of 3650 kHz. The side length of the square is $\frac{1}{4} \lambda$ (66 feet). Each element has a length of 132 feet, with their bases positioned at a height of 15 feet. The relative currents into the feed points are: $I_{front} = 1 \angle -180^\circ$, $I_{side} = 1 \angle -90^\circ$, and $I_{back} = 1 \angle 0^\circ$. The peak gain = 5.81 dBi at an elevation angle of 15.4° . The half-power beamwidth = 98.0° .

Using the classical 90° values for element spacing and current phasing in a typical Four-Square, the performance of this unusual array is listed in Table 8, with Figures 17 and 18 displaying the key radiation patterns. Peak gain for this array occurs at a takeoff angle that is lower than that of any other antenna described here. This particular system does the best job of concentrating all of the radiation at very low elevation angles. Also (as before), the input currents can be reconfigured to make the array fire through the sides of the square.

Four-Element “Lazy-V” Parasitic Array

This antenna, shown in Figure 19, is an 80 meter version of the 160 meter sloper system that was used for a number of years at the K3LR superstation.³ Each element has an overall length of 128.4 feet, and resembles an inverted V laid on its side (a “lazy V”). The feed points are located at a height of 80 feet above the ground, and are placed at the corners of a square whose side length is $\frac{1}{4} \lambda$ (66 feet) at a frequency of 3650 kHz. The included angle inside each “lazy V” is equal to 118° . All of the antennas are connected to

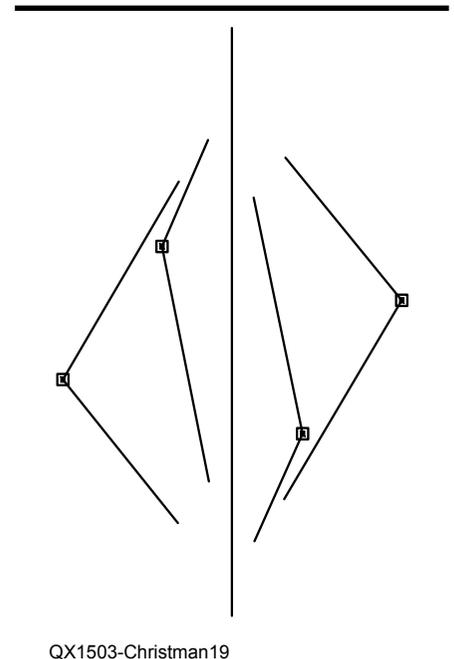


Figure 19 — Computer-generated drawing of a 4-element array of “lazy-V” antennas, along with the 180 foot tower in the center. There is an 8 foot buried ground rod at the base of the tower. Each element of the array has an overall wire length of 128.4 feet, and the included angle inside the “V” is 118° . The feed points are located at a height of 80 feet above ground, and form the corners of a square whose side length is 66 feet ($\frac{1}{4} \lambda$ at $f = 3650$ kHz).

a central switch box via sections of Belden RG-8X transmission line that are each 91 feet in length. Only a single radiator is active at any given time, while the other three lazy Vs have the lower ends of their RG-8X feeders open-circuited at the switch-box. These open-circuited lines are transformed into complex impedances at the feed points of the three inactive elements, which makes them act as parasitic reflectors.

Table 9 presents a summary of the array's performance, and the principal radiation-

pattern plots are supplied in Figures 20 and 21. Although the gain and front-to-back ratio are moderate, peak gain occurs at a takeoff angle that is almost as low as that of the Four-Square array of $\frac{1}{2} \lambda$ elements. This lazy-V system works well, and is also easy to feed. According to EZNEC, the input impedance of the active element is close to 50Ω when using the dimensions given, and provides a 2:1 SWR bandwidth of about 130 kHz (3595 to 3725 kHz).

Square array. The usual Four-Square feed point currents are applied: $I_{front} = 1 \angle -180^\circ$, $I_{side} = 1 \angle -90^\circ$ and $I_{back} = 1 \angle 0^\circ$. All four dipoles are placed in the same positions as in the parasitic array, but each one is slightly longer than before, with an overall length of 132 feet.

The main operating parameters are listed in Table 10. Figures 22 and 23 display the principal elevation- and azimuth-plane radiation patterns, respectively. The driven array generates more gain, and has better front-to-back ratio, when compared to the parasitic array. On the other hand, the feed system required for this antenna system is much more complex.

Four-Element "Lazy-V" Driven Array

This system is a variation of the one just described, but now all four of the elements are actively driven, just as in a classic Four-

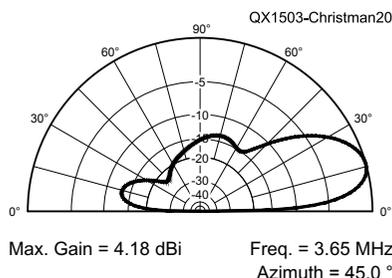


Figure 20 — Elevation-plane radiation pattern for the 4-element parasitic array of "lazy-V" antennas shown in Figure 19. Each element of the array has an overall wire length of 128.4 feet, and the included angle inside the "V" is 118°. The feed points are located at a height of 80 feet above ground, and form the corners of a square whose side length is 66 feet ($\frac{1}{4} \lambda$ at $f = 3650$ kHz). The peak gain = 4.18 dBi at a takeoff angle of 16.0°. The front-to-back ratio = 13.03 dB.

Table 9

Performance of a four-element parasitic system of "lazy-V" antennas (see Figure 19), designed for operation on the 80 meter band at a frequency of 3650 kHz. Each dipole has an overall length of 128.4 feet, and is constructed from #12 AWG copper wire. The feed points are at $H = 80$ feet, and form the corners of a square whose side length is $\frac{1}{4} \lambda$ (66 feet).

Parameter	Value
Input impedance	51.64 + j 1.3 Ω
Peak gain and takeoff angle	4.18 dBi at 16.0°
Front-to-back ratio	13.03 dB
Gain at 5° takeoff angle	0.18 dBi
Gain at 10° takeoff angle	3.35 dBi
Gain at 15° takeoff angle	4.16 dBi
Gain at 20° takeoff angle	3.92 dBi
Gain at 25° takeoff angle	2.99 dBi
Gain at 30° takeoff angle	1.49 dBi
Gain at 35° takeoff angle	-0.565 dBi
Azimuth-plane half-power beamwidth	113.7°
Azimuth-plane gain at 45° away from bore-sight	2.32 dBi (- 1.86 dB _{max})

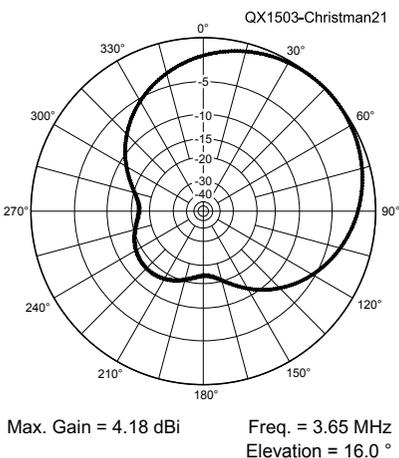


Figure 21 — Azimuth-plane radiation pattern for the 4-element parasitic array of "lazy-V" antennas shown in Figure 19. Each element of the array has an overall wire length of 128.4 feet, and the included angle inside the "V" is 118°. The feed points are located at a height of 80 feet above ground, and form the corners of a square whose side length is 66 feet ($\frac{1}{4} \lambda$ at $f = 3650$ kHz). The peak gain = 4.18 dBi at an elevation angle of 16.0°. The half-power beamwidth = 113.7°.

Table 10

Performance of a four-element driven array of "lazy-V" antennas, similar to what is shown in Figure 19, designed for operation on the 80 meter band at a frequency of 3650 kHz. Each dipole has an overall length of 132 feet, and is constructed from #12 AWG copper wire. The feed points are at $H = 80$ feet, and form the corners of a square whose side length is $\frac{1}{4} \lambda$ (66 feet). The system uses progressive 90° current phase-shifts between the elements, the same as in a classic Four-Square phased-vertical array.

Parameter	Value
Input impedance	106.0 + j 118.0 Ω (Front Element) 82.45 - j 35.68 Ω (Side Elements) - 27.53 - j 36.19 Ω (Back Element)
Peak gain and takeoff angle	4.91 dBi at 16.2°
Front-to-back ratio	18.03 dB
Gain at 5° takeoff angle	0.86 dBi
Gain at 10° takeoff angle	4.05 dBi
Gain at 15° takeoff angle	4.89 dBi
Gain at 20° takeoff angle	4.69 dBi
Gain at 25° takeoff angle	3.81 dBi
Gain at 30° takeoff angle	2.38 dBi
Gain at 35° takeoff angle	0.43 dBi
Azimuth-plane half-power beamwidth	110.0°
Azimuth-plane gain at 45° away from bore-sight	2.92 dBi (- 1.99 dB _{max})

Conclusions

This article has compared the performance of a variety of wire antennas designed for low-band DXing, which are suitable for installation on a 180 foot tower. Some configurations are very simple, yet provide

surprisingly good performance. Other arrays are more difficult to build and feed, but their direction of fire can be switched from one compass direction to another. Although each of these antennas was created specifically for use on the 80 meter band, they can easily be modified to work on other frequencies. Perhaps one of them — or even a pair of the bidirectional types, installed at right angles to each other — might be right for you!

20 meter phone, where he still needs two more countries to reach the top of the Honor Roll. When the weather is nice, Al may be found riding the back roads on his motorcycle.

Notes

¹H. Ward Silver, NØAX, Ed., *The ARRL Antenna Book*, 22nd Edition, American Radio Relay League, Newington, CT, 2011, Elevation Angles for HF Communication, pp 4-32 – 4-40.

²EZNEC Antenna-Simulation Software is available from Roy Lewallen, W7EL, P O Box 6658, Beaverton, OR 97007; www.eznec.com/.

³Al Christman, KB8I, Tim Duffy, K3LR, and Jim Breakall, WA3FET, "The 160-Meter Sloper System at K3LR," *QST*, August 1994, pp 36 – 38. An expanded version of this article appeared in Volume 4 of *The ARRL Antenna Compendium*.

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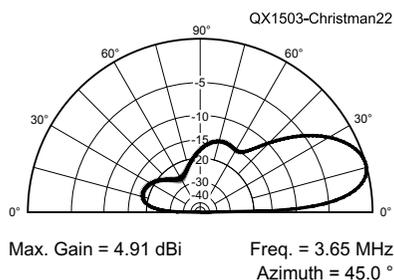


Figure 22. Elevation-plane radiation pattern for the 4-element driven array of "lazy-V" dipole antennas, similar to what is shown in Figure 19. The relative currents into the feed points are: $I_{front} = 1 \angle -180^\circ$, $I_{side} = 1 \angle -90^\circ$, and $I_{back} = 1 \angle 0^\circ$. Each element of the array has an overall wire length of 132 feet, and the included angle inside the "V" is 118° . The feed points are located at a height of 80 feet above ground, and form the corners of a square whose side length is 66 feet ($\frac{1}{4} \lambda$ at $f = 3650$ kHz). The peak gain is 4.91 dBi at a takeoff angle of 16.2° . The front-to-back ratio = 18.03 dB

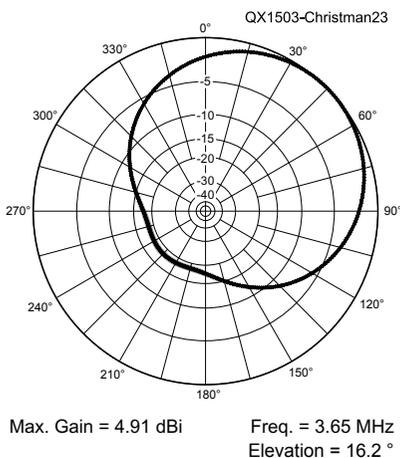


Figure 23 — Azimuth-plane radiation pattern for the 4-element driven array of "lazy-V" dipole antennas, similar to what is shown in Figure 19. The relative currents into the feed points are: $I_{front} = 1 \angle -180^\circ$, $I_{side} = 1 \angle -90^\circ$, and $I_{back} = 1 \angle 0^\circ$. Each element of the array has an overall wire length of 132 feet, and the included angle inside the "V" is 118° . The feed points are located at a height of 80 feet above ground, and form the corners of a square whose side-length is 66 feet ($\frac{1}{4} \lambda$ at $f = 3650$ kHz). The peak gain is 4.91 dBi at an elevation angle of 16.2° . The half-power beamwidth = 110° .

Table 11

Various Antennas in Order of Their Gain at a 5° Take-Off Angle.

Rank	Description	Gain at 5° (dBi)
1	2-element end-fire phased-array of Inverted-V elements (45° spacing, 135° phasing)	2.88
2	Elevated 4-Square phased-array of $\frac{1}{2} \lambda$ vertical elements (90° spacing, 90° phasing)	1.95
3	2-element end-fire phased-array of Cubical Quad elements (45° spacing, 135° phasing)	1.47
4	4-Square phased-array of "Lazy-V" elements (90° spacing, 90° phasing)	0.86
5	Elevated 4-Square phased-array with $\frac{1}{4} \lambda$ vertical elements and $\frac{1}{8} \lambda$ horizontal radials (90° spacing, 90° phasing)	0.15
6	4-Square parasitic array of "Lazy-V" elements	0.08
7	Single Inverted-V element, apex height = 180 feet	-0.98
8	Single Cubical-Quad element, apex height = 180 feet	-2.43
9	Stacked pair of Inverted-V elements, apex heights of 90 and 180 feet, driven in phase	-2.63
10	Bi-square element, apex height = 180 feet	-2.80

Table 12

Various Antennas in Order of Their Gain at a 10° Take-Off Angle.

Rank	Description	Gain at 10° (dBi)
1	2-element end-fire phased-array of Inverted-V elements (45° spacing, 135° phasing)	8.17
2	2-element end-fire phased-array of Cubical-Quad elements (45° spacing, 135° phasing)	6.91
3	Elevated 4-Square phased-array of $\frac{1}{2} \lambda$ vertical elements (90° spacing, 90° phasing)	5.07
4	Single Inverted-V element, apex height = 180 feet	4.34
5	4-Square phased-array of "Lazy-V" elements (90° spacing, 90° phasing)	4.05
6	Elevated 4-Square phased-array with $\frac{1}{4} \lambda$ vertical and $\frac{1}{8} \lambda$ horizontal radials (90° spacing, 90° phasing)	3.56
7	4-Square parasitic array of "Lazy-V" elements	3.35
8	Single Cubical-Quad element, apex height = 180 feet	3.05
9	Stacked pair of Inverted-V elements, apex heights of 90 and 180 feet, driven in phase	2.84
10	Bi-square element, apex height = 180 feet	2.77

A Triband Dipole for 30, 17, and 12 Meters

W1VT describes a dipole antenna that can fill in some gaps in band coverage for many stations.

Here is a simple wire dipole that works well on the 30 meter, 17 meter, and 12 meter amateur bands. A cleverly designed section of 600 Ω ladder line allows the use of a 1:1 choke balun and 50 Ω coax back to the radio with good efficiency, although a tuner at the radio is necessary to get the very low SWR most hams desire.

If your radio has a built-in autotuner, you can have the efficiency and ease of use of a coax fed monoband dipole on three bands, without the hassle of bringing open wire into the shack. The SWR is below 3:1 over these three bands — low enough to allow efficient matching with a tuner at the radio. This antenna would be a good complement to the many popular antennas that don't cover one or more of these bands. The popular G5RV and ZS6BKW multiband wire dipoles have high SWR on 30 meters — resulting in very poor system efficiencies, if a match can be obtained at all.

I discovered this antenna while running computer simulations based on the $\frac{1}{2}$ wavelength dipole — by adding $\frac{1}{6}$ th wavelength of feed line to this particular length of dipole — one obtains resonances on many harmonics, making it quite useful for multiband operation.^{1,2} I looked at two more variables besides dipole and feeder length — height above ground and ladder line impedance. I found that if I increased the ladder line impedance, I could tweak the harmonic resonances to land precisely on the 10 and 25 MHz bands. The article by Taft mentions harmonic displacement and suggested tuning the transmitter to compensate — I used it to advantage! It helped that I was not looking for a perfect

¹Notes appear on page 38.

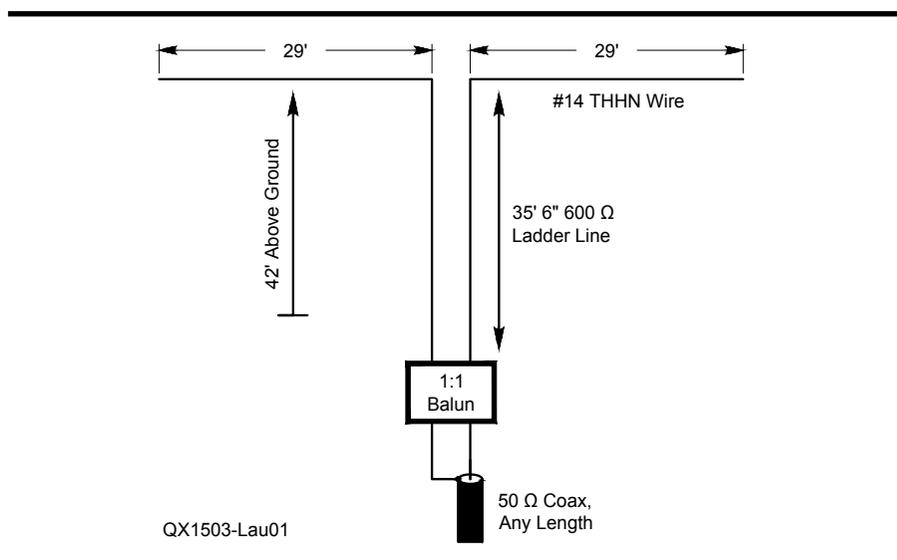


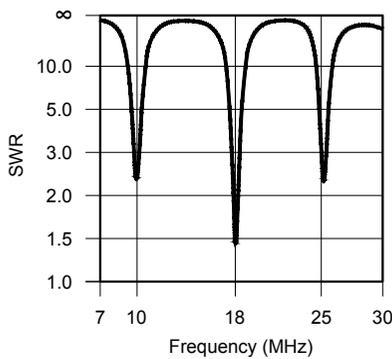
Figure 1 — Here is the basic configuration of the triband dipole. It consists of a 58 foot doublet fed with 35.5 feet of 600 Ω open wire feed line that works with good efficiency on the 30, 17, and 12 meter amateur bands.

match, or I may not have looked at matching impedances far from the optimum value of 375 Ω for the $\frac{1}{2}$ wavelength dipole.

Height above ground has a large effect on antenna impedance — from 45 to 98 Ω for the classic half wave dipole — so you should determine the optimum height first, before optimizing anything else.³ It does little good to design the perfect antenna only to find out that you have no way of putting up your antenna that high, or finding out that your trees are too close together! In designing this antenna, I maximized the height and length of the antenna, while making sure I didn't exceed the practical limits of my support structures. I set the height at 42 feet, the

height of the support ropes I have between two trees.

You want a choke balun between the open wire feed line and the coax, to prevent the outside of the coax shield from becoming a radiating antenna element. While it is possible to decouple coax with an excellent ground, such as a radial system, choke baluns are more practical if that is all you need to do. A vertical antenna makes much better use of a radial system; not only is the feed line decoupled, but system efficiency is much improved with a radial system. Either way, you still need a single point entrance panel bonded to a ground rod for lightning protection.



QX1503-Lau02

Figure 2 — I used *EZNEC* to calculate the SWR across the entire frequency range. You can see that around 10 MHz there is a dip that results in an SWR of about 2.4 and around 24 MHz there is a slightly deeper dip to an SWR of about 2.3. The lowest SWR is 1.47 at 18 MHz.

I'd suggest using a coaxial choke wound on a ferrite toroid — 11 turns of RG-58A/U on an FT-140-43 core works well from 10 to 30 MHz. Steve Hunt, G3TXQ, published an excellent balun design. He used 11 turns of RG-58 on a stacked pair of FT-240-52 toroids.⁴ He measured impedances in excess of 8000 Ω between 10 and 25 MHz. Steve's design is better able to handle the high differential impedances encountered if you want to use this antenna on another band.

The balun is a weak point of many multiband systems — many folks have seen their SWR drift as the balun heated up to destruction when the impedance was just too high for the balun to handle. Fortunately, with this antenna, impedances on 30, 17, and 12 meters are all moderate; you don't really need Steve's design, unless you want to operate on yet another band. Assuming the choking action of the balun is perfect, you can model its effect on the system as a short length of 50 Ω coax. This is easily handled in Roy Lewellan's *EZNEC*, using virtual wires.

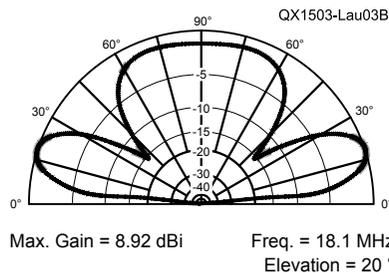
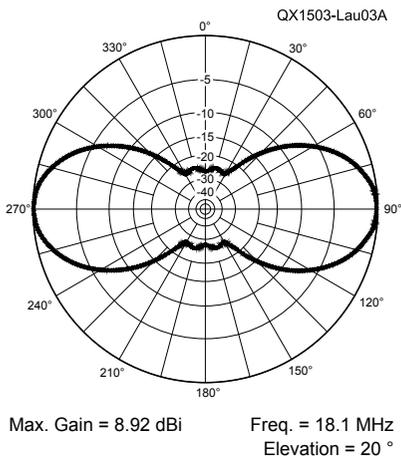


Figure 3 — Part A shows the 17 meter azimuthal radiation pattern, which is close to the pattern we normally expect to see from a dipole, with maximum signals at 90° to the wire orientation. Part B is the elevation pattern. The maximum signal is at an elevation angle of about 20°, but there is a broad lobe at very high elevation angles.

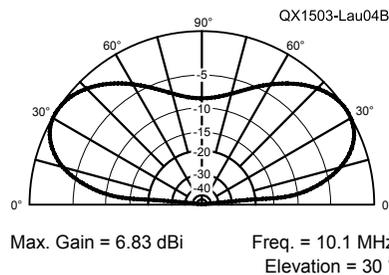
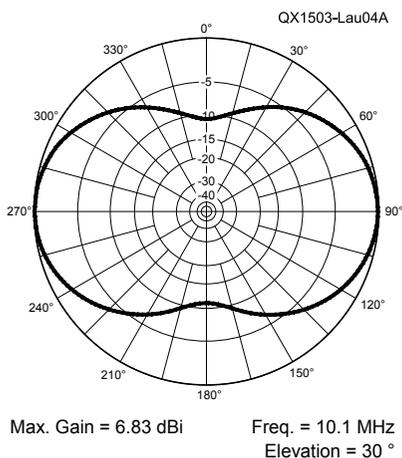
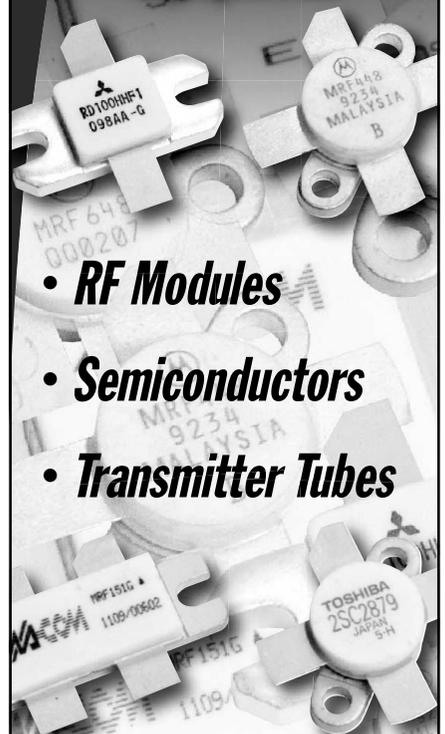


Figure 4 — Part A is the azimuthal radiation pattern on 30 meters, which shows only a slight dip in the radiated signal in the direction of the wire, with most of the signal still being broadside to the wire. Part B is the elevation pattern. The maximum signal is at an elevation angle of about 30°.

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I found that a few feet of coax drastically lowers the impedance on 15 meters, making it much harder for an autotuner mounted at the balun to operate efficiently. One solution is to add more coax. An electrical multiple of a half wavelength will reflect the input impedance to the output. The cost to efficiency is high, however. You can expect to lose an S unit with 20 feet of RG-8X, and yet another one with 40 or 60 feet of RG-8X, assuming 6 dB/S unit.

The triband dipole is a 58 foot doublet made out of #14 THHN solid house wire fed with a 35.5 foot matching section of 600 Ω ladder line having a velocity factor of 91%. See Figure 1. The somewhat low velocity factor of the ladder line assumes you are using insulated wire. The #14 THHN house wire has two layers of insulation: 15 mils of PVC and another 4 mils of nylon. While the nylon typically flakes off in less than a year, I modeled the antenna in *EZNEC* using an insulation thickness of 19 mils and a dielectric constant of 3.5. Changing the insulation thickness to 15 mils doesn't appreciably change the resonance points. The length of the 50 Ω cable isn't critical, unless you have tweaked its length to accommodate another band, like 15 or 20 meters. I suggest using the shortest length of 50 Ω coax that will comfortably reach the single point entrance panel for your station.

I used *EZNEC* to determine the theoretical SWR values. I set the loss of the 600 Ω ladder line to 0.20 dB/100 ft at 50 MHz. Figure 2 is the SWR plot across the bands. I later determined that identical impedance values were obtained at 30 MHz with a line loss of 0.153 dB/100 ft and at 10 MHz with a line loss of 0.090 dB/100 ft, in case you want to know how *EZNEC* extrapolates the loss with frequency. I chose a slightly low velocity factor of 91%, as most modern

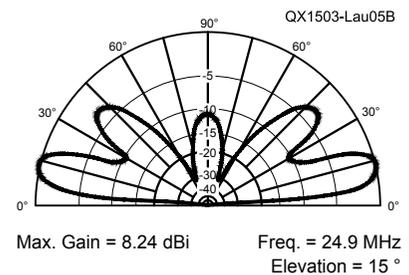
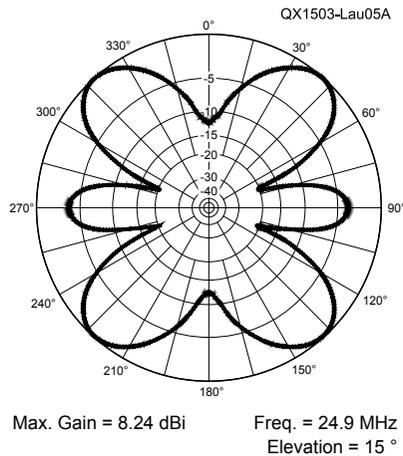


Figure 5 — On 12 meters, the azimuthal radiation pattern, shown at Part A, has four strong lobes at about 50° from the direction of the wire. There is a pair of weaker lobes at 90° to the wire in this case. Part B shows the elevation pattern, with the strongest radiation at an elevation of about 15°. There are also lobes at about 40° and 90°.

implementations of ladder line use PVC insulated wire as opposed to bare copper. If you wish to use another type of 600 Ω line, I'd suggest using a length of (velocity factor) × 39 feet. I'd avoid extremely low loss 600 Ω open wire — the 6 inch spacing is likely to bring on issues with feed line radiation. *The ARRL VHF Manual* by Ed Tilton suggests 1.5 inch spacing at 50 MHz, which translates to 3 inch spacing at 25 MHz.⁵

On 17 meters, you get a clean bidirectional pattern, with maximum gain broadside to the wires, just like a dipole. Here in New England, this pattern works great when pointed at Europe. Figure 3A gives the azimuthal radiation pattern and Figure 3B shows the elevation radiation pattern.

On 30 meters, you also get gain broadside to the wires, but due to the relatively low height, there is a fair amount of signal in all directions. Figure 4A is the azimuthal radiation pattern and Figure 4B is the elevation pattern.

On 12 meters, as the antenna is higher and longer, the antenna has an azimuthal radiation pattern with four main lobes, 50° off broadside. You still get some gain broadside, but they are small lobes 3.5 dB weaker than the main lobes. See Figure 5A. The elevation pattern is shown in Figure 5B.

Notes

- ¹Andrew Griffith, W4ULD, "The 1/3-Wavelength Multiband Dipole," *QST*, Sep 1993, pp 33 – 35.
- ²Taft Nicholson, W5ANB, "Compact Multiband Antenna Without Traps," *QST*, Nov 1981 pp 26 – 27.
- ³Ward Silver, NØAX, *The ARRL Antenna Book for Radio Communications*, 22nd Edition, p 3-5.
- ⁴Steve Hunt, G3TXQ: www.karinya.net/g3txq/chokes/
- ⁵Tilton, Edward P., W1HDQ, *The Radio Amateur's VHF Manual*, p 163 (ARRL 1972)

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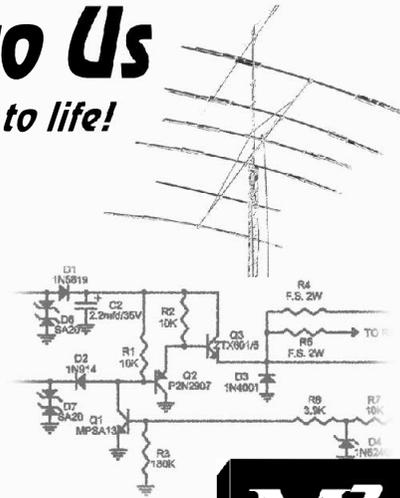
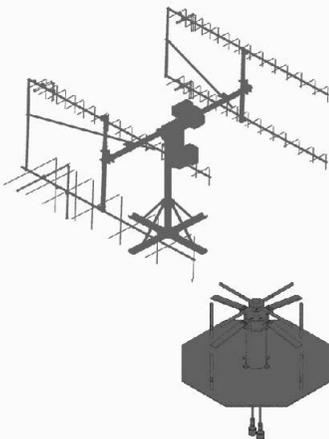
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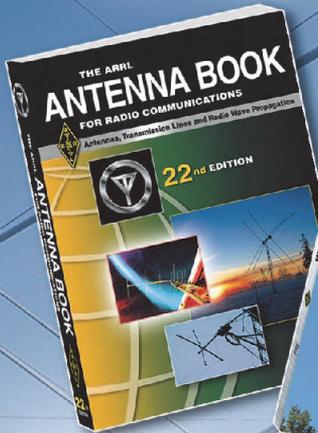
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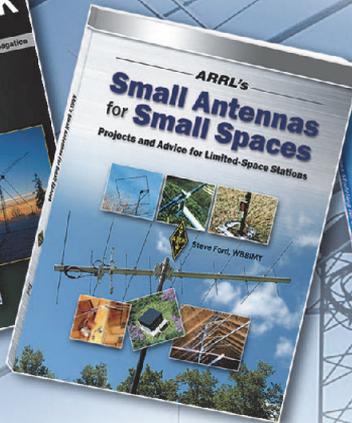
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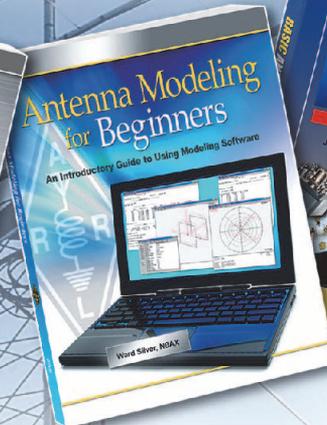
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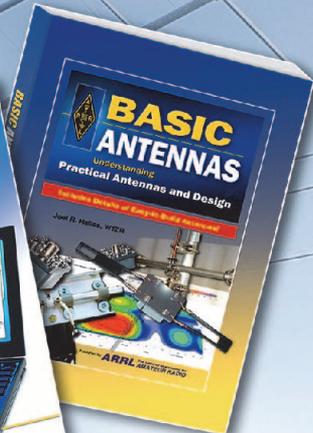
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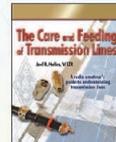
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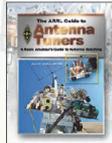
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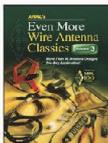
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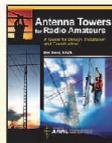
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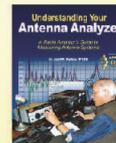
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