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INCLUDING: COMMUNICATIONS QUARTERLY

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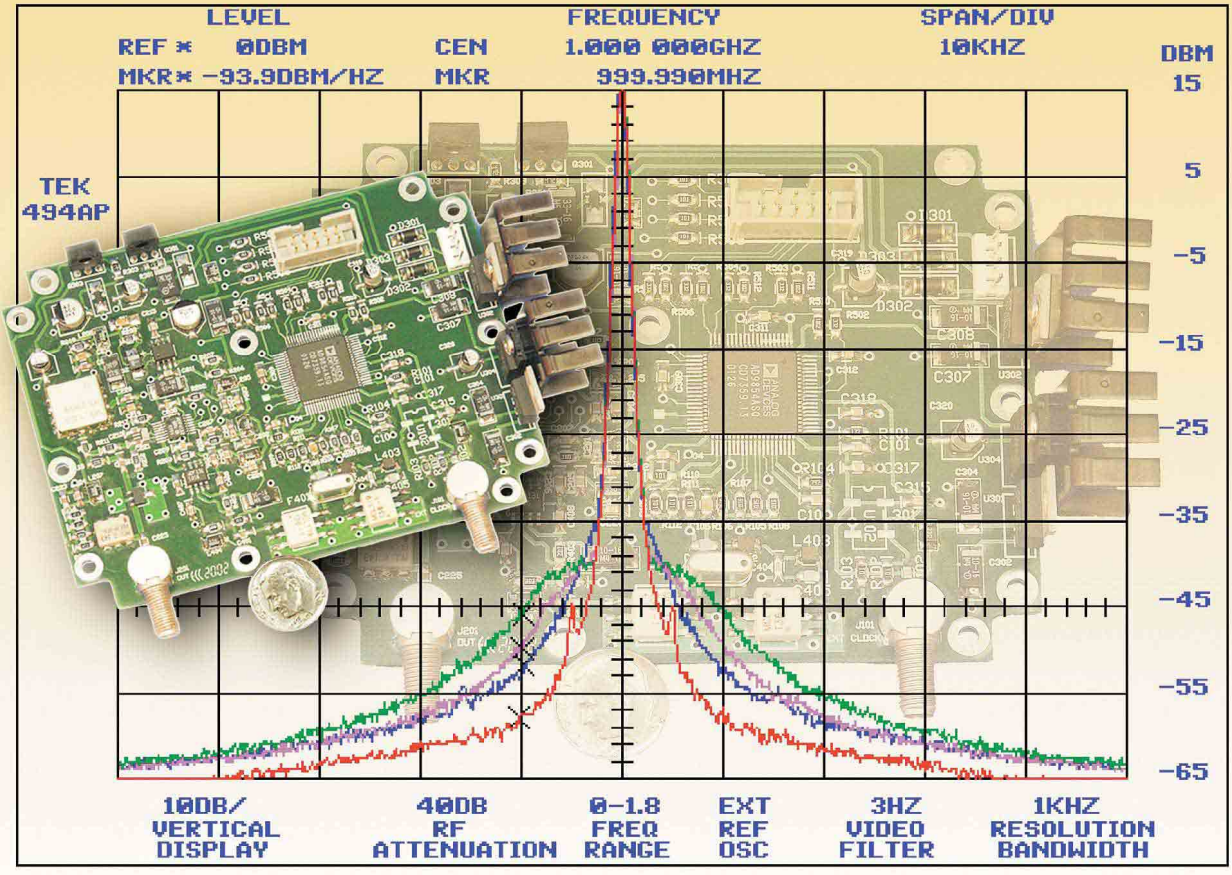
March/April 2004

Issue No. 223



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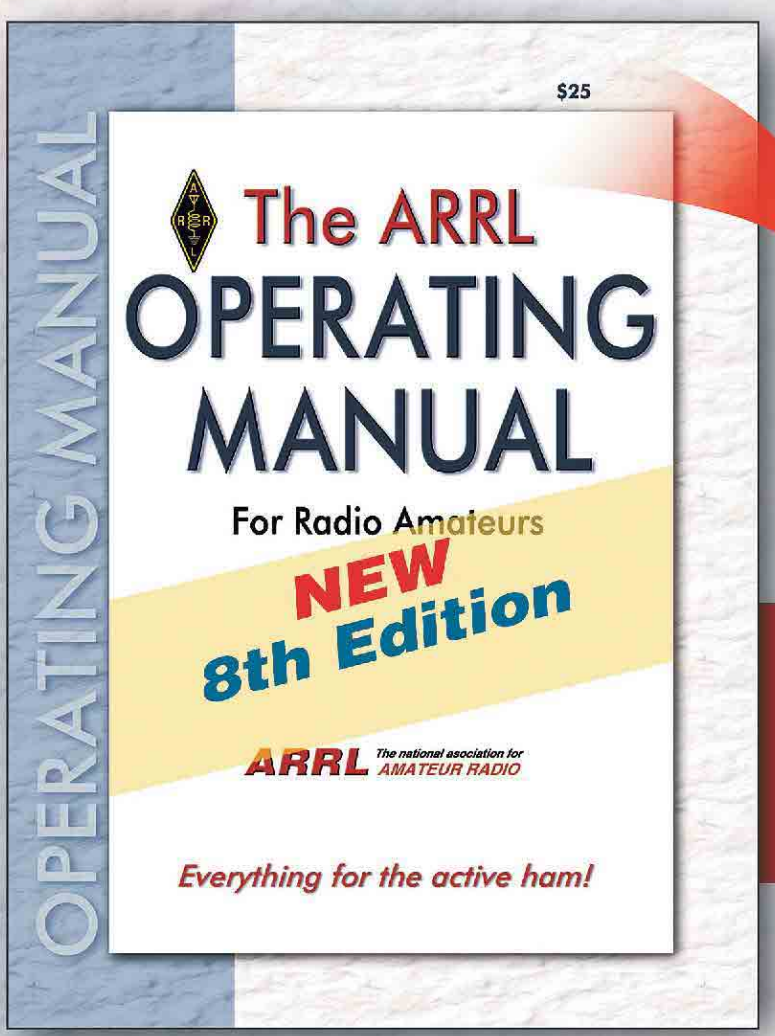

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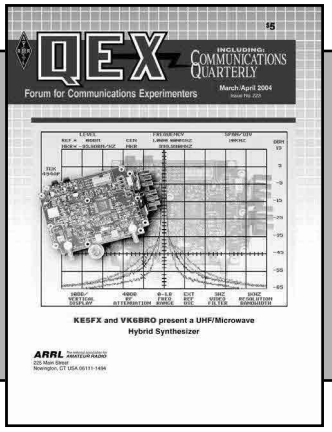

About the Cover

Use this reproducible, adaptable synthesizer for your next project (details begin on p 3).

Features

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THE AMERICAN RADIO RELAY LEAGUE

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2) document advanced technical work in the Amateur Radio field, and
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Empirical Outlook

Rulemaking: A Make-or-Break Dilemma

On December 30th, 2003, the FCC issued a Notice of Proposed Rule Making concerning so-called cognitive and software-defined radios (SDRs). The document may be found at **hraunfoss.fcc.gov/edocs_public/attachmatch/FCC-03-322A1.pdf**. Amateur transceivers covering only HF are normally exempt from FCC certification. To remain exempt, the proposed rules would require manufacturers of Amateur Radio SDR transceivers to restrict transmitter operation to frequencies inside the ham bands. Most manufacturers of other types of rigs do that now, but some rigs may be readily modified for wider coverage.

The FCC proposes that to remain exempt from certification, SDR transmit range must be restricted by features in hardware. Evidently, that means some kind of hardware key must be used as opposed to a software password or other means.

The Commission also seeks comment on whether it needs to restrict mass marketing of certain high-speed digital-to-analog converters (DACs), especially PC-based types. They reason that such devices could easily be turned into exciters and their outputs amplified to make transmitters. While they have made it clear that they don't want to do anything that would hinder Amateur Radio experimentation, we're not sure this proposal is compatible with that goal.

QEX believes that much of what we have here is an enforcement issue. By analogy, marketing of automobiles that will go 150 km/hr is perfectly legal, but you'd better not do that anywhere except on the Autobahn. Too many radios, both new and old, can be opened up by simply clipping a diode or some such thing. Information about how to do so is prevalent. If *all* ham rigs were to be covered by new restrictions, which would only be fair, then would it be illegal for me to sell my older, opened-up rig? If so, who would be there to stop me?

It seems to us that rules are only as good as the enforcement backing them. It's unclear that a purely technical solution to this would work. Lawbreakers are always going to find a way to do their thing unless the deterrence is strong enough to stop them.

SDR technology is good for our Service. We think its benefits far outweigh any detriments. What do *you* think?

On the digital voice front: AOR Japan's ARD9800 has at last been released for production and sale. The ARD9800 is an external box that can be used with virtually any ham transceiver to achieve digital voice, data and video (slow-scan) communications. Using protocols originally developed by Charles Brain, G4GUO (see *QEX*, May/Jun 2000), the unit employs an AMBE2020 voice codec, an NTSC frame grabber and built-in error detection and correction. For more information, see the product review in the Feb 2004 *QST* or visit the AOR Web site at **www.aorusa.com**.

In This Issue

John Miles, KE5FX, and Richard Hosking, VK6BRO, bring us a versatile hybrid synthesizer design. It is intended chiefly for UHF and microwave work, although we suppose it could be adapted elsewhere. Al Buxton, W8NX, writes about loaded dipoles designed using a technique he calls the dominant-element principle. It's a way to produce multiband dipole antennas without losing efficiency or bandwidth. Check it out.

Brian Cake, KF2YN, returns with a follow-on to his article about Twin-C antennas in the last issue. This time, the subject is what he calls "Boxkite" Yagis. Ample data and discussion are accompanied by construction details of arrays based on Twin-C elements. Randy Evans, KJ6PO, discusses tapped-capacitor matching circuits. Rod Green, VK6KRG, weighs in on the issue of receiver dynamic-range testing. Rod presents some examples using his own Dirodyne design, which was introduced recently (Jul/Aug 2002) here in *QEX*.

In RF, Contributing Editor Zack Lau, W1VT, presents two signal sources for 1296 work.—*73, Doug Smith, KF6DX, kf6dx@arrl.org.* □□

A Versatile Hybrid Synthesizer for UHF/Microwave Projects

This "no-tune" +14 dBm 1-2 GHz signal source for microwave projects is PC or MPU controlled. The parts are available, and the cost is reasonable.

By John Miles, KE5FX, and Richard Hosking, VK6BRO

Ever want to build a "dc-to-daylight" receiver or digitally controlled spectrum analyzer? How about a transceiver for the amateur UHF bands, or a signal generator with octave-band coverage? At the heart of each of these projects is a local oscillator with good stability and spectral purity. Our goal in this article is to present a versatile and *practical* synthesizer design that can address almost any homebrewer's need for a digitally tunable signal source from VHF to 4 GHz.

Unlike most published approaches, we've focused our design efforts as much on affordability, flexibility and reproducibility as on "specsmanship." The synthesizer we'll describe offers continuous coverage between 1 and 2 GHz with fast switching, better than 1 Hz tuning resolution and very good close-in noise performance. There's nothing to tweak or align with exotic test equipment—if you build it, it will work. Best of all, every component is available off-the-shelf from Mini-Circuits, Digi-Key or Analog Devices for a total of less than $200!

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Design Overview

When it comes to modern synthesizer design trends, numerous authors have made the case for a hybrid topology that combines the strengths of direct digital synthesis (DDS) and traditional PLL technology.[1, 2, 3, 4, 5] Before these hybrid techniques became practical, PLL synthesis often involved awkward tradeoffs between frequency-step size, spectral purity and overall loop complexity. While standalone DDS chips do not yet have the output frequency range (and in many cases, the spectral purity) to offer an across-the-board replacement for PLL technology, it's easy to use DDS technology to build a PLL synthesizer with arbitrary frequency-control precision, competitive spectral purity and low complexity.

In its most basic form, a hybrid synthesizer uses a DDS source to provide a stable, clean, and precisely tunable reference for a conventional PLL. The output of a hybrid synthesizer derives its tuning precision and stability from its DDS reference while providing the frequency coverage range typical of a PLL. The approach we've taken is similar to that of Cornell Drentea,

[1]Notes appear on page 15.

KW7CD, in his recent microwave DDS-driven PLL article,[6] adapted to use newer, more readily-available parts and improved post-DDS filtering. Tuning control is provided via a PC parallel port or an Atmel microcontroller. Like Cornell's design, our synthesizer can be used as a standalone VHF/UHF/microwave source or with an external frequency divider to achieve exceptional noise performance in HF applications.

The synthesizer's heart is the AD9852 DDS chip from Analog Devices. The AD9852 is used to generate a finely tunable reference signal near 10.7 MHz for the PLL. Chosen for its superior performance over the less-costly (and somewhat more popular) 10-bit AD9850, the 12-bit AD9852 is clocked by either an onboard 10-MHz oscillator or an external 10-MHz source, using the chip's clock-multiplier feature to generate internal clock frequencies between 80 and 120 MHz.

After passing through a crystal filter to tame any wideband spurs, the signal from the DDS is amplified and converted to a square wave by an LT1016 comparator from Linear Technologies. The filtered and squared PLL reference signal from the comparator, along with a sample of the signal from the synthesizer's VCO obtained from a resistive divider, is applied to any of several programmable PLL synthesizer ICs from National Semiconductor's LMX2306/16/26 or Analog Devices' ADF4110/11/12/13 families. These PLL chips are marketed toward the wireless- and cellular-communications industry, but their low prices, ease of use and availability in small quantities make them attractive for Amateur Radio applications from the

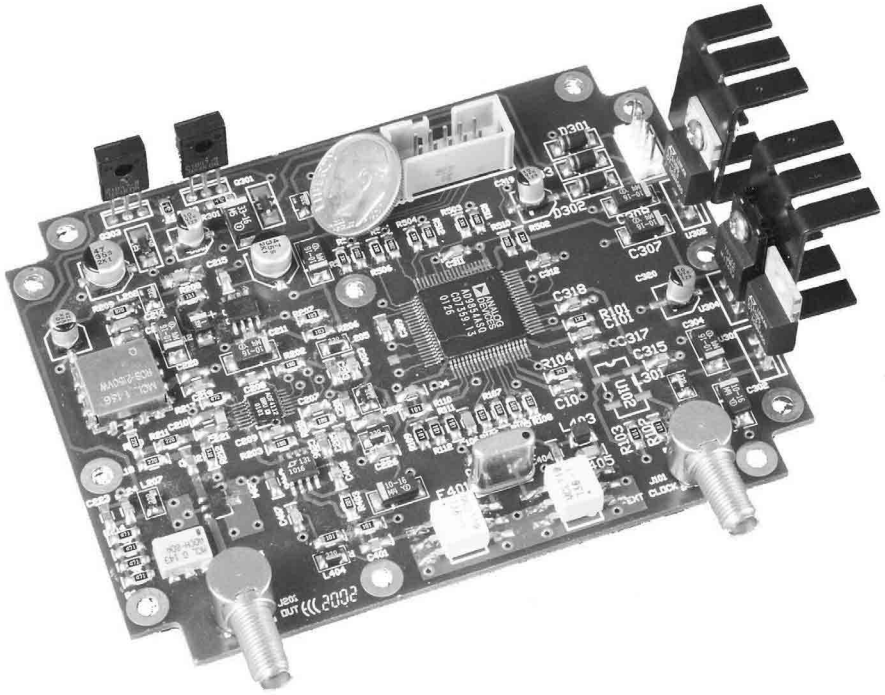

Fig 1—Complete synthesizer PC board with output and external-clock jacks.

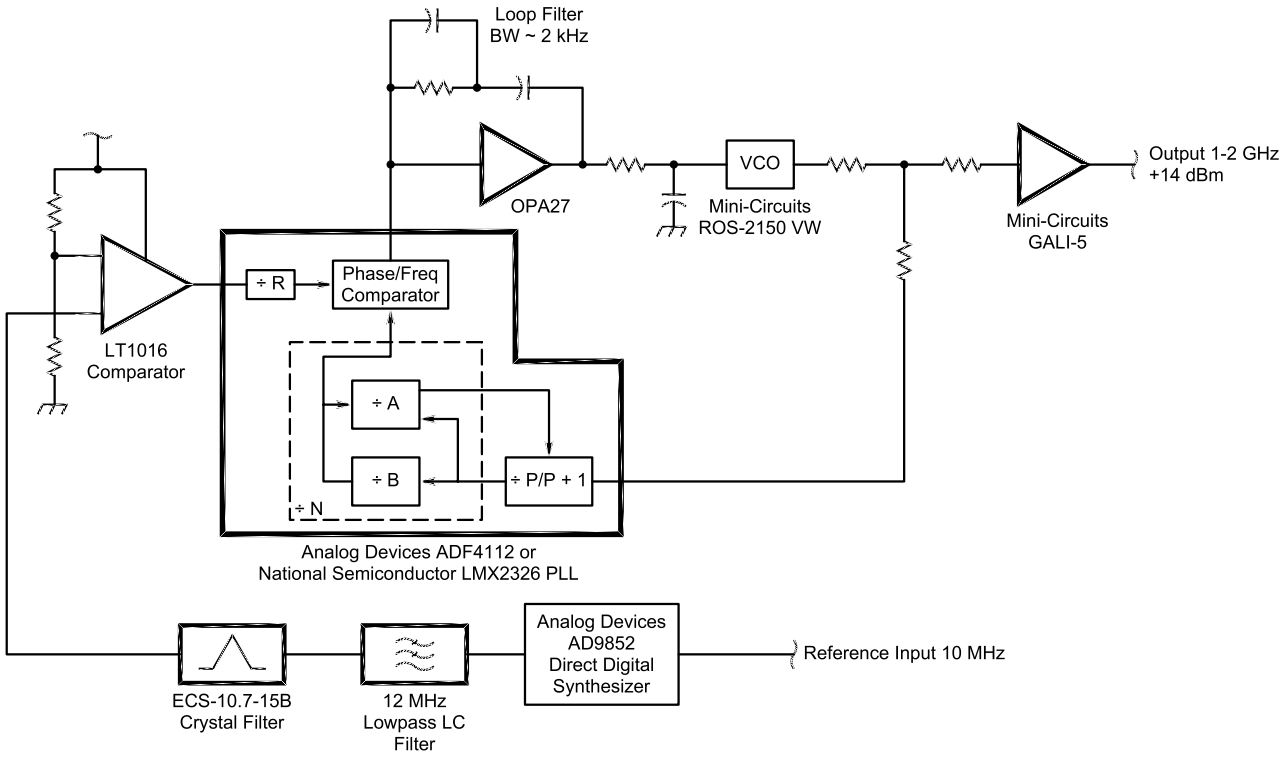

Fig 2—Block diagram.

lower VHF region to frequencies well beyond the 2.4 GHz band.

A commercial varactor-tuned voltage-controlled oscillator module generates the synthesizer's output signal. A wide variety of prepackaged VCOs are available with industry-standard PC-board footprints from vendors such as Mini-Circuits and Synergy Microwave, offering various tuning ranges, output power levels, harmonic and noise performance specifications and supply voltages. The synthesizer project described here uses the ROS-2150VW from Mini-Circuits, which provides an impressive 970-2150 MHz tuning range for about $30.

A third-order active loop filter based on the low-noise OPA27 op amp from Texas Instruments determines loop characteristics such as phase margin, bandwidth and lockup time. The op amp not only filters the digital signal from the PLL chip's charge-pump output, but also amplifies it to the 0.5-25 V level required for maximum VCO tuning range.

Following the VCO and resistive divider, a GALI-5 MMIC from Mini-Circuits provides approximately 16 dB of gain. With the ROS-2150VW VCO and divider shown, midband power at the output jack is approximately +14 dBm with less than ±2 dB of variation between 1000 and 1800 MHz.

Performance Considerations

Output spectral purity is a key specification of any PLL frequency synthesizer. Phase noise, also known as "jitter," is caused by random short-term excursions in the carrier's phase and can arise from a variety of causes. Amplitude noise is the other aspect of composite noise performance as observed with a receiver or spectrum analyzer, but it is usually insignificant compared to phase/frequency jitter. Finally, in addition to composite AM/PM noise, the synthesizer's output signal may contain discrete spurs that appear as sidebands on either or both sides of the carrier. For a detailed discussion of the nuances of noise and spur performance, see Dean Banerjee's outstanding *PLL Performance, Simulation, and Design*, downloadable at **www.national.com/appinfo/wireless/files/DeansBook_4_01.pdf**. (A printed and bound version is available at **www.amazon.com**.)

Unlike a simple LC oscillator stage, the factors that can contribute to noisy or otherwise-impure signals at the output of a PLL are almost too numerous to count. Worse, it's impossible to label a given synthesizer with a simple "spectral purity" specification that will allow direct comparisons with its peers. Noise and spurs are two-dimensional quantities—to evaluate their severity, we must consider both the amplitude relative to the carrier signal *and* the frequency offset from the carrier at which the effect in question was measured. Any synthesizer used in a receiver or transmitter must be carefully designed to minimize noise and spurs at frequency offsets *that have the potential to degrade the receiver or transmitter performance.* The last point is significant—a synthesizer serving as a wideband FM receiver local oscillator can be designed to much looser specifications than one intended for use in a 40-meter contest-grade rig.

A detailed discussion of noise causes and cures is beyond the scope of this article. However, in a nutshell, PLL noise and spurious signal analysis must consider reference noise, VCO noise, and the multiplication effect of the loop. The design of the loop filter is critical, as the bandwidth of the loop should be tailored to the VCO's needs. It is also important to consider extraneous noise and spur sources such as power supplies and intermodulation effects between various parts of the circuit.

Loop Multiplication Effect

Any PLL will increase the phase-noise amplitude of its reference source by $20 \times \log(N)$ dB within the loop bandwidth, where N is the loop's overall frequency-multiplication factor. Any discrete reference spurs within the loop bandwidth will be amplified by a similar factor, noting that their frequency offset from the output carrier will remain the same as their offset from the reference. Consider a synthesizer with a 1-GHz output frequency and a 3-kHz loop bandwidth, whose reference frequency is 1 MHz with discrete sidebands at ±1 kHz and –80 dBc. N is 1000 in this case, and $20 \times \log(N)$ is 60 dB. At its output, the synthesizer will show sidebands at ±1 kHz and –20 dBc, which may not be acceptable for many applications. It is therefore critical to use a high-quality reference source for microwave PLLs with their high N ratios—or, failing that, a very narrow loop bandwidth with a high-quality VCO.

Reference-Related Noise and Spurs

The random phase-noise performance of a DDS is quite good. It is determined by either the noise of its own reference—typically a very clean crystal oscillator—or the noise-floor limitations of the VLSI process by which the DDS chip was fabricated (typically –140 dBc/Hz for ECL technology and –150 dBc/Hz or better for modern CMOS parts such as the AD9852). However, while its phase-noise performance is adequate for most purposes, the output of a DDS exhibits discrete sideband spurs due to phase truncation and timing tolerances in the lookup table and DAC.

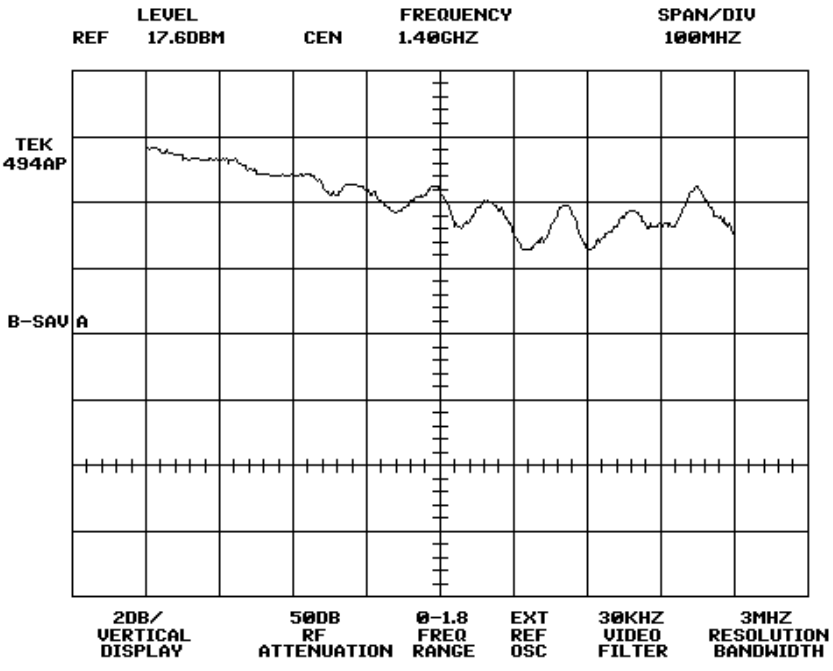

Fig 3—Output flatness from 1000-1800 MHz at 2 dB/vertical division.

These are often significant enough to rule out the use of a standalone DDS as the first local oscillator in a high-performance HF receiver. Discrete spurs in the DDS reference can appear in the synthesizer's output signal at significant carrier offsets, falling away outside the loop bandwidth after being amplified by $20 \times \log(N)$ dB within the loop bandwidth (see above). The frequency offsets of any reference-related spurs will remain unchanged regardless of the loop's overall frequency-multiplication factor.

In reality, our loop's vulnerability to spurs in its reference source is greater than one might expect. Both the National Semiconductor LMX2326 and Analog Devices ADF4112 PLL chips exhibit a readily observed (yet apparently undocumented) tendency to respond to reference-signal spurs at offset intervals corresponding to their internal comparison frequency, from dc to 100 MHz and beyond. Consider a loop with a 1-MHz comparison frequency, achieved by programming the PLL chip for a reference-divider modulus (R) of 10 with a DDS-generated reference signal at 10 MHz. As expected, DDS spurs close to the 10 MHz reference will appear in the synthesizer's output signal as mentioned above. Additionally, any DDS spurs appearing near 1 MHz intervals on either side of the 10-MHz reference frequency will appear in the output signal exactly as if they had been generated in the vicinity of 10 MHz. For example, a spur at 7.001 MHz would produce sidebands at ±1 kHz from the carrier at the output of the synthesizer. This effect has been noticed with the National chip's reference/evaluation board as well as our prototype ADF4112-based synthesizer. It is clear that low-pass filtering the DDS reference is not enough—we must bandpass-filter it to suppress as many spurs as possible across the entire RF spectrum.

Our synthesizer addresses DDS spur problems by severely band-limiting the loop's reference signal with an inexpensive four-pole monolithic crystal filter. With this 15-kHz-wide filter in place, a series of 5000 automated measurements taken at randomly-selected frequencies between 1000 and 1800 MHz revealed no significant spurious responses at any frequency. Without the filter, the synthesizer's overall spur performance was dramatically worse. In the latter test, almost every randomly chosen frequency exhibited at least one noticeable spur.

The Loop Filter and VCO

The loop filter in a PLL is designed to attenuate high-frequency components of the loop error signal so that they do not modulate the VCO output. In practice, the loop filter cutoff is commonly set at between 2% and 5% of the reference frequency to obtain adequate attenuation of comparison-frequency sidebands appearing at the phase-detector output. In our circuit,

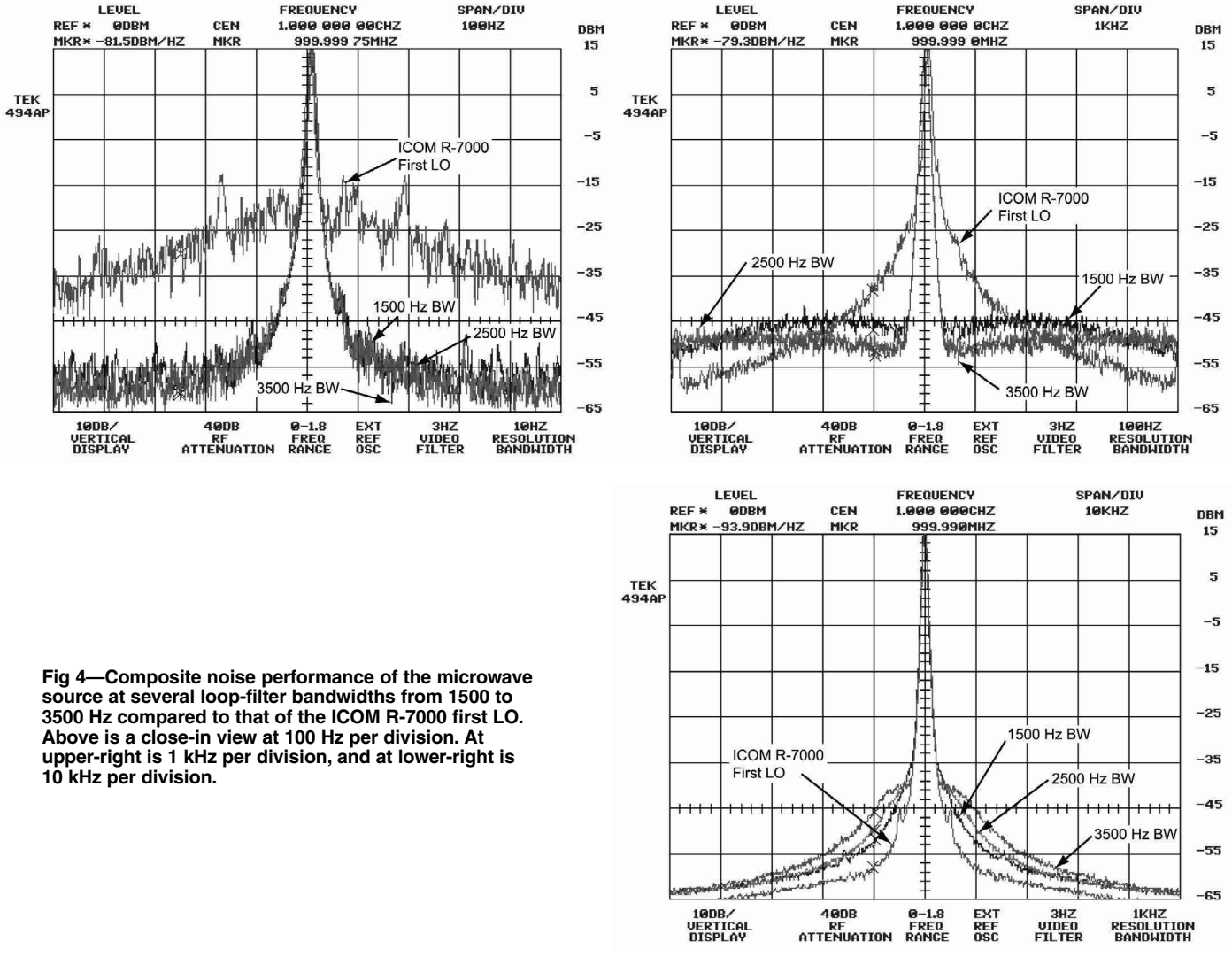

Fig 4—Composite noise performance of the microwave source at several loop-filter bandwidths from 1500 to 3500 Hz compared to that of the ICOM R-7000 first LO. Above is a close-in view at 100 Hz per division. At upper-right is 1 kHz per division, and at lower-right is 10 kHz per division.

the comparison frequency is approximately 900 kHz, so this issue can be largely ignored. We consequently design the loop filter for best system phase-noise performance based on the VCO noise characteristics.

At offsets from the VCO carrier less than the loop-filter bandwidth, the PLL attenuates noise contributed by the VCO. At offsets that are significantly greater than the PLL loop bandwidth, the principal source of noise is the VCO itself. Within the loop bandwidth, the noise performance is determined by the PLL reference source and the phase detector—and possibly the broadband noise floor of the frequency dividers as well. Even the noisiest VCO can be cleaned up by a PLL within its loop bandwidth, but extremely wide loop bandwidths carry a price of their own. As described in Analog Devices' data sheet for the ADF4110/11/12/13, the in-band noise floor of a typical inexpensive phase-frequency detector is limited to –85 to –90 dBc/Hz, after allowing for the multiplication effect of the loop mentioned above. The phase-noise specifications of a good-quality VCO at offsets greater than 10 kHz from the carrier will be better than this—typically around –95 to –110 dBc/Hz. Consequently, it makes sense to choose a loop bandwidth narrower than the carrier-offset points where the VCO free-running noise profile crosses the PLL noise floor.

Besides requiring physically larger components, a narrower-than-necessary loop bandwidth allows more VCO noise to appear in the output signal. It also slows the loop lock time. The latter may be an issue where rapid tuning is required, such as in a sweep generator or spectrum analyzer application. Conversely, an excessively wide loop bandwidth means that the PLL is actually contributing noise to the output, degrading the VCO noise profile rather than improving it.

With the Mini-Circuits VCO family we've specified, loop bandwidths in the 1.5 kHz-2.5 kHz range seem to yield the best compromise between component size, lock time and noise performance. Some typical composite-noise results are shown in Fig 4. For comparison purposes, the red trace was obtained from the first local-oscillator section of an ICOM IC-R7000 VHF/UHF communications receiver. The R7000 synthesizer splits its 770-1290 MHz output range between two separate VCOs, using a narrow loop bandwidth to suppress the reference-frequency spurs at 5 kHz. As a result, its close-in noise performance suffers relative to the hybrid synthesizer, but at offsets greater than a few kilohertz from the carrier, the ICOM's dual discrete VCOs demonstrate their superiority.

There's no escaping the fundamental truth: A high-quality synthesizer design must start with a high-quality VCO. As the ICOM design shows, multiple oscillators with narrow tuning ranges perform better than octave-band units like the ROS-2150VW, assuming the basic tank-circuit technology remains the same. Nevertheless, the Mini-Circuits parts hold up surprisingly well when compared to discrete-component VCO topologies like those of the IC-R7000 that are beyond the reach of most homebrewers.

Phase-Detector Noise and Comparison Frequency

Apart from the multiplication factor described above, noise contributed by the phase detector increases with increasing comparison frequency—the frequency at which the phase detector itself operates, after any prescaling and division is accounted for. Further, in our design, higher comparison frequencies require the DDS reference to cover a wider frequency range, potentially making post-DDS filtering more difficult with off-the-shelf parts. Using a cheap 10.7-MHz FM crystal filter with 15-kHz bandwidth, we found a PLL reference frequency of about 1 MHz (10.7 MHz divided by 11) gave the best tradeoff between phase-detector noise and DDS bandwidth.

Intermodulation Effects

Another potential source of discrete spurs in the synthesizer output is crosstalk between the DDS and PLL chips. The AD9852 DDS is a power-hungry device capable of radiating and conducting high-amplitude RF onto circuit-board traces in its vicinity. Without extensive physical shielding between the two components (that is, placing them in separate RF-tight enclosures) the PLL output exhibits spurs when tuned near a multiple of either 1/2 or 1/3 of the DDS chip master clock frequency.

If the DDS is driven by a 100-MHz clock, for example, there are spurs on either side of the synthesizer's output signal when tuned near 1033 and 1050 MHz as well as most other multiples of 33 and 50 MHz. One spur appears at the fractional clock-frequency multiple in question, while an identi-

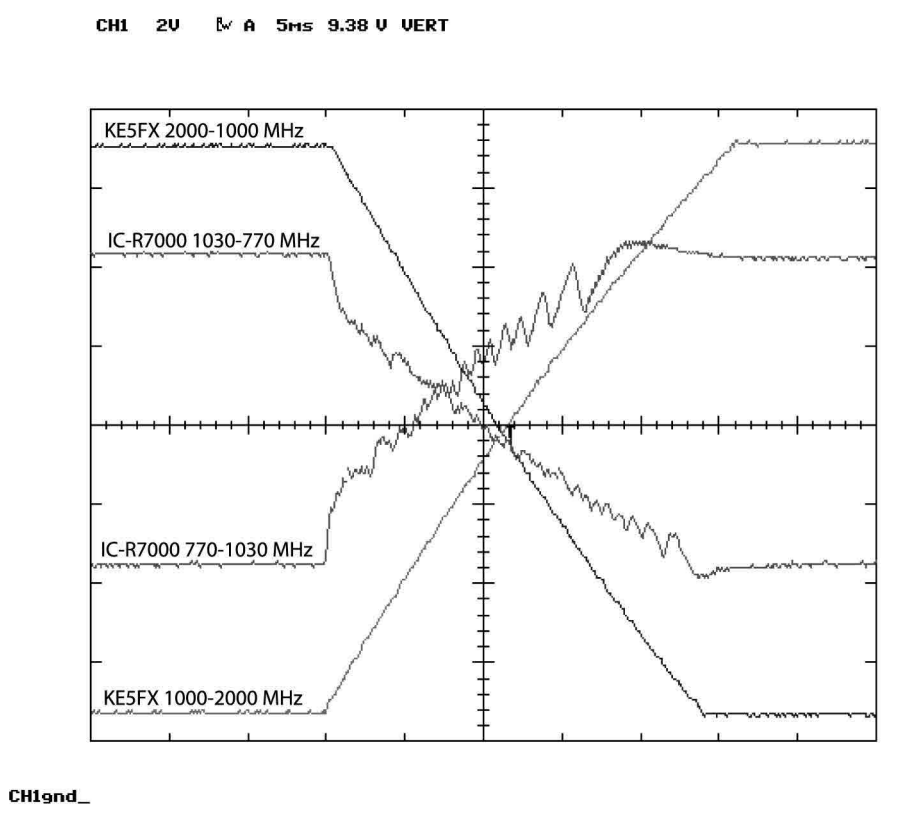

Fig 5—Synthesizer lock-up characteristics compared to ICOM IC-R7000. Curves show ICOM IC-R7000 first LO synthesizer VCO tuning lines (770-1030 MHz and 1030-770 MHz) and KE5FX hybrid synthesizer VCO tuning lines (1000-2000 MHz and 2000-1000 MHz).

cal spur appears at the same offset on the other side of the output signal. Like other reference-derived spurs, these spurs begin to fall off in amplitude once their offset from the output frequency exceeds the PLL loop bandwidth.

At a few of these problematic output frequencies, the crosstalk effect is severe enough to destabilize the loop and cause intermittent oscillation. The solution we've implemented takes advantage of the AD9852 built-in clock multiplier feature. Instead of clocking the DDS at a constant 100 MHz, we apply 10 MHz to the DDS clock input. We then use its clock multiplier to select one of five possible clock frequencies between 80 and 120 MHz, maximizing the distance between any harmonic of fDDSClk/2 or fDDSClk/3 and the synthesizer output frequency. This technique keeps the nearest fractional clock harmonic over 1.5 MHz away from the carrier at any given frequency, eliminating the problem entirely except for residual leakage of clock harmonics into the signal path associated with U204's input and output. Even without any additional shielding on the board, the latter spurs are seldom worse than –80 dBc.

While this approach avoids spurs due to this intermodulation effect, it does carry the penalty of increased software complexity. The extra calculations pose no significant burden to a PC or high-performance Atmel AVR controller, but may be a consideration if a less-capable microcontroller is used to drive the board.

Power Supplies and Noise

Some sections of the circuit are very sensitive to power-supply noise. In particular, overall phase noise performance will be degraded if supplies to the VCO and the PLL chip are not adequately filtered and decoupled. Typical IC voltage regulators are very convenient to use, but they may exhibit wideband noise at magnitudes many times greater than a well-designed discrete-component regulator. We used Zener diodes as relatively quiet references for critical parts of the circuit. Additionally, separate regulators are used to isolate different parts of the circuit, notably the digital and analog DDS sections.

Lock Time

By toggling the synthesizer between its frequency extremes while monitoring the VCO tuning port with a digital oscilloscope at 5 ms/division, the loop's lockup time and damping characteristics can be observed directly. As the graphs in Fig 5 show, worst-case lockup time is approximately 25 ms. Like the phase-noise graphs, the lock-time graphs were taken with an ROS-2150VW VCO. The results were compared to those obtained from the ICOM IC-R7000 first local oscillator. The hybrid synthesizer loop bandwidth was approximately 2 kHz.

Assembly

To obtain acceptable performance at microwave frequencies, it's necessary to use small components. The ICs used in the synthesizer come in TQFP, SOIC and SSOP packages with pin spacing as small as 0.6 mm. It is nearly impossible to work with these devices without a printed circuit board. While our prototype was constructed dead-bug style on a bare copper-clad board, the author's eyesight and nerves have yet to recover from the experience!

Many hobbyists are intimidated by the precision and small dimensions involved with surface mount construction, but the truth is that SMT homebrewing is relatively easy to master with inexpensive tools, a modicum of patience and a clever trick or two. In fact, surface-mount construction is a boon in disguise. Because all of the components and their pins are accessible from the top of the board, a dual-layer surface-mount board carries almost all of the "tweakability" advantages of dead-bug or Manhattan construction, while surface-mount components tend to be easier to purchase and stock due to industry standardization. Conversely, traditional DIP IC packages are fading from the scene at a frightening pace. Most modern RF ICs including DDS and PLL parts are simply not available in DIPs.

Soldering

Even if this is your first surface-mount project, you'll find that assembly goes smoothly with a few basic tools you may already own. A grounded soldering iron with a clean, fine tip is a must. Many constructors find a lighted magnifier helpful as well. Manipulating the 1206-sized resistors and other smaller components is very difficult by hand, but a pair of cosmetology-grade tweezers such as the 3 3/4″ Rubis model (**www.folica.com/removal/rubis_costwe132.htm**) makes the job trivial. Don't settle for whatever's on sale for $1.99 at your local drugstore – when you're doing SMT work, a good pair of tweezers is one of those tools you won't want to live without. The Rubis tweezers have razor-sharp tips that can be used to straighten pins on the smallest SMT IC packages, as well as extract resistors from the tape strips they're embedded in.

Soldering the 0.6-mm ICs—including the 80-pin DDS and the 16-pin PLL chip—will likely be the most daunting part of the project, but it's not as difficult as you might expect. The secret? A roll of ordinary solderwick (Digi-Key 50-4-25-ND). Clean the IC pads thoroughly with isopropyl alcohol prior to soldering—this goes for the rest of the board, too!—following up with a liquid flux pen (DigiKey KE1803-ND), if desired. After positioning and aligning each chip on the board, tack a couple of its corner pins into place with the soldering iron. Good pin alignment on all sides is critical, so it's important to keep the chip from shifting in place during soldering. Now, drag the soldering iron tip *lightly* across each row of pins while feeding fine-gauge solder to the point of contact. Take care not to apply enough force to bend any adjacent pins together – if this happens, fine-point tweezers or a dental pick will be necessary to get out of trouble.

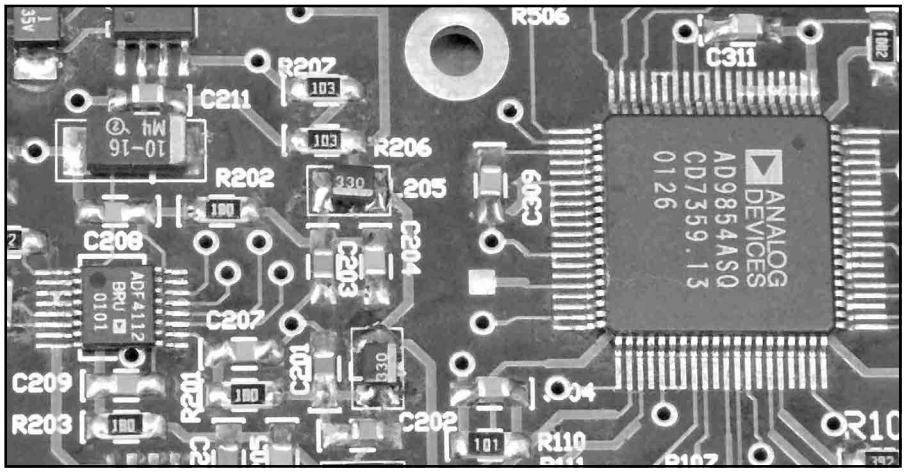

Fig 6—Close up of 0.6 mm spaced leads soldered as described in the text.

You'll find that this process unavoidably creates numerous solder bridges along each row of IC pins. That's where the solder-wick comes in: simply lay a strip across the bridged pins and apply the iron to it. The result, believe it or not, will be a row of cleanly soldered, unbridged pins that's almost indistinguishable from a professional wave or reflow soldering job (see Fig 6). Don't be overly concerned about heat damage to the chips; use a hot (750°F) iron and move along at a comfortable pace that gives the solder enough time to melt and flow around each pin. Heat soak (caused by using a too-cold or dirty iron tip over the excessively long period of time needed to make a good connection) is a greater threat to the chip than momentary contact with a hot iron.

Most of the other components, including the SOIC ICs with their 0.050″ pin spacing, do not need any special soldering techniques. However, it can be awkward to mount the resistors and capacitors due to the apparent need for three hands to keep the part from moving. You'll find that there's usually enough solder on the pads to tack one end into place long enough to solder the other end properly. Don't forget to return to the first pad and make the temporary connection permanent.

The VCO should be mounted with the dot or circle on its case to the upper right, towards C212. Notice that its pin rows are offset slightly. Solder all 16 pads, again using a clean, hot iron to minimize heat soak. Get it right the first time, because the VCO, like the DDS chip, cannot be removed once soldered into place! Solder will flow under the part, out of the reach of solder-wick and into a place where it cannot be safely remelted without overheating the VCO or damaging the board.

Pay close attention to the bands on the electrolytic capacitors and Zener diodes. The polarity bands on the latter, D304 and D306, are difficult to see compared to the larger 1N4002 diodes used for reverse-polarity protection. Ideally, F401, the crystal filter, would be mounted with a spacer to keep its pads from shorting against the bottom of the filter's case. Since no spacer is provided by the manufacturer, you should leave a half-millimeter or so of clearance between the bottom of the filter and the PC board.

Finally, use isopropyl alcohol to clean up any excess flux remaining on the board after soldering. A Q-tip or sheet of optical-grade paper tissue is helpful.

Enclosure and Shielding

The board is designed to fit into a Hammond 1590BB cast aluminum box. Applications in which the synthesizer board is not enclosed in its own chassis box may require extra shielding to suppress RFI from the DDS chip. Female SMA connectors are provided for the external clock input and synthesizer output signals. Deliver power through feedthrough capacitors. The external data connection is left to the builder's discretion, depending on what drives the module. A DB-25 connector works well, allowing initial testing with PC-based software via the printer port. Table 1 describes the required connections between the board's 10-pin IDC connector and the PC- or Atmel AVR-based controller.

Ten holes are provided in the board for #4-40 or #2-56 screws. When tightening these screws—and the mounting nuts for the SMA jacks—use caution to avoid warping or stressing the board excessively. Use spacers beneath each screw hole; the bottom of a Hammond chassis box is not perfectly flat. SMT resistors and capacitors have almost no tolerance for physical stress, and components with cracks too small to see with the naked eye can be difficult to identify.

Power Consumption

Power is applied to the board via J501, a 4-pin header with separate pins for the VCO, DDS and PLL supplies. Under normal circumstances, pins 2 and 3 should be tied together and connected to a clean, low-ripple +15 V dc supply.

While pin 2 requires less than 100 mA, the current drain at pin 3 is influenced heavily by the AD9852 clock-multiplier setting. Applications that use the suggested internal clock rates of 80-120 MHz may need as much as 400 mA to pin 3. Although we haven't encountered the phenomenon ourselves, a few AD9852/AD9854 users have observed incidents in which the chip has initialized itself in a state that causes it to draw excessive current when its reset pin (71) is not asserted during power-up. Consequently, we recommend adding a 0.5-A fuse to the power-supply connection at pin 3 in applications that cannot guarantee a logic HIGH at DDSRESET (pin 2 of J501) at power-up time.

Pin 1 should receive either +15 V or the maximum VCO tuning voltage required for the application, whichever is higher. Current drain at this pin is determined by the choice of VCO; it is typically less than 50 mA. Onboard regulation is provided for all supplies, but excessive input voltage at pin 3 should be avoided unless a substantial heatsink is provided for U304. Don't run the board—even for a few moments—without any heat sinking at all of U302 and U304! It is normal for a fully enclosed synthesizer assembly to run quite warm to the touch, especially at the higher DDS clock rates.

Reference Clock Sources

According to Analog Devices' data sheet for the AD9852, the REFCLK input pin accepts either normal 3.3 V CMOS logic levels for square-wave drive, or a 1 V pk-pk sine wave centered about 1.6 V. R102 and R103 establish a 1.6 V bias point for the REFCLK input and provide RF termination for a 10 MHz source with 50-Ω output impedance, with dc blocking by C102. The 1 V pk-pk specification corresponds to approximately +4 dBm at J101. In practice, sine-wave clock signals at J101 from –10 dBm (200 mV pk-pk) to +10 dBm (2 V pk-pk) appear to work well, with the DDS ceasing operation at –15 dBm.

Pads are provided on the board for U102, an optional 10 MHz clock module. When U102 is installed, R102 and R103 should be increased from 100 to 1000 Ω, omitting C102 and J101. However, a high-quality ovenized (or at least temperature-compensated)

Table 1

PC parallel port and Atmel AVR connections to J501

IDC Connector	LPT Port	AVR Port 'A' Signal
1	15	PA0
2	9	PA1
3	—	—
4	6	PA2
5	7	PA3
6	8	PA4
7	4	PA5
8	2	PA6
9	3	PA7
10	18-25	GND

external reference source is strongly recommended for most applications. At 1 GHz, a 50-ppm clock at U102 could put your signal 50 kHz off frequency!

Test and Demonstration Software

The synthesizer can be operated by a PC running *Windows* 95, 98 or ME, or by an Atmel microcontroller. This unique cross-platform capability is a consequence of our decision to use *C++* to program the synthesizer, rather than *Visual BASIC* or other proprietary languages. While *C++* is a more complex language than VB or *Delphi*, it's nevertheless possible to write highly-readable, portable code by eschewing the language's more arcane features.

A broad range of compilers and development tools from many vendors support *C++*. The *Windows* version of the control software is compiled with Microsoft's *Visual C++*, but the same code may also be compiled for the Atmel ATmega128 using the popular—and free!—*AVR-GCC* package (see notes at end of article for Web address). In fact, the *GCC* compiler is available on just about every platform under the sun including *Windows* and *Linux*, so even the *Windows* control program could be compiled under *GCC* with little effort. Instructions for compiling both the *Windows* MSVC and Atmel *AVR-GCC* versions are included in the PROJECT.MAK makefile, compatible with common MAKE utilities such as Microsoft's *NMAKE*. These commands may also be executed independently, from a DOS session or batch file.

PC-hosted development environments can be handy for prototyping microcontroller-based projects. You don't have to continually program and reprogram your microcontroller to test new functionality. Debugging facilities offered by packages like *Visual C++* are superior to anything available in the embedded world. Unfortunately, *Windows NT*-based operating systems such as *Windows 2000* and *Windows XP* don't normally permit direct access to I/O ports from user-mode code, so our PC control software doesn't work on these platforms. While workarounds do exist, they're beyond the scope of this article; check **www.geekhideout.com/iodll.shtml** for details.

Windows Control Program

Two versions of the Windows control program, *NSTEST.EXE* and *ASTEST.EXE*, are provided. Both are simple Win32 console applications intended to be run from the DOS command line. If your synthesizer uses the National Semiconductor LMX2326 PLL chip, run *NSTEST* <n>, where <n> specifies the parallel port connected to the synthesizer board. For synthesizers constructed with the Analog Devices ADF4112 PLL chip, use *ASTEST* <n> instead. The differences between the two chips are not profound, but they do require slightly different control code. By default, the control software expects to talk to a synthesizer based on the LMX2326 or ADF4112 chip, although the underlying SYNTH control class also supports the LMX2316 and LMX2306 parts as well as any ADF4112-compatible part in the ADF411X family.

Once the program is up and running, it should resemble the display in Fig 7. Several options are provided to aid in testing and evaluation of the synthesizer. The "R" key tunes the synthesizer to a random frequency between 1000 and 1800 MHz, while the "E" key allows the user to specify any desired frequency between 1000 and 2000 MHz (which may be entered directly in hertz or as a three or four-digit value to be interpreted as an integral multiple of 1 MHz). The 0-8 keys decrease the current frequency by 10^n Hz; holding down Shift key while typing 0-8 increases the current frequency by the same amount. The space bar forces the PLL and DDS chips to be reprogrammed (from scratch) for the current frequency, which can be helpful if power to the synthesizer is interrupted while the program is running.

Both *ASTEST.EXE* and *NSTEST.EXE* are built from *STEST.CPP*, which contains several configuration options accessible only by modifying and recompiling the source code. ANALYZER_CONTROL, which defaults to 0, can be set to 1 to enable the control program to tune a spectrum analyzer along with the synthesizer. This will also add options to the menu to acquire analyzer screenshots and execute automated random spur searches, two powerful features that were used to help develop and document the project. If you happen to have a Tektronix 490P or 2750P-series analyzer connected to

Fig 7—Win32 console application for PC parallel-port control.

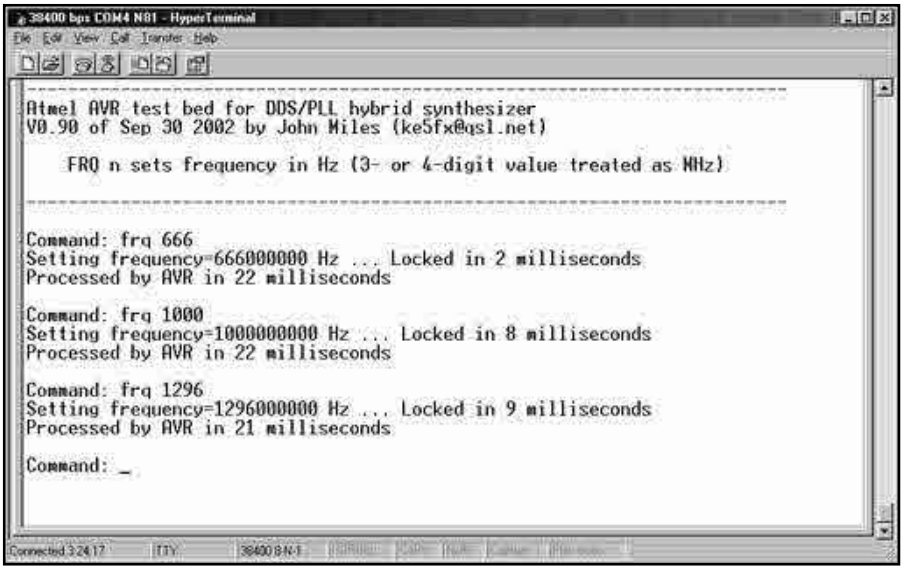

Fig 8—Communicating with the Atmel ATmega128 control program in an EIA-232 terminal session.

your PC with a National Instruments GPIB interface, give the ANALYZER_CONTROL option a try!

WAIT_FOR_LOCK, which defaults to 1, causes the control software to wait for the PLL lock-detect line to go active after any change in frequency. If the program displays a continuous string of periods after the frequency reading, it means that the loop is unlocked and troubleshooting is necessary. Recompiling *STEST.CPP* with WAIT_FOR_LOCK set to 0 will cause the program to ignore the lock-detect line.

FOUT_MIN, FOUT_MAX, FOUT_RAND_MAX and FOUT_DEFAULT determine the minimum and maximum frequencies supported by the "E" key; the maximum random frequency available by pressing "R"; and the program's default power-up frequency, respectively. These may need to be changed if your synthesizer uses a VCO other than the ROS-2150VW. DDS_CLOCK_FREQ should be set to the clock frequency provided at the DDS clock input jack (normally 10 MHz), while DDS_CENTER_FREQ should be left at 10.7 MHz for use with the crystal filter specified. DDS_MIN_MULT and DDS_MAX_MULT specify the range of possible DDS clock-multiplier constants, defaulting to 8 and 12 respectively.

Atmel ATmega128 Control Program

The ATmega128 test program, *AVRSTEST.CPP*, uses the same synthesizer control class declared in *SYNTH.CPP* as its PC-based counterpart. There the resemblance ends, however: *AVRSTEST* is a simple host program that displays a logon banner on an RS-232 terminal connected to the ATmega128's UART0 port and waits for an incoming FRQ command to program the synthesizer to a given frequency. As with the PC program, the FRQ <n> command accepts values directly in hertz with 1-Hz precision or three or four-digit values interpreted as integral multiples of 1 MHz.

The HyperTerminal program included with most versions of *Windows* offers an easy way to communicate with *AVRSTEST* (Fig 8). *AVRSTEST* assumes the ATmega128 chip is clocked at 16.0 MHz. Terminal settings should be 38,400 bps, no parity bits, 8 data bits and 1 stop bit.

Other Atmel AVR processors are candidates for controlling the synthesizer, although not all offer the speed and comprehensive I/O capabilities of the ATmega128. Programming and construction details for the AVR family are beyond the scope of this article, but there are countless online resources that discuss part selection, support-circuit design, prototyping and programming for the Atmel controllers. I encourage you to wade in with both feet. One excellent site is **www.avrfreaks.net/**, which enabled me to climb the AVR learning curve in only a few days with no prior microcontroller experience.

The SYNTH Control Class

SYNTH.CPP contains all of the functionality needed to program the hybrid synthesizer. Although the SYNTH class is designed to be easily understood and reused, we'll examine it here in some detail for the benefit of readers who may not be familiar with the *C++* language.

Creating and Initializing a SYNTH Object

To use *SYNTH.CPP* in your application, simply add it to your project's existing Win32 or Atmel *C++* code with the "#include" directive. For each synthesizer module you wish to control, you must declare an object instance of type SYNTH, passing various parameters to its *C++* constructor as shown in Code A.

On the Atmel platform, control_port is a value of type SYNTH_PORT (SYNTH_PORT_A through SYNTH_PORT_D) that specifies which of four possible Atmel I/O ports is connected to the synthesizer hardware. On a Windows PC, control_port is the integer I/O address of the desired PC parallel port, typically 0x278, 0x378, or 0x3BC. (The PC test program *STEST.CPP* determines the I/O address of the specified parallel port by reading the system's BIOS data area, another legacy technique not supported by NT-based versions of Windows.

Chip_type is a value of type PLL_CHIPTYPE that corresponds to the PLL chip used by the synthesizer board. LMX2306 specifies the National Semiconductor LMX2306, LMX23X6 specifies the LMX2316 or LMX2326, and ADF411X is used to communicate with the Analog Devices ADF4110, ADF4111, ADF4112 or ADF4113.

The paremeters min_output_frequency and DDS_ center_frequency are the synthesizer's minimum supported output frequency and the post-DDS crystal filter's center frequency in hertz, respectively. These values help determine how the synthesizer fills in the gaps between PLL multiplier settings with the finely tunable DDS reference.

DDS_clock_frequency specifies the frequency of the clock signal fed to the AD9852 in hertz, while DDS_min_clock_multiplier and DDS_max_clock_multiplier specify the permissible range of DDS clock-multiplier settings. Operating the synthesizer with DDS_clock_frequency ´ DDS_max_clock_multiplier products greater than 120 MHz is not recommended, since higher clock rates increase current consumption without offering any significant improvement in spectral purity. Internal clock rates greater than 200 MHz may cause damage to the DDS chip itself.

Code A

```
SYNTH::SYNTH      (SYNTH_PORT   control_port,
                   PLL_CHIPTYPE chip_type,
                   S64          min_output_frequency,
                   S32          DDS_center_frequency,
                   S32          DDS_clock_frequency,
                   S8           DDS_min_clock_multiplier,
                   S8           DDS_max_clock_multiplier)
```

Code B

```
SYNTH synth       (SYNTH_PORT_A,      // Use AVR port A
                   ADF411X,           // Talk to Analog Devices ADF4112 chip
                   970000000,         // Minimum frequency 970 MHz for ROS-2150VW
                   10700000,          // DDS center frequency = 10.7 MHz
                   10000000,          // DDS clock input = 10 MHz
                   8,                 // Minimum DDS clock multiplier = 8X
                   12);               // Maximum DDS clock multiplier = 12X
```

Code B is an example of how to create a SYNTH object, taken from the Atmel test program *AVRSTEST.CPP*.

Using a SYNTH Object

Once you've created a SYNTH object, you can set the synthesizer's output frequency with the SYNTH::set_frequency() function (see Code C). The hertz parameter is an unsigned 64-bit integer that specifies the desired output frequency in hertz.

After tuning the synthesizer, you can call the SYNTH::locked() function (Code D) to determine when the loop has locked at the new frequency. Depending on the loop bandwidth and the magnitude of the requested frequency change, SYNTH::locked() will return TRUE within several milliseconds of a call to SYNTH::set_frequency().

Code E is a small *C++* fragment showing how to tune the synthesizer object to a given frequency and wait for the command to succeed."

Synthesizer Programming in Detail

You can create and use SYNTH objects in your own *C++* code without knowing anything about programming the synthesizer hardware. For the curious, however, here are a few of the technical details underlying the SYNTH class. *SYNTH.CPP* is heavily commented, but it does have aspects that may not be readily apparent.

Precalculation of DDS and Comparison-Frequency Constants: The SYNTH constructor's first task is to compute and store the *R* (reference) modulus for the PLL chip based on the DDS_center_frequency parameter. *R* determines the relationship between the 10.7 MHz reference frequency from the DDS and the actual PLL comparison frequency (*Fcomp*) where the phase detector operates. At reference frequencies under 16 MHz an *R* modulus of 11 is selected, yielding *Fcomp* ≈ 973 kHz for the standard 10.7 MHz reference. Higher reference frequencies, such as would be associated with a 21.4 MHz crystal filter, are divided by 32.

Once *R* is known, the following equation yields the required tuning range of the DDS synthesizer:

$$DDS_{\mathrm{BW}} \quad \frac{DDS\_center\_frequency^2}{min\_output\_frequency \bullet R} \qquad \text{(Eq 1)}$$

For example, the 10.7 MHz DDS reference in a 1000-2000 MHz synthesizer will need to be tuned across a range approximately 10.4 kHz wide to cover the gaps between adjacent PLL *N* factors. This is a good match for the 15-kHz bandwidth of the ECS-10.7-15B crystal filter. Higher DDS frequencies require broader crystal filters, leading to impaired spur performance.

After calculating the DDS tuning range, the minimum and maximum possible comparison frequencies are obtained by Eq 2:

$$Fcomp_{\min,\max} \quad \frac{DDS\_center\_frequency \pm \left(\frac{DDS_{\mathrm{BW}}}{2}\right)}{R} \qquad \text{(Eq 2)}$$

$Fcomp_{min}$ is stored with the SYNTH object and used later by SYNTH::set_frequency() to determine the PLL's overall *N* division factor for the requested frequency. Needless to say, performing the $Fcomp_{min}$ calculation when the SYNTH object is created rather than every time SYNTH::set_frequency() is called saves quite a bit of processing time!

Prescaler Modulus Selection: Most modern PLL chips, including those used by the synthesizer, contain dual-modulus prescalers that divide the sampled VCO signal prior to applying it to the A and B counters that perform the loop's divide-by-*N* function. Because of the way these three counters –A, B and P–interact, the dual prescaler factors P and P+1 determine the minimum overall *N* value the chip can support[8] according to the equation $N_{min} = P^2–P$.

The National Semiconductor chips have fixed prescaler constants that the software must look up based on the chip_type parameter. The LMX2306, intended for lower-frequency use through 550 MHz, offers a relatively-small *P* factor of 8/9 corresponding to N_{min} = 56. The higher-frequency LMX2316 and LMX2326 parts use *P* constants of 32/33, so their minimum *N* factor is substantially higher (N_{min} = 992). Notice that when $Fcomp_{max}$ = 973 kHz as determined above, the LMX2316/26 parts are incapable of operation below 965 MHz (973 kHz× 992)! To use the LMX2316/26 parts at lower frequencies, the *R* modulus calculation will need to be modified to yield a lower $Fcomp_{max}$, possibly degrading phase-detector performance in the process.

The Analog Devices ADF411X chips offer a more flexible alternative by supporting programmable *P* factors from 8/9 to 64/65. When chip_type is set to ADF411X, the SYNTH constructor calculates N_{min} based on $Fcomp_{max}$ and the specified min_ output_frequency**,** and selects the largest *P* factor that will satisfy the $N \geq P^2–P$ relation.

PLL Initialization: Once the *P* and *R* modulus values have been determined, the PLL chip is ready for initialization. Again, this is done only once when the SYNTH object is constructed, rather than every time a new output frequency is requested. The chip's digital lock-detection feature is also enabled at this point. The initialization procedure is slightly different for the National and Analog parts, due to the latter's programmable prescaler and charge-pump current control features.

DDS Initialization: Finally, the SYNTH constructor must reset and initialize the AD9852 DDS. This step has been a source of confusion to many AD9852 users, because the chip powers up in a mode that causes its internal registers to update themselves periodically whether the initialization data has been completely transmitted or not! Our approach is to initialize the DDS chip twice with identical command words, turning off the auto-update feature and setting the minimum clock-multiplier factor by default. Portions of the chip that are unused by the synthesizer are turned off to save power, including the secondary or quadrature DAC and internal comparator (which is re-

Code C

```
void SYNTH::set_frequency(U64 hertz)
```

Code D

```
BOOL SYNTH::locked(void)
```

Code E

```
synth.set_frequency(1296001575);          // Tune to 1296.001575 MHz
while (!synth.locked());                  // Wait for phase-lock
```

placed by the LT1016 in our circuit due to its superior sensitivity and output level). Even if the first initialization attempt is incomplete due to an asynchronous register update, the second attempt will ensure that the entire initialization command is latched manually at the proper time.

SYNTH::set_frequency(): When the synthesizer is tuned to a new frequency, the SYNTH::set_frequency() function first calculates the PLL's overall *N* division factor by dividing the output frequency by the previously calculated $Fcomp_{min}$. The required DDS reference frequency *D* is then given simply by

$$D = \frac{F_{out} \bullet R}{N} \qquad \text{(Eq 3)}$$

Because the *D* value is computed in 56.8 fixed-point format, the DDS reference frequency can be set with 1/256 Hz precision, corresponding to tuning steps roughly 0.73 Hz wide at a 2-GHz output frequency. (A 76-GHz rig can be tuned in 30 Hz steps with this degree of control—so given the wide availability of less than 1-ppb crystal, GPS and rubidium standards on eBay, there's no excuse for not knowing where you are!)

Next, the PLL's *A* and *B* counters are programmed with the calculated *N* value and a series of assert() statements ensure that the resulting values make sense for the PLL chip type. Attempting to tune to an out-of-range frequency will yield a fatal error in the Windows test program. Phase continuity during most incremental tuning operations is ensured by skipping the PLL programming step if the *N* value has not changed since the last call to SYNTH::set_frequency(). This way, the synthesizer can be tuned smoothly with a rotary encoder without generating clicks or other objectionable artifacts in received audio.

The AD9852 is programmed to generate the reference frequency *D* in two steps. First, clock multiplier *CM* is chosen according to the algorithm described in "Intermodulation Effects" above. Because a change to the clock multiplier reinitializes the DDS chip, requiring extra processing time and breaking phase continuity, the clock multiplier is not reprogrammed if the previous *CM* value is still optimal for the new output frequency. After the clock-multiplier calculation step, the quotient of the *D* value and (DDS_clock_frequency × CM) is written to the DDS phase-increment register at 36-bit precision, and the loop begins its phase-locking process.

SYNTH::locked(): This function returns the logic level at pin 14 of the PLL chip. This is a digital lock-detection output that goes high after the detected phase error remains below a predetermined minimum for a period of five cycles of F_{comp}.

Schematic Notes

Power Supply (Fig 9): D306 determines the voltage supplied to the VCO module, minus the voltage drop across the series pass transistor of approximately 0.6 V. See Table 2 for recommended D306 part numbers for 5 V and 12 V VCOs.[9]

PLL and VCO (Fig 10): Loop-filter components C212, C213, C216, R208 and R209 are determined according to

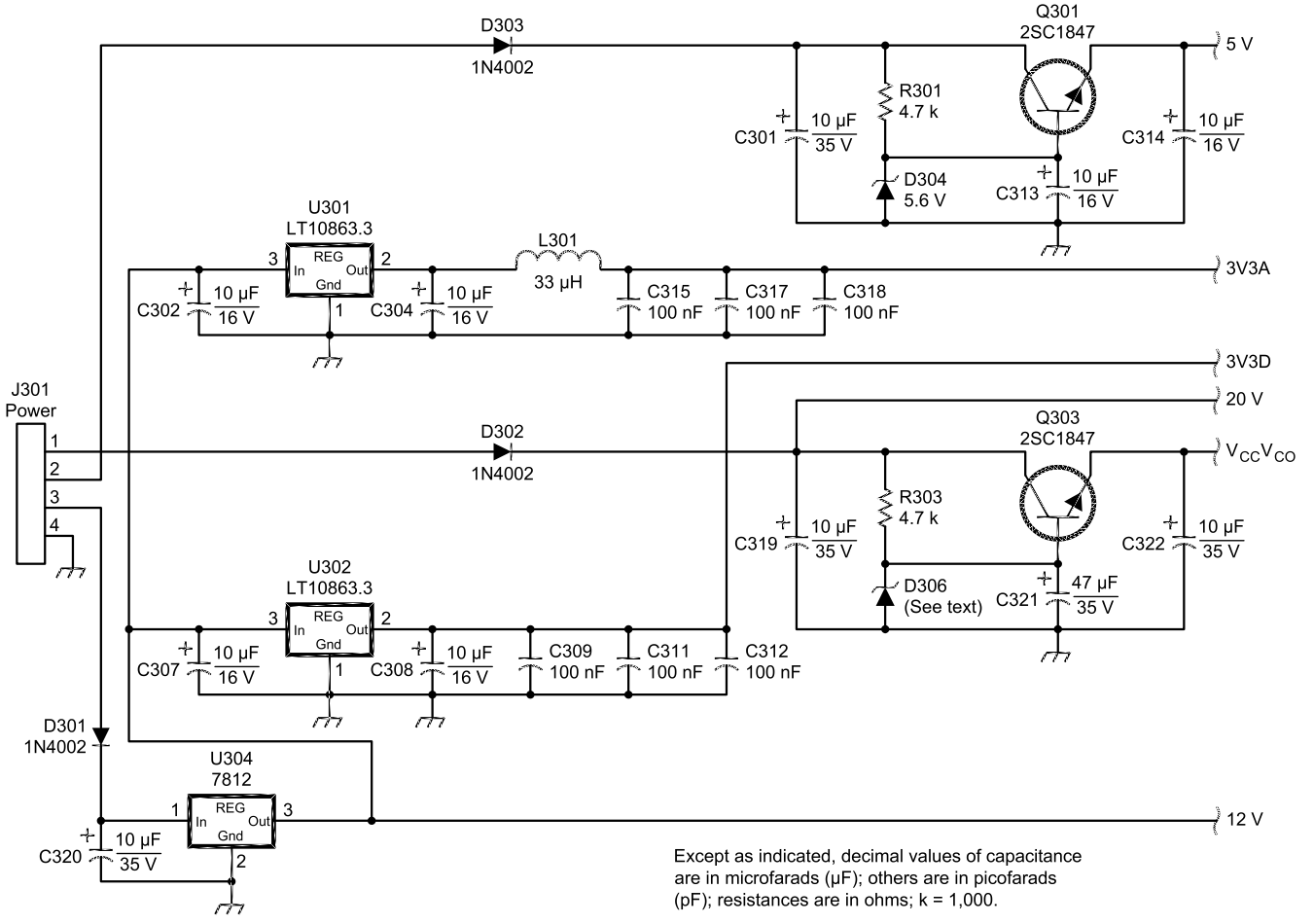

Fig 9—Power-supply section.

the equations from the Banerjee reference (see sidebar).

If an Analog Devices ADF4110, ADF4111, ADF4112 or ADF4113 is selected for U201, R217 must be installed between pin 1 and ground to bias the chip's internal charge-pump current source. Boards assembled with the National Semiconductor LMX2306, LMX2316 or LMX2326 should omit R217.

C230 is included to discourage any tendency of the PLL to lock to VCO harmonics. During testing, the ROS-2150VW VCO second-harmonic level was observed to increase by as much as 2-3 dB relative to a 1 GHz fundamental at temperatures close to 0°F, causing occasional lock failures when the board was initially powered up below room temperature. A 1 pF capacitor between the differential FIN pins prevented this symptom from occurring. Even-larger shunt capacitor values may be necessary with other VCOs, especially when the synthesizer is operated well below the upper frequency limit of the PLL chip.

Similarly, when working with other VCOs, the divider network consisting of R210-R212 and R218 may need to be adjusted to keep the sampled VCO signal at pin 6 of U201 within the manufacturer's recommended 0 to –10 dBm range.

DDS and Clock (Fig 11): There is provision for an internal clock module to be installed at U102, although higher-quality external clock sources are recommended. If an onboard clock source is installed, the components associated with the external-clock input (R102, R103, C102, J101) should be omitted.

U101 may be either an Analog Devices AD9852AST or AD9854AST. The AD9854 supports the generation of in-phase and quadrature signals—a feature not used by the synthesizer—but is otherwise identical to the AD9852. The -AST suffix refers to the family of parts designed for a maximum internal clock rate of 200 MHz. While the more-expensive -ASQ part supports clock rates up to 300 MHz, its conductive bottom surface must be reflow soldered to the PC board to dissipate enough

Table 2

Complete parts list including Digi-Key, Mini-Circuits and Analog Devices part numbers. All parts are from Digi-Key unless otherwise specified.

R101—1.3 kΩ (P1.3KECT-ND)
R102, 103—100 Ω (P100ECT-ND, 50-Ω external clock input only)
R102, 103—1 kΩ (P1.0KECT-ND, internal clock source only)
R403—1 kΩ (P1.0KECT-ND)
R104—3.9 kΩ (P3.9KECT-ND)
R105-108, 212—51 Ω (P51ECT-ND)
R201-203—18 Ω (P18ECT-ND)
R206, 207, R510-514—10 kΩ (P10KECT-ND)
R210, 211, 218—22 Ω (P22ECT-ND)
R213-216—470 Ω (P470ECT-ND)
R217—4.7 kΩ (P4.7KECT-ND, ADF4112 PLL chip only; omit for LMX2326)
R301, 303—4.7 kΩ (P4.7KECT-ND)
R401, 402, 501, R507-509, R109-112—100 Ω (P100ECT-ND)
R502-506—3.3 kΩ (P3.3KECT-ND)
C101, 103, 207, 208, 209, 401—0.01 µF, 50 V ceramic (399-1234-1-ND)
C102, 104, 106, 202, 204, 205, 211, 215, 219, 224, 226, 309, 311, 312, 315, 317, 318, 407, 408—0.1 µF, 50 V ceramic (PCC104BCT-ND or 311-1179-1-ND)
C201, 203, 206, 210, 217, 220—100 pF, 50 V ceramic (399-1205-1-ND)
C214, 321—47 µF, 35 V electrolytic (PCE3280CT-ND)
C218, 228, 302, 304, 307, 308, 313, 314, 409—10 µF, 16 V tantalum (399-1595-1-ND)
C221-223, 225, 406—0.001 µF, 50 V ceramic (311-1170-1-ND)
C230—1 pF, 50 V ceramic (see text) (399-1178-1-ND)
C301, 319, 320, 322—10 µF, 35 V electrolytic (PCE3413CT-ND)
C403, 405—270 pF, 50 V NP0 ceramic (399-1209-1-ND)
C404—470 pF, 50 V NP0 ceramic (399-1213-1-ND)
D301-303—1N4002 (DL4002DICT-ND)
D304—5.6 V 500 mW Zener (BZT52C5V6-7DICT-ND)
D306—5.6 V 500 mW Zener (5 V VCOs only) (BZT52C5V6-7DICT-ND)
D306—12 V 500 mW Zener (12 V VCOs only) (BZT52C12-7DICT-ND)
F401—ECS-10.7-15B monolithic crystal filter, ±7.5 kHz bandwidth, 25 kHz stopband (X704-ND)
J101, 201—SMA female bulkhead jack (J569-ND)
J301—four-position straight header (A1912-ND)
J501—10-position shrouded header (MHB10K-ND)
L402, 403—0.91 µH RF choke (DN1015CT-ND)
L201, 202, 204-207, 301, 404—33 µH 115 mA RF choke (TKS2638CT-ND)
L203—Mini-Circuits ADCH-80A
Q301, 303—2SC1847 (2SC18470Q-ND)
T401, 402—Mini-Circuits T36-1-KK81 36:1 RF transformer
U101—Analog Devices AD9852AST DDS synthesizer
U102—ECS-3953M 10 MHz oscillator module for internal-clock option (XC288CT-ND)
U201—Analog Devices ADF4112BRU 3.0 GHz RF PLL frequency synthesizer
U201—National Semiconductor LMX2326TM 2.8 GHz RF PLL frequency synthesizer (LMX2326TM-ND)
U202—Burr-Brown OPA27 low-noise opamp (OPA27GU-ND)
U203—Mini-Circuits ROS-2150VW 1-2 GHz VCO
U204—Mini-Circuits GALI-5 monolithic amplifier
U301, 302—Linear Technology LT1086-3.3 voltage regulator (LT1086CT-3.3-ND)
U304—7812 voltage regulator (NJM7812FA-ND)
U401—Linear Technology LT1016 precision comparator (LT1016CS8-ND)

Miscellaneous Hardware and Optional Parts

Hammond 1590BB aluminum enclosure (HM152-ND)
TO-220 mounting kits for U301, U302 (4724K-ND)
10-position IDC socket for J501 (MKC10A-ND)
10-position ribbon cable (MC10G-5-ND

Loop Filter Components (ROS-2150VW VCO, 2.5 kHz loop bandwidth)

R208—150 Ω (P150ECT-ND)
R209—82 Ω (P82ECT-ND)
C212—1 µF, 35 V tantalum (PCS6105CT-ND)
C213—0.1 µF, 50 V ceramic (PCC104BCT-ND)
C216—0.1 µF, 50 V ceramic (PCC104BCT-ND)

heat for operation beyond 200 MHz.

Post-DDS Filtering (Fig 12): F401 is designed to be terminated with 3 kΩ for minimum passband ripple, but it works well in this noncritical application with 36:1 broadband transformers and a 50-Ω resistive termination at U401. The low-pass filter consisting of L402, L403 and C403-405 helps reject DDS image signals at higher frequencies where F401's parasitic elements degrade its attenuation.

Digital Control Interface (Fig 13): R501 and R507-509 help protect U201 from ESD and transients, while the dividers formed by R501-506 and R510-514 allow 5 V logic families to drive the data lines of the 3.3 V DDS chip (U101) safely. Table 1 details the connections between J501 and the IBM PC parallel port or Atmel AVR microprocessor used to control the synthesizer.

Analog Devices recommends that the DDSRESET line (J501 pin 2) be asserted HIGH during power-up initialization. When using the PC parallel port, it's a good idea to include a 1/2 A fuse in the power-supply line to J301 (pin 3) to protect the chip against invalid initialization states.

PC Boards

Dual-layer PC boards with plated vias, solder mask and component markings are available from John Miles, KE5FX (**jmiles@pop.net**) for US $25 postpaid. Cash, checks and PayPal are accepted.

Postscript: Collaborative Design in the Internet Age

This board was designed entirely via e-mail—the two authors have never met! Richard, VK6BRO, was courageous enough to devote substantial personal labor to the project sight-unseen, fashioning the schematics and PC board layout from a few vague sentences from John, KE5FX. ("Pin 10 goes to pin 15, with a 33 µH RF choke to the supply bus.") Despite the 9000 miles that separated us, the design process could scarcely have been easier with two engineers in adjacent cubicles. Our synthesizer boards have undergone substantial testing over the past year, and we're both eager to hear the experiences of others who've duplicated our work or improved upon it. Additional thanks go to Kathy Stenger for her drafting assistance.

Notes

[1]QUALCOMM Inc, "Hybrid PLL/DDS Frequency Synthesizers," AN2334-4 (CL80-3459-1A), March 1992.

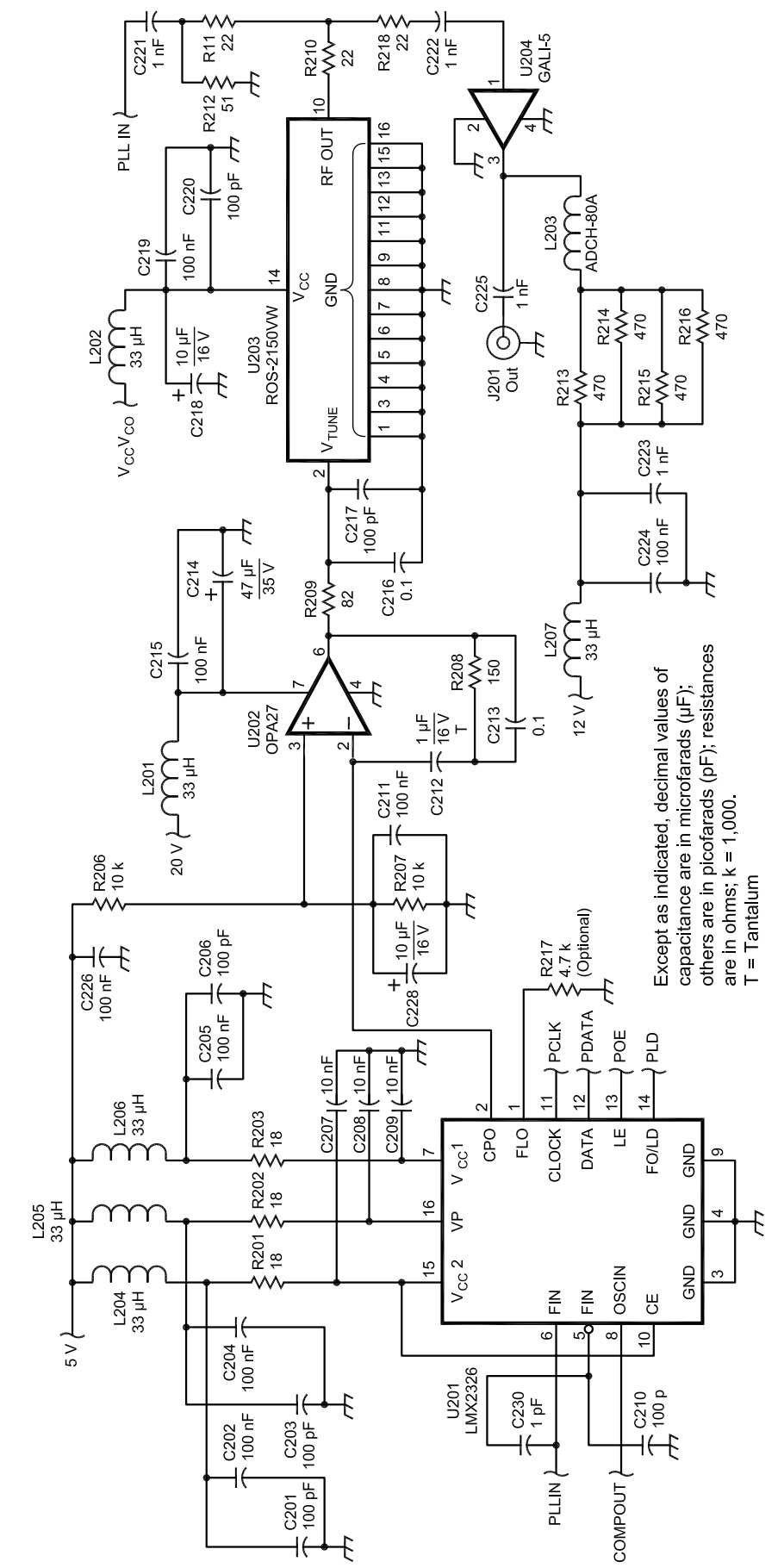

Fig 10—PLL and VCO sections.

Spectral-Noise Measurement

Spur and noise amplitudes are expressed relative to a desired carrier signal. A spur at –80 dBc has an amplitude 80 dB below that of the carrier. Unlike CW spur signal power, though, noise power is proportional to the square of the bandwidth over which it is measured; noise levels measured by a receiver with a 1-kHz IF filter cannot be directly compared to levels measured with a 100-Hz filter. So noise power is usually expressed in units of dBc/Hz, that is, decibels below the carrier amplitude, normalized to a bandwidth of 1 Hz. When using a spectrum analyzer to measure composite noise, its resolution bandwidth setting (which corresponds to the IF filter bandwidth in a traditional receiver) can range from 1 Hz to 1 MHz or more. As a first approximation, the noise level observed on a receiver or spectrum analyzer at a given bandwidth can be normalized to 1 Hz by subtracting $10 \times \log_{10}(BW)$.

However, this isn't the whole story. The shape factor of a filter affects its *noise equivalent bandwidth*, which is another way of saying that a filter's 3-dB points measured or modelled with a CW signal may not accurately reflect its response to broadband noise. A spectrum-analyzer filter designed with a gradual slope to reduce ringing and distortion during fast sweeps may exhibit a noise equivalent bandwidth substantially wider than its specifications suggest. Finally, the logarithmic amplifier and video detector stages may also introduce errors in the analyzer's apparent response to noise. For these reasons, most traditional (non-FFT-based) spectrum analyzers require a correction factor of +2 to +2.5 dB to be added to normalized noise powers.[10]

Many newer analyzers include a "noise normalization" feature that computes log(*BW*) and assorted correction factors automatically. The Tektronix 494AP used to capture the spectral-purity graphs in this article displays normalized noise values in dBm/Hz, so all of the graphs were recorded with a –16 dBm offset value to compensate for the +16 dBm amplitude of the 1 GHz carrier being measured.

Loop Filter Component Selection

When choosing a particular VCO or loop bandwidth for your synthesizer, it will be necessary to recalculate the loop-filter component values. This is a step-by-step process that begins with a few key loop parameters.

K_{vco} is the VCO tuning-port sensitivity in Hz/V. This may vary by a factor of 2:1 or more over the VCO tuning range. Varactor-tuned VCOs are less sensitive at the upper end of their range. In our calculations with the ROS-2150VW, we use its K_{vco} at 1000 MHz (70 MHz/V), but loop performance can be further optimized by looking up—or experimentally measuring $-K_{vco}$ at the frequency of interest.

K_{pfd} is the phase detector's current gain in amperes per 2π radians of phase error. K_{pfd} is not well characterized by many manufacturers. Some specify it in milliamperes per radian, while others neglect to mention whether or not it's dependent on the PLL chip supply voltage. Analog Devices employs a constant-voltage source with an external resistor to establish their chips' maximum K_{pfd}, while the LMX2326's figure is 1 mA for a 3 V supply and "is about 25% more when operating at 5 V versus 3 V and varies with voltage in a linear fashion," according to the online help at National Semiconductor's *WEBBENCH* page (see Table 3 for the URL). For our example, we'll select a programmed value of 1.88 mA for the ADF4112.

F_{out} is the output frequency in hertz. For synthesizers with wide tuning ranges, we take the geometric mean (the square root of the product) of its maximum and minimum frequencies. To cover 1000-2000 MHz, for example, F_{out} would be 1414 MHz.

F_{comp} is the comparison frequency in hertz. We assume the DDS reference is centered at 10.7 MHz, and choose an *R* divisor of 11 to yield F_{comp}= 973 kHz.

F_c is the loop bandwidth in hertz. We'll use 2500 Hz in our example calculation, since this yields readily available component values and results in fast lock times without degrading the VCO noise performance.

Θ is the desired phase margin, typically between 40° and 55°. A margin of 48° is a good compromise between minimal spectral "shoulders" and lock time.

T31 is the ratio of the time constants of poles T3 (R209, C216) and T1 (R208, C212, and C213) in the active-filter topology we've selected. Banerjee's suggested[7] *T31* constant of 0.5 is used.

C3 is the capacitor value in farads at the final pole before the VCO, C216 in our case. Values of a few hundred picofarads are common, but these lead to large (read: noisy) series resistor values. In the author's experience, as long as the opamp is stable driving a capacitive load, relatively large *C3* values have the benefit of keeping wideband noise from the rest of the loop out of the VCO. The OPA27 used in our loop works well with C216 = 0.1 μF.

First, the phase margin and loop bandwidth are converted to radian-based notation:

$$\Theta = \frac{\Theta \cdot 2\pi}{360} \quad \text{(Eq 4)}$$

$$\omega_c \quad 2\pi \cdot f_c \quad \text{(Eq 5)}$$

The time constants of the three filter poles can then be determined:

$$T1 \quad \frac{\left(\frac{1.0}{\cos\Theta}\right) - \tan\Theta}{\omega_c}\left(\frac{1.0}{1.0 + T31}\right) \quad \text{(Eq 6)}$$

$$T3 \quad T1 \bullet T31 \quad \text{(Eq 7)}$$

$$T2 \quad \frac{1.0}{\omega_c^{\,2}(T1 + T3)} \quad \text{(Eq 8)}$$

Next, the loop's *N* factor (or its geometric mean, in this case) is calculated along with a few intermediate results:

$$N \quad \frac{F_{out}}{F_{comp}} \quad \text{(Eq 9)}$$

$$Cx_a \quad \frac{K_{pfd} \bullet K_{vco}}{\omega_c^{\,2} \bullet N} \quad \text{(Eq 10)}$$

$$Cx_b \quad \frac{1.0 + \left(\omega_c^{\,2} \bullet T2^2\right)}{\left(1.0 + \left(\omega_c^{\,2} \bullet T1^2\right)\right)\left(1.0 + \left(\omega_c^{\,2} \bullet T3^2\right)\right)} \quad \text{(Eq 11)}$$

$$Cx \quad Cx_a \bullet Cx_b^{\,0.5} \quad \text{(Eq 12)}$$

The loop-filter component values are now available (see Table 4), with the results for our example 2500 Hz loop filter shown in parentheses.

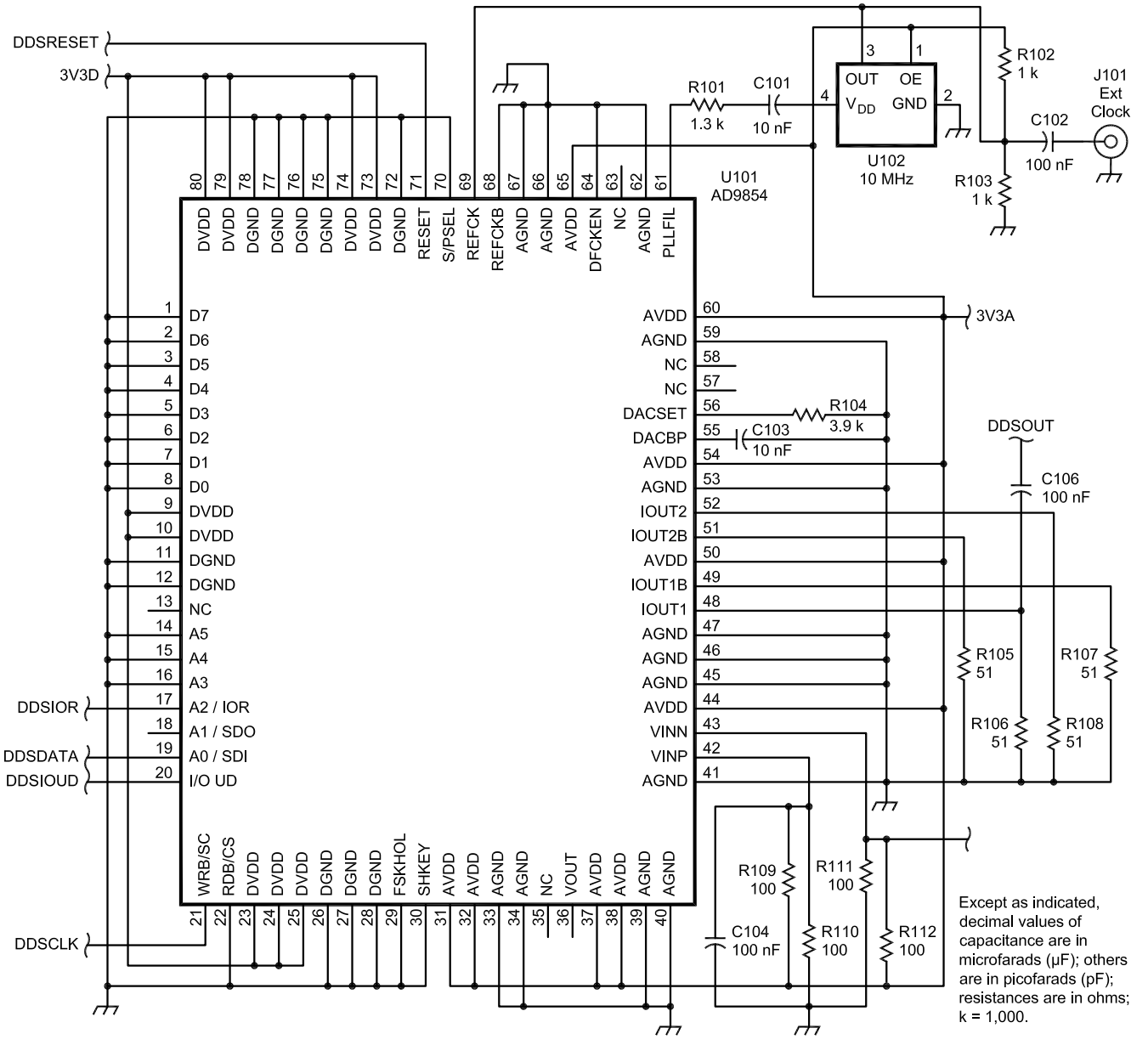

Fig 11—DDS section.

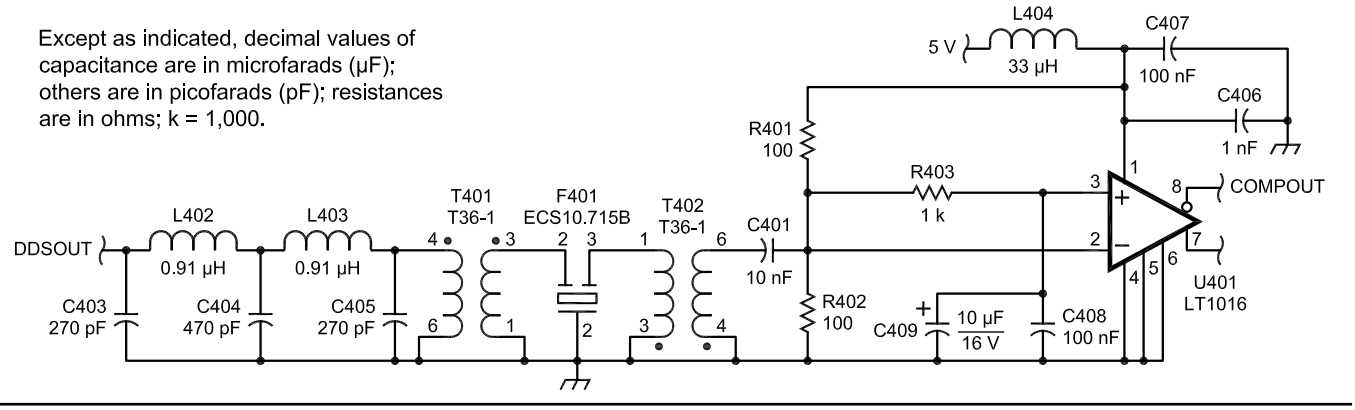

Fig 12—Filter and comparator section.

[2]US Patent No. 4,965,533 Direct Digital Synthesizer Driven Phase Lock Loop Frequency Synthesizer, QUALCOMM Inc.

[3]US Patent No. 5,028,887 Direct Digital Synthesizer Driven Phase Lock Loop Frequency Synthesizer with Hard Limiter, QUALCOMM Inc.

[4]U. L. Rohde, DJ2LR/KA2WEU, "A High Performance Hybrid Synthesizer," *QST*, Mar 1995, pp 30-38.

[5]U. L. Rohde, *Microwave and Wireless Synthesizers: Theory and Design* (New York: John Wiley and Sons, ISBN 0471520195, 1997), pp 489-504.

[6]C. Drentea, KW7CD, "Beyond Fractional N," *QEX*, Mar/Apr 2001, pp 18-25 and May/Jun 2001, pp 3-9.

[7]D. Banerjee, *PLL Performance, Simulation, and Design,* 2nd Edition (National Semiconductor Corporation, ISBN 0970820704, 2001), pp 105-113.

[8]Banerjee, p 160.

[9]You can download a document of Table 2 with active hyperlinks from the ARRLWeb **www.arrl.org/qexfiles/**. Look for 0403Miles.zip.

[10]R. Witte, *Spectrum and Network Measurements* (Norcross, Georgia: Noble Publishing, ISBN 1884932169, 2001), pp 147-148.

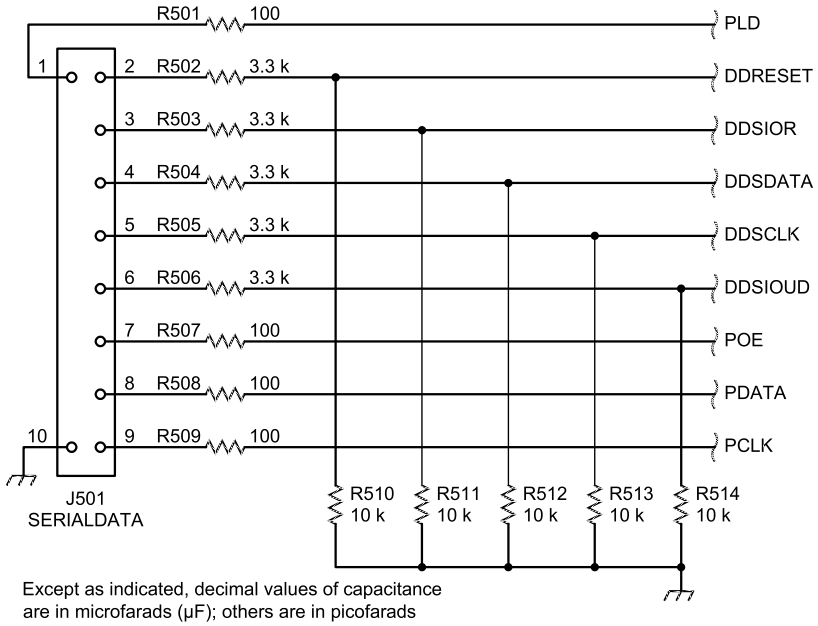

Fig 13—Data interface section.

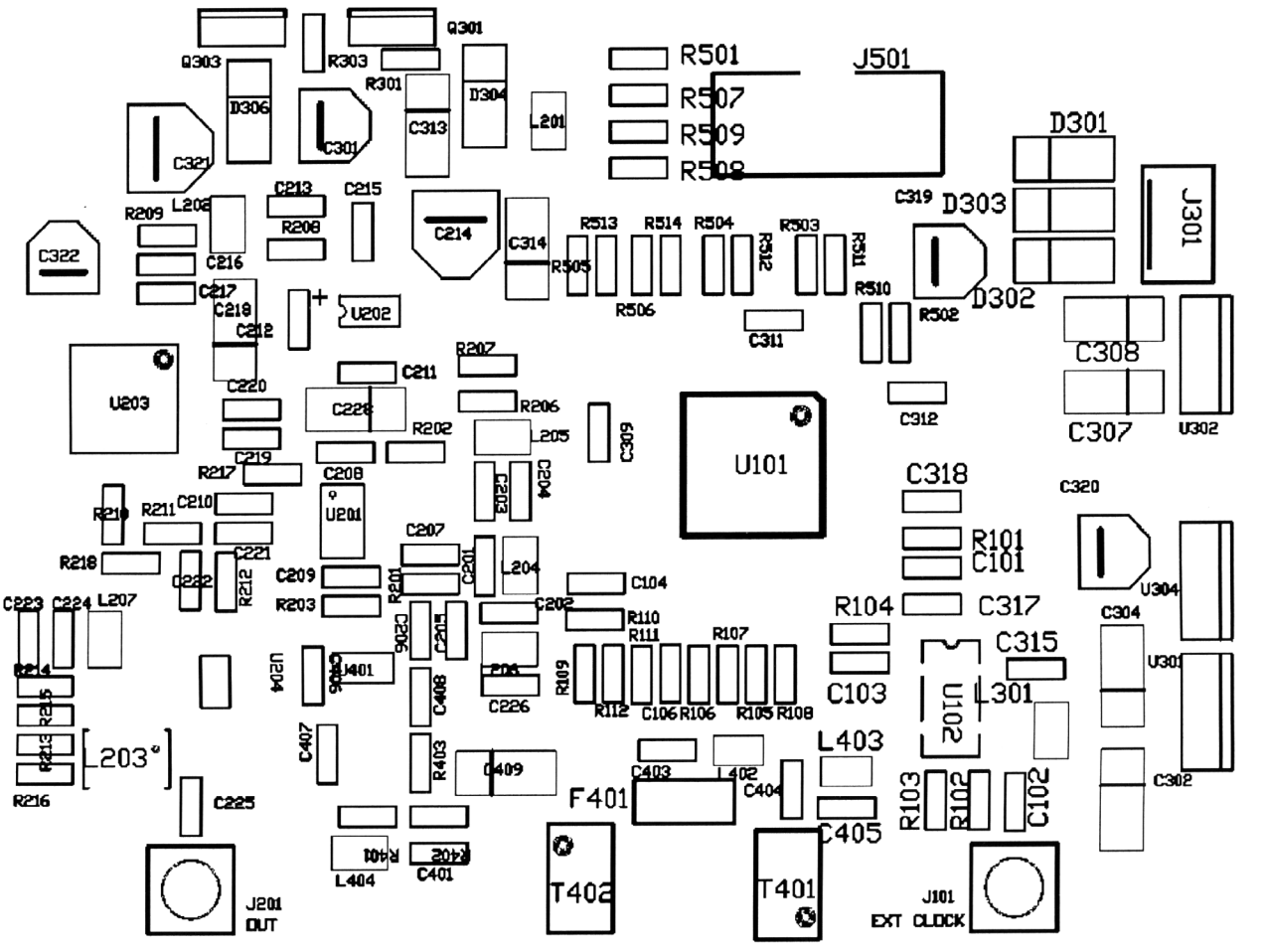

Fig 14—PC board component layout.

Table 3

Software and Supplementary Files

www.qsl.net/ke5fx/synth.html

Data Sheets and Other Online Resources

AD9852: **products.analog.com/products/info.asp?product=AD9852**
LMX2306/16/26: **www.national.com/pf/LM/LMX2326.html**
ADF4110/11/12/13: **products.analog.com/products/info.asp?product=ADF4112**
GALI-5: **www.minicircuits.com/cgi-bin/spec?cat=amplifier&model=GALI-5**
ADCH80A: **www.minicircuits.com/dg03-242.pdf**
LT1016: **www.linear.com/prod/datasheet.html?datasheet=157**
OPA27: **//focus.ti.com/docs/prod/folders/print/opa27.html**
ROS-2150VW: **www.minicircuits.com/cgi-bin/spec?cat=vco&model=ROS-2150VW**
National Semiconductor's *WEBENCH* (an excellent online PLL modelling program): **wireless.national.com/**
Analog Devices ADIsimPLL Version 2.0: **forms.analog.com/Form_Pages/RFComms/ADIsimPLL.asp**
Mini-Circuits application notes for VCOs and other components: **www.minicircuits.com/application.html**
AVR-GCC (*C++* compiler for Atmel microcontrollers): **www.avrfreaks.net/AVRGCC/**

Table 4

Loop filter component values

$C212_{\mu F}$	= 1E6 • Cx	(0.98 µF)
$C213_{\mu F}$	= 1E6 • Cx * (T1 / (T2 - T1))	(0.11 µF)
$C216_{\mu F}$	= 1E6 • C3	(0.1 µF)
$R208_{\Omega}$	= 1E6 • T2 / (C212 + C213)	(152 Ω)
$R209_{\Omega}$	= 1E6 • T3 / C216	(81 Ω)

Licensed since 1983, John Miles is an independent software and systems consultant in Seattle, Washington. John's personal and professional interests range from digital communications to RF and microwave homebrewing, as well as embedded and PC-based test and control systems. His software-development background has included projects for companies such as Rockwell-Collins and Microsoft.

Richard Hosking has been a hobbyist in radio and electronics for 35 years, since his school days. Professionally, he has pursued a medical career and currently works as a primary care physician in Perth, which is the capital of Western Australia. He holds a primary medical degree [Bachelor of Medicine, Bachelor of Surgery (Melbourne)], a Fellowship of the Royal College of Surgeons of Edinburgh and a Fellowship of the Royal Australian College of General Practitioners. His electronic interests include QRP RF design and microcontrollers. Other interests are environmental issues and backpacking. □□

Dominant-Element-Principle Loaded Dipoles

Get rid of your old dipole traps! A new design technique makes trap look-alikes do double duty. Each sets resonance for two bands and the whole wire radiates on every band.

By Al Buxton, W8NX

This article and the accompanying computer programs introduce a new, efficient category of multiband antennas to the radio amateur fraternity. Many amateur transceivers are of the single black-box type with a built-in antenna tuner to cover all high frequency amateur bands. It would be desirable for the sake of both simplicity and appearance to connect such a multiband transceiver to a corresponding multiband antenna. Unfortunately, many hams simply sacrifice operating privileges on too many of our authorized bands for lack of a good all-band antenna.

There are many approaches to attaining a multiband antenna, all with varying degrees of success. All resonant antenna approaches suffer penalties of reduced bandwidth as the price for any additional band of operation. Nonresonant antenna approaches such as random wires or loops pay the penalty of being unsuitable for low-impedance current feed provided by fully shielded coaxial feed lines. They require ladder line or open-wire feeders giving rise to feed line radiation, RF in the shack and high voltage ratings of the capacitors and inductors in the attendant transmatch. The dominant-element principle (DEP) minimizes such penalties and maximizes the number of bands that may be covered with a single antenna. Maximum bandwidth and multiband operation are attained by dominant-element-principle dipoles, which take full advantage of both the fundamental and odd-harmonic resonances of long-wire dipole antennas. Indeed, the new dominant-element-principle dipole antenna, implemented with parallel L/C load elements and short hanging stubs properly distributed along the antenna, both shifts and doubles the number of such fundamental and odd-harmonic frequencies. A computing algorithm that feeds back antenna input reactance to adjust each respective dominant element of the antenna enables a computer to solve for the entire antenna configuration, even for antennas of high complexity. The accuracy of the computer solution is as accurate as the analytical model of the antenna input impedance.

It has long been known that every ordinary long-wire dipole antenna has a fundamental resonant frequency as well as a series of both odd and even order harmonics. Fig 1 is an idealized plot of long-wire dipole input impedance as a function of frequency. It covers a wide range of frequencies from the fundamental out to the 11th harmonic. Notice that the resistance scale is logarithmic to expand the useful

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low-resistance input impedance region for clarity. Frequency increases in a clockwise motion around the spiral. Notice that the input impedance of the antenna at its fundamental resonant frequency, *F1* and all of its odd-harmonic resonant frequencies: *F3*, *F5*, *F7*, *F9* and *F11*—indicates this antenna could be suitably fed with a 75-Ω coaxial cable. Notice that the SWR on the 75-Ω feed line would be less than 3:1 at the fundamental and all odd-harmonic frequencies. The convenience and safety of fully enclosed wires and the zero RF outside shield voltage of coaxial feed lines is very desirable. The even-order harmonics with input impedances of thousands of ohms are unsuitable for operation with coaxial cable. The trick for radio amateurs is to make the fundamental and odd-harmonic frequencies match those assigned by the FCC to the Amateur Radio service. The dominant-element principle performs this trick.

Dominant-Element-Principle (DEP) Dipoles

DEP dipoles are made up of wire or tube radiating segments, hanging stubs and parallel L/C load elements, all of systematically determined values. These load elements are distributed along the dipole in a special sequence. The dipole configuration is symmetrical about the feed-line connection, having mirror symmetry of the left and right monopoles. For each monopole, the first load element out from the feed is a hanging stub—if there is one. Next comes the sequence of one or more radiating wire segments and parallel L/C load elements. Proceeding outward from the feed, the sequence of load-element resonant frequencies goes from the lowest frequency to the highest. This is the reverse order from that of ordinary trap dipole antennas. Despite the fact that every element of the dipole makes some contribution, however slight, to every resonant frequency of the dipole, one element is dominant at any specified frequency and has more effect on resonance than any other element. Therefore, the value of each dominant element may be adjusted to give antenna resonance at its corresponding operating frequency. An iterative computer algorithm using very weak negative feedback of antenna input reactance adjusts the value of each dominant element at its respective frequency. The computer program starts with an estimated antenna configuration and converges on a design solution for the antenna wherein the input reactance at all chosen operating frequencies approaches an acceptable minimum value, perhaps close to zero. The computer solution does not converge to a high-impedance even-order harmonic solution because the slope of the input-reactance function for long-wire dipoles at even harmonics is negative, whereas the slope at odd harmonics is positive.

Mathematicians studying this algorithm will immediately see the similarity of this algorithm to Newton's method of finding roots of high-order polynomial equations. However, the computer algorithm uses this method in an inverse manner: It sets the roots where we want them to be, rather than simply find the roots.

Every DEP dipole has an order of dominance of its elements in tuning the dipole to its set of operating frequencies. The orderliness of the dominance is very pronounced. The first L/C load elements (closest to the feed) induces a pair of fundamental operating frequencies. The second load elements, if used, induce a pair of third harmonic operating frequencies. The third load elements, if used, induce a pair of fifth harmonic operating frequencies, and so on. (A DEP dipole using four pairs of load elements has been designed for all-band operation from 160-10 m.[1])

The lower fundamental operating frequency sets the required inductance of the first load element, and the higher fundamental operating frequency sets its capacitance. The inductance of the third load element is fixed by the lower third harmonic frequency and the capacitance is fixed by the higher third-harmonic frequency. Proceeding from inner radiating elements to outer radiating elements, the lengths of the radiating segments are also dominant at their respective frequencies starting from the next highest odd-harmonic frequency of the load elements to still

[1]Notes appear on page 30.

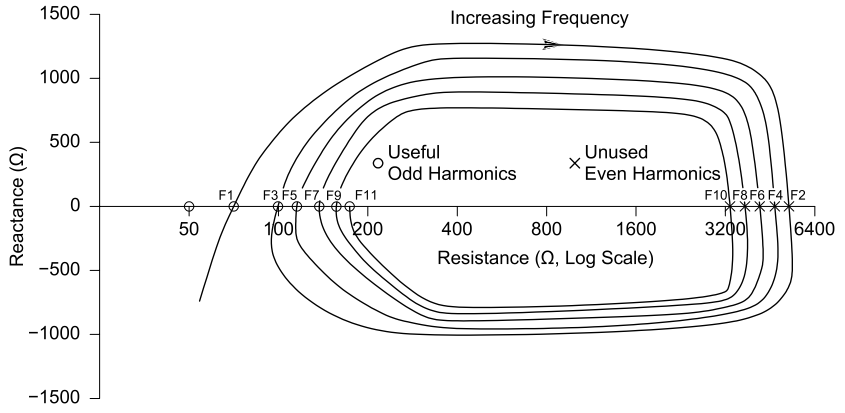

Fig 1—The input-impedance spiral of a long wire dipole.

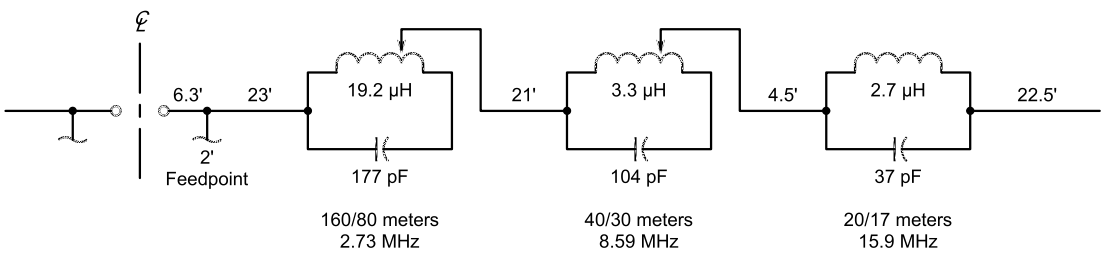

Fig 2—A DEP eight-band dipole.

higher odd-harmonic frequencies. However, the lengths of the radiating elements as dominant elements are sometimes sacrificed for the purpose of minimizing modal cross coupling in the antenna, easing the convergence to a solution. Also, sometimes there is no legally assigned amateur frequency that relates to the lengths of the radiating elements, creating unusable elements of design freedom and forcing omission of some of the odd harmonics within the sequence.

DEP dipoles are more clearly defined by example. Fig 2 shows my present eight-band working DEP dipole employing three pairs of parallel L/C loads and one pair of hanging stubs. The values shown are those after fine-tuning experimentally. As shown in Fig 2, the loads look the same as conventional traps inserted into the antenna, but they differ in an essential way. Notice also the lowest-frequency loads are closest to the feed line and the highest-frequency loads are farthest out from the antenna feed. The medium-frequency loads are located between the low and high-frequency loads. The sequence of load locations is the reverse of that in conventional trap dipoles. Moreover, the loads do not approximate open switches at the operating frequencies. With a few exceptions in the *DEP4BD* and *DEP5BD* dipoles, they are all nonresonant and simply act as either equivalent inductors or equivalent capacitors, depending on the operating frequency. At frequencies below load resonance, they are inductors, increasing the effective electrical length of the antenna. Conversely, at frequencies above load resonance, they look like capacitors, shortening the electrical length of the antenna. They do not disconnect the outboard portions of the antenna. The entire length of the antenna radiates on all bands. With certain exceptions, the load resonant frequencies are located about halfway between the frequencies of the two bands where they apply their major loading effect. Their load reactance and rate of reactance change with frequency is low in their respective bands of operating frequencies. Thus, there is less forcing or loading of the antenna than with traps and only low characteristic impedance loads (low L/C ratios) are needed. The low L/C ratios may be implemented by use of tapped output, double coaxial load elements. If you wish, open air inductors and weatherproof fixed capacitors may be used. If these three pairs of load elements were used in the classic manner of traps, the antenna could have covered only four bands. The loading technique of this DEP loaded dipole is twice as efficient as traps in producing additional bands. Building a similar antenna using classic traps would have required seven pairs of traps and would have greatly diminished the useful bandwidth on all bands.

The dipole thus has two different fundamental frequencies as well as a series of double odd-harmonic frequencies. The eight-band DEP dipole has fundamentals at both 1.9 and 3.85 MHz, third harmonics at 7.175 and 10.125 MHz, fifth harmonics at 14.175 and 18.1 MHz, a single seventh harmonic at 21.225 MHz and finally a ninth harmonic at 28.4 MHz. In short, eight amateur bands are covered—all the HF bands between 160 and 10 meters with the exception of 12 meters.

Fig 3 shows the reactance plotted versus frequency of the 160/80 m load elements resonant at 2.72 MHz. Notice the reactance is positive (inductive) for frequencies below the 2.72 MHz resonant frequency and negative (capacitive) for frequencies above resonance. Remember inductive loading increases the equivalent electrical length of the antenna and capacitive loading shortens the electrical length of the antenna. At 1.9 MHz, they have a reactance of 460 Ω (inductive), thereby raising the electrical length of the dipole from its physical 154-foot length to an equivalent 245-foot length—the length of a standard 1.9 MHz wire dipole. Conversely, at 3.8 MHz they have a reactance of –483 Ω (capacitive), which shortens the equivalent electrical length of the dipole to 123 feet, the length of a standard 3.8 MHz dipole. The lengthening and shortening action of the other load elements is similar at their respective dominant-element frequencies.

Summarizing, only three pairs of load elements and a pair of very short 10-m loading stubs were added to the 154-ft long center-fed wire dipole to tune the antenna to its eight frequencies. If the traditional trap dipole approach had been used to create an eight-band dipole, seven pairs of traps would have been required. The DEP approach is twice as efficient as traps in creating multiband operation. The innermost pair of load elements—parallel 19.2-µH inductors and 178-pF capacitors—tune the antenna to its 160- and 80-m frequencies. The middle pair of load elements—parallel 3.3-µH inductors and 104-pF capacitors—set the 40-m and 30-m frequencies. The outermost pair of load elements—parallel 2.7-µH inductors and 37-pF

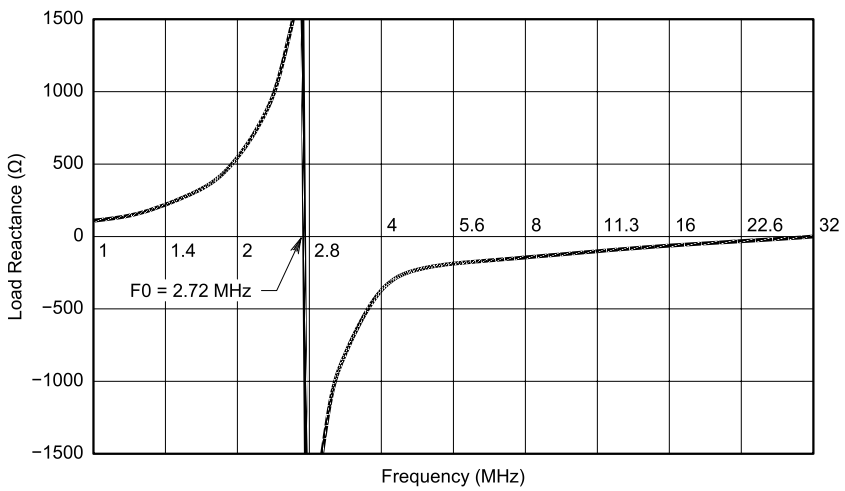

Fig 3—A plot of load reactance versus frequency for the 160/80 load element.

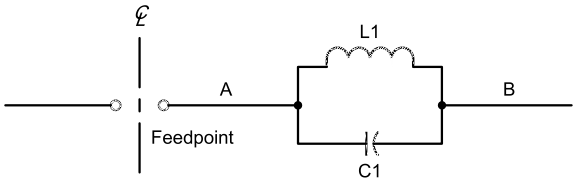

Fig 4—Various four-band DEP dipoles.

capacitors—tune the antenna to its 20-m and 17-m frequencies. The short hanging stubs tune the antenna to its 10-m frequency.

Table 1 shows the relationships between the unloaded and the loaded frequencies of the dipole. The unloaded frequencies are the resonant frequencies the dipole would have if all the load elements and stubs were eliminated. The dipole would then be an ordinary dipole, each leg of 77 feet length. While every dipole element Affects every resonant frequency to some extent, the respective load elements dominate strongly in their respective bands. Note the 3.13 MHz unloaded fundamental frequency turns into two fundamental frequencies at 1.92 and 3.86 MHz, mostly because of the dominant effect of the 160/80-m load element. Similarly, the 9.52 MHz unloaded third-harmonic frequency is replaced by two third-harmonic frequencies at 7.18 and 10.125 MHz; mostly because of the dominance of the 40/30-m load element. Likewise, the 15.92 MHz fifth-harmonic frequency is replaced by two fifth-harmonic frequencies at 14.175 and 18.1 MHz; mostly due to the dominance of the 20/17-m load element. The seventh harmonic unloaded frequency at 22.32 MHz is reduced to 21.225 MHz by the combined effect of the short 10-m stubs and stray capacitance of all the load elements. The ninth harmonic unloaded frequency is slightly lowered by the stubs and load elements to 28.4 MHz.

Choices of DEP Dipoles

There are many choices of DEP dipoles available (and more may be discovered). The simplest, having four-band capability, utilize two pairs of radiating wire segments and one pair of parallel L/C load elements. The loads may be made either of coax (RG-58 or RG-58A) or open inductors in parallel with fixed high-voltage precision weatherproof capacitors. The output connection may be tapped some distance up the coil to facilitate non-standard values of capacitance.

DEP dipoles range in complexity from simple four-band antennas to those with four pairs of load elements and coverage of all nine HF bands from 160-10 meters. The 80/40/17/10-m dipole of Fig 4 was featured in the July, 1996 *QST*,[2] but it was not recognized as a DEP dipole at the time. The full recognition and statement of the dominant-element principle, as such, was not made until 2002. This article presents its first published statement.

Fig 5 shows a group of five- and six-band DEP dipoles. The five-band dipoles differ from four-band dipoles by the addition of a pair of stubs. Also, the loads are resonant slightly above the high fundamental frequency rather than between the two fundamental frequencies. Six-band dipoles employ two pairs of load elements but use no stubs. This configuration can theoretically cover seven bands, but unfortunately at least one will be slightly outside the closest assigned amateur band. The 160/80/40/30/20/15-m six-band dipole was used at my station for over two years before it was succeeded by the present eight-band 160/80/40/30/20/17/15/12 antenna.

The eight-band DEP dipole is again shown in Fig 6, showing the values before experimental fine-tuning. It is the best of all the DEP dipoles so far discovered. The bandwidth penalties associated with multiband operation are surprisingly less than I thought they would be. The bandwidth penalties on 30 and 17 m are mitigated by

Table 1

Unloaded Frequency (MHz)	*Harmonic*	*Rin (Ω)*	*Loaded Frequency (MHz)*	*Harmonic*	*Rin (Ω)*
3.13	1	65	1.92	1	43
			3.86	1	83
9.52	3	102	7.18	3	83
			10.125	3	270
15.92	5	124	14.175	5	128
			18.1	5	360
22.32	7	143	21.225	7	158
28.71	9	159	28.4	9	165

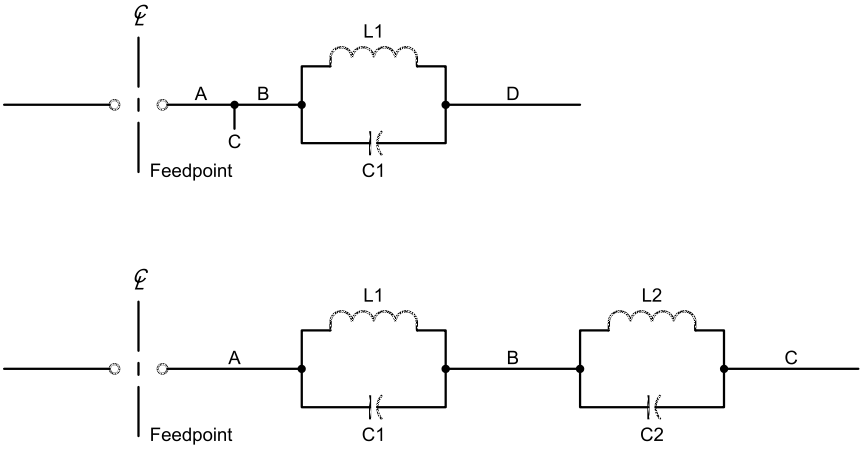

Fig 5—Five- and six-band DEP dipoles.

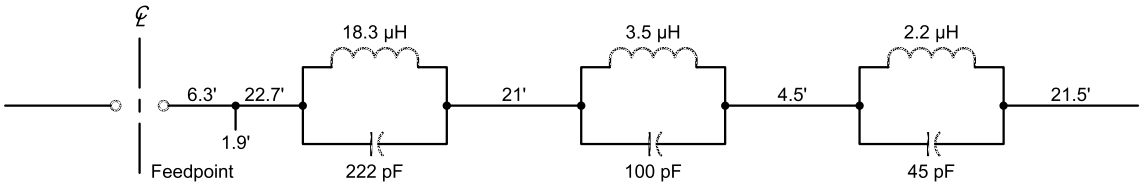

Fig 6—The eight-band DEP dipole (160/80/40/30/20/17/15/10 m).

the very narrow bandwidth of these assigned bands. The SWRs are all manageable by the built-in automatic antenna tuner of my transceiver. The antenna is compatible with my linear amplifier when used in conjunction with my high power 1500 W antenna tuner. The antenna has the conventional multilobed radiation patterns of long wire dipoles. It is not competitive with my 20/15/10-m rotatable beam on those three bands, but it fills a gap, easily permitting me to work worldwide DX on 17 m. The coverage of the lower-frequency bands, 160-30 m, is especially desirable as we approach the downside of the 11-year sunspot cycle.

The SWR curves of the *DEP8BD* dipole are shown in Fig 7 (lower bands) and Fig 8 (higher bands). With the exception of the 30-and 17-m bands, the minimum SWRs are all below 3:1. The automatic antenna tuner in my FT-990 keeps the transmitter happy across major portions of all eight bands, with some favoring of the phone bands.

These curves are for the antenna installed as an inverted V, with heights of 47 feet at the apex and about 18 feet at each end. The bandwidth penalties were much less than I feared they would be. The worst-case SWR is for the 17-m band where the antenna's input resistance is unexpectedly above 325 Ω. However, the tuner pulls the antenna right in, so the transceiver thinks it is working into a 1:1 SWR clear across the narrow band. Similarly, on 30 m, the antenna's input resistance is higher than anticipated. The minimum SWR on 160 is slightly above 2:1, because of the low input resistance of the low, short antenna. It has an effective bandwidth of about 80 kHz on 160 m. The antenna favors the phone portion of the 80-m band, but coverage extends below 3.75 MHz into the CW portion.

This series of DEP dipoles would not be complete without showing the nine-band DEP dipole covering every band from 160-10 m. All-band coverage requires four pairs of load elements but no stubs. Unfortunately, the fourth pair of load elements adds 12 m but significantly decreases bandwidth on both 15 and 10 m. The tradeoff for going from eight-band operation to all-band operation is not advantageous. The law of diminishing returns seems to have taken over at nine-band operation. However, somebody may want to build it anyway. After all, it truly is an all-HF-band ham antenna with genuine low-impedance current feed. Making and testing one would provide further confirmation of the dominant-element principle.

Initial Configuration Estimating

Design of DEP dipoles starts with an appropriate configuration and estimated values of all the load and radiating elements. These estimates are not obtained by pure guesswork even though there remains trial and error in making them. For the computer design programs to converge to a solution from the initial estimates, several constraints exist that must be accepted and used as guidelines. First, a design solution must exist. Not all desirable antennas can have a physical reality. For instance, the laws of physics fix the rate of change of input reactance with frequency. Therefore, chosen bands of operating frequencies must have proper constraining limits on their separation. Further, the chosen set of operating frequencies must be within those frequency bands that

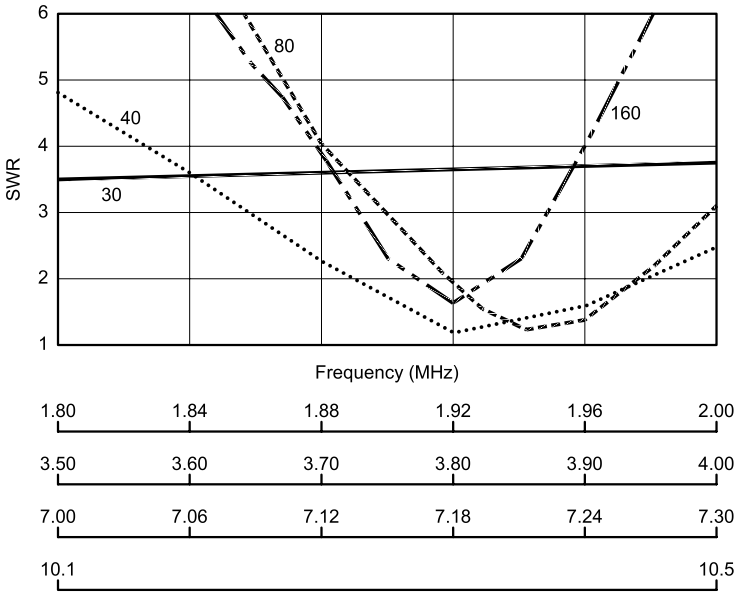

Fig 7—Low-band SWR curves for the eight-band DEP dipole.

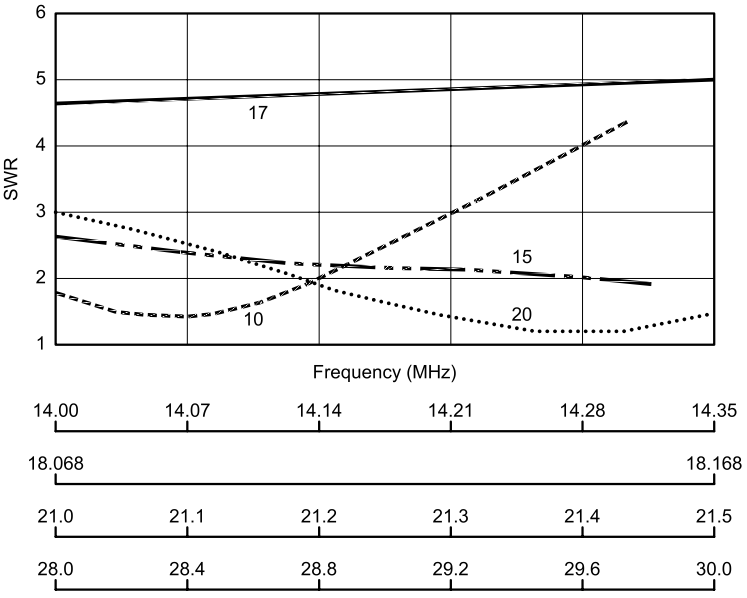

Fig 8—High-band SWR curves for the eight-band DEP dipole.

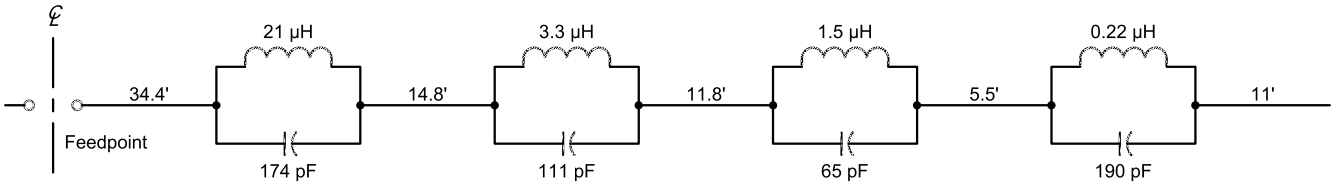

Fig 9—A nine-band DEP dipole (160/80/40/30/20/17/15/12/10 m).

the FCC rather arbitrarily assigned to the Amateur Service years ago. One may ask what is the probability that the FCC-assigned bands would have the proper frequency separation? It is just serendipitous that proper separation exists for the amateur bands for a large number of DEP dipoles.

First, consider the compatibility of the set of operating frequencies with each other. This constraint shows up in the following empirical monopole equivalent-electrical-length equation:

$$meel = \frac{983.57(n-0.05)}{4 f_{\mathrm{MHz}}} = Zphysical + Zloading \qquad \text{(Eq 1)}$$

where:

meel = the monopole equivalent electrical length of each monopole, in feet.

Zphysical = the physical height of an equivalent vertical radiator above a perfect ground plane, in feet.

Zloading = the contribution in electrical height made by the load elements, in feet.

983.57 = wave propagation velocity, in feet/microsecond.

f_{MHz} = the frequency in megahertz.

n = the order of the harmonic frequency.

(n–0.05) = the nominal length factor where the –0.05 term is caused by fringing of the electrical field at the end of the antenna.

Of course, *meel* is also equal to the physical height of an unloaded vertical monopole of the same frequency above a perfect ground plane. If the *meel*s for the various operating frequencies are spread too far apart, then convergence may be impossible. The load elements may simply be unequal to the task of pulling the antenna into resonance.

Further constraint is imposed by the desirability to equalize the loading bandwidth penalty in the two dominant-frequency bands by keeping the resonant frequency of all loads near the geometric mean of their two respective dominant frequencies. However, the dominant-element principle is still applicable and usable where the loads are tuned a few percent above the high fundamental frequency, as will be illustrated later in this section. Likewise, there is the desirability of using very low characteristic-impedance loads to reduce the bandwidth penalty in both bands. Hopefully, the L/C ratios of all load elements may be made to correspond to a characteristic impedance of less than 500 Ω—where lower is better from a bandwidth-conservation point of view. These constraints are met by the convergence algorithm, which sets the exact values of L and C for each load. Thus, they are useful guidelines for estimating the initial configuration needed by the convergence algorithm. These constraints give us the following equations for the initial values of L and C for the loads:

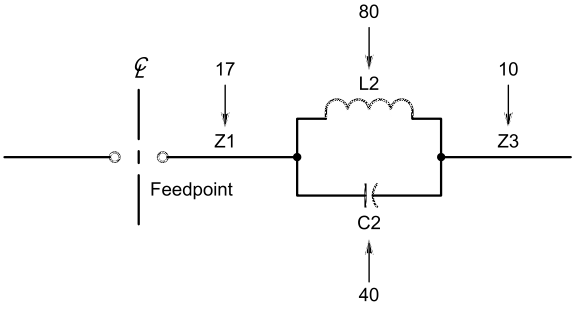

Fig 10—A simple 80/40/17/10 m dipole. The arrows indicate dominant elements.

$$L = \frac{Z_0}{2\pi f_{\mathrm{MHz}}} \qquad \text{(Eq 2)}$$

$$C = \frac{1{,}000{,}000}{2\pi Z_0 f_{\mathrm{MHz}}} \qquad \text{(Eq 3)}$$

where:

L = inductance of the load, in microhenries.

C = capacitance of the load, in picofarads.

Z_0 = assumed trial characteristic impedance, generally between 100 and 500 Ω.

f_{MHz} = geometric mean of the two dominant load frequencies in megahertz.

Let's apply these guidelines in a couple of examples. First is the simplest DEP dipole: a four-bander with only four elements of design freedom, one for every band of operation (see Fig 10). The dipole is symmetrical about the feed line. The arrows show the dominant relations. The input reactance of the antenna at the 80-m design frequency is reduced to zero by adjusting the size of the load inductance *L2*. Similarly, the input reactance of the antenna at the 40-m design frequency is reduced to zero by adjusting the load capacitance, C2. Likewise, the length of the innermost radiating element, *Z1*, tunes the antenna to resonance on 17 m; and the length of the outer elements, *Z3*, brings the antenna into tune on 10 m. These adjustments are all cross coupled to some extent, but the orderly element dominances of DEP dipoles permit us to unscramble the cross coupling effects via a computer program incorporating very weak, iterative negative-feedback algorithm.

Begin the task of making the estimates of the initial values of the four elements of each monopole. First, choose preferred operating frequencies in the four bands. For this example, let's choose 3.8, 7.15, 18.1 and 28.6 MHz. The antenna will have two fundamental frequencies at 3.8 and 7.15 MHz. There will be third-harmonic operation on 18.1 MHz and fifth-harmonic operation on 28.6 MHz. Phone operators may prefer different design frequencies from those of CW operators. If you don't like those frequencies, choose your own and redo the calculations.

Since the L/C load elements will be tuned to about 5.2 MHz (the mean

of 3.8 and 7.15 MHz), they will have very little loading effect on 10 m at 28.6 MHz, giving *zloading* = 0. Therefore, the overall length of each monopole is best estimated by the *meel* of Eq 1 applied for fifth-harmonic 10-m operation at 28.6 MHz:

$$meel \quad Z1+Z3 \quad \frac{983.57(5-0.05)}{4(28.6)} \quad 42.5 \text{ ft} \qquad \text{(Eq 4)}$$

Next, assuming the loads will be located somewhere near the middle of each monopole, giving *InitialZ1*= *InitialZ3*= 42.5/2= 21 feet in rounded off numbers for initial estimates of the length of each radiating element.

You may wish to calculate the *meel*s for the other operating frequencies with the same equation to get an estimate of the amount of loading equivalent lengths:
at 3.8 MHz,

$$meel \quad \frac{983.57(0.95)}{4(3.8)} \quad 61.5 \text{ ft} \qquad \text{(Eq 5)}$$

at 7.15 MHz

$$meel \quad \frac{983.57(0.95)}{4(7.15)} \quad 32.7 \text{ ft} \qquad \text{(Eq 6)}$$

at 18.1 MHz,

$$meel \quad \frac{983.57(0.95)}{4(18.1)} \quad 40.1 \text{ ft} \qquad \text{(Eq 7)}$$

These *meel*s tell us that the inductive loading for 3.8-MHz operation must add 61.5 – 42.5 = 19 ft of length to each monopole. On 7.15 MHz, the capacitive loading must be the equivalent of 32.7 – 42.5 or – 9.8 ft. On 18.1 MHz, the load element is only very slightly capacitive, changing the length by 40.1 – 42.5 = –2.4 ft. Experience shows that all of these loading values are acceptable without sacrificing too much bandwidth on any of the bands.

Next, determine estimates of the *L* and *C* of the load. Assuming a characteristic impedance of 350 Ω for the load and using Eq 2, we get:

$$InitialL2 \quad \frac{350}{2\pi 5.2} \quad 10.7 \text{ µH} \qquad \text{(Eq 8)}$$

and using Eq 3:

$$InitialC2 \quad \frac{1{,}000{,}000}{2\pi(350)5.2} \quad 87.4 \text{ pF} \qquad \text{(Eq 9)}$$

Of course, we would probably round off the numbers to, say, 10 µH and 90 or even 100 pF. These initial estimates are close enough to permit successful convergence to the accurate final values of the four elements of each monopole. If successful convergence had not been achieved, we would have repeated the calculations using either higher or lower assumed values of characteristic impedance. It is interesting to compare the final solved values of the load and radiating elements with the initial estimated values to get a feel for the tolerance of the DEP method to initial configuration errors. To make this comparison, use the print option during the computer run to print the specifications of the designed antenna. Unfortunately, more complex antenna configurations have less tolerance to errors in the estimated initial configuration.

When making a computer run, you may also choose the option to monitor the convergence process on an iteration-by-iteration basis. This may give clues to why convergence was not attained, such as conflict between harmonic operation of differing orders. Watch the individual antenna input reactance for such conflicts. These conflicts can sometimes be eased by appropriate changes of operating frequency—or watch the overall convergence parameter, σ, which is the rss of the antenna's input reactance for the entire set of operating frequencies. However, monitoring step-by-step is a slow and tedious process, and you may prefer not to monitor in this manner. With lower gains in the negative-iterative-feedback algorithm, the algorithm is more tolerant of highly inaccurate initial configuration estimates. The expense is slower convergence, requiring more iteration to reach the solution. Up to 1000 iterations are used for the most complex antenna configurations.

Let's look at another, more complex example of initial configuration estimating: a six-band DEP dipole using two pairs of load elements and three pairs of radiating elements (see Fig 11). This configuration is interesting because the configuration has seven elements of design freedom with only six operating bands. If amateurs still had the 11-m band, this antenna could have covered seven bands. The extra element of design freedom is used to minimize a cross coupling conflict between the fifth-harmonic 20-m band and the seventh-harmonic 15-m band. That saves a little bandwidth in each band, aids the convergence process and slightly relaxes the tolerances on the estimated initial configuration.

The inner pair of load elements dominates on 160-m and 80-m operation, the outer pair on 40-m and 30-m operation. The 15-m band is the most removed from the effects of the loads and therefore the overall length of each monopole is set by the *meel* at 21.15 MHz, giving:

$$meel \quad Z1+Z3+Z5$$
$$\frac{983.57(6.95)}{4(21.225)} \qquad \text{(Eq 10)}$$
$$80.8 \text{ ft}$$

and

$$meel \quad \frac{983.57(4.95)}{4(14.25)} \quad 85.4 \text{ ft} \qquad \text{(Eq 11)}$$

These two *meel*s show a basic conflict between 15 and 20-m operation. Both the 160/80 and 40/30 load elements are being operated well above their resonant frequency so their shortening effect is slight. However, what is needed is a relative lengthening effect on 20 m of about five feet. The way out of this dilemma comes through the stray capacitance of both pairs of load elements acting as shunt capacitance to ground. The stray capacitance of the 160/80 load is about 4.5 pF, that of the 40/30 load about 3 pF. These stray capacitances sufficiently lengthen the antenna on 20 meters, both loads in close enough proximity of 20-m voltage maximums.

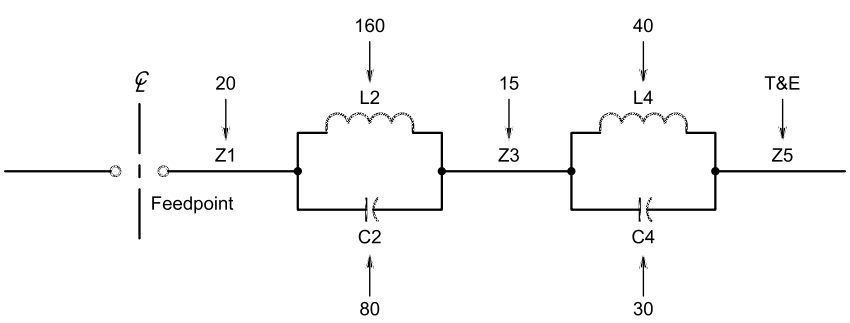

Fig 11—A six-band DEP dipole (160/80/40/30/20/15 m). The arrows indicate dominant elements.

The choice of a 33-ft length for *Z5* and the 28-ft length of *Z3* determined by the convergence algorithm thus supplies the lengthening needed on 20 m. These load stray capacitances, acting as hidden shunt elements to ground, become additional useful lengthening loading elements.

This phenomenon shows the vital necessity for having an accurate representation of the load stray capacitance in the analytical model of the antenna. The load stray capacitance effect is also magnified further when the loads have parasitic resonances not far enough above their normal resonant frequency. Large, low-frequency loads may thus have a surprisingly great effect at much higher frequency operation, especially if the stray capacitance is magnified by parasitic resonance.

The length *Z5* being 33 feet leaves (80.8 – 33 = 47.5) or 47.8 feet for the sum *Z1* + *Z3*, which if split evenly gives:

$$InitialZ1 \quad InitialZ3 \quad 23.9 \text{ ft} \qquad \text{(Eq 12)}$$

A trial of these values shows they do not give good convergence, so try shortening *InitialZ1* to 20 feet and lengthening *InitialZ3* to 28 feet.

The initial *L* and *C* values for the loads will now be determined. First, the 160/80 load, whose resonant frequency is assumed to be the mean of 1.9 and 3.8 MHz, or 2.68 MHz. Also, assume a characteristic impedance of this load of 250 Ω. Applying Eq 2 gives:

$$L2 \quad \frac{250}{2\pi\, 2.68} \quad 14.8, \text{say } 15\ \mu\text{H} \qquad \text{(Eq 13)}$$

Applying Eq 3 gives:

$$C2 \quad \frac{1{,}000{,}000}{2\pi(250)2.68} \quad 237.5, \text{say } 230 \text{ pF} \qquad \text{(Eq 14)}$$

Repeat these calculations for *L4* and *C4* of the 40/30-m load element using your own set of assumed load resonant frequency and characteristic impedance. Trial and error will show the initial values for *L4* and *C4* are near 4 μH and 100 pF, respectively.

You now are set for a *DEP6BD* program run either using these initial estimates for the configuration or accepting the default values for the default antenna in the program. You may want to calculate some other estimated initial values based on other assumed load characteristic impedances.

Two DEP dipoles employing the alternative method of tuning the loads to a frequency slightly above the high fundamental frequency will now be discussed. They both satisfy the *meel*, criteria, differing only in the load-tuning criteria from other DEP dipoles. Consider the 80/40/20/15-m dipole of Fig 4. Notice the *L* is 6.6 μH and *C* is 69.2 pF, corresponding to a load resonant frequency of 7.447 MHz, about 4 % above the middle of the 40-m band. Similarly, the 80/40/20/15/10-m five-band DEP dipole of Fig 6 has a load inductance of 6.3 μH and a load capacitance of 77.7 pF. The load resonant frequency is 7.193 MHz, about 0.6 % above the middle of the 40-m band. One might consider these DEP dipoles as ordinary trap dipoles. However, they were designed according to the dominant element principle; and with the exception of the high fundamental frequency, the loads do not truncate the outboard radiating elements. The entire length of all the elements on all other bands act as radiators. Unfortunately, the loads of the 80/40/20/15-m dipole tuned 4% above the middle of the 7.15 MHz frequency cause rather rapid change of load reactance with frequency, and there is significant loss of bandwidth on 40 m.

Tweaking the Design

As is the case with all antenna design, experimental fine-tuning can improve upon DEP designed antennas. The accuracy of the DEP design programs is limited by the accuracy of the input impedance analytical model of the programs. There are simply too many unknowable factors for the analytical model to have absolute accuracy. The model assumes free-space operation, and this is a cause of error, especially for the lower frequency bands where ground effects can lower the frequency by two or three percent. Thus a 160-m design frequency at 1.9 MHz will usually result in resonance at perhaps 1.85 MHz when the antenna is installed at, say, 40 or 50 feet. However, the ground will much less affect the higher frequencies of the antenna. A second source of error is the stray capacitance of the loads to ground, which is empirically approximated in the analytical model to an accuracy of perhaps one picofarad. This small amount of capacitance error can produce small but significant error at the higher frequencies of the antenna. Thirdly, a small but significant error arises in the assumption of standard "lossy" transmission-line theory, where transmission-line losses simulate the antenna radiation resistance. Other unknown errors are also believed to exist. Thus, most DEP antenna designs should be tweaked or fine-tuned experimentally.

A few tricks can be valuable during experimental fine-tuning of the antenna. First, the higher-frequency loads may be space wound, so that they may be adjusted by compressing or further expanding the turns. This type of fine-tuning the load must be done before you have stabilized the windings with PVC glue. If you have already stabilized the windings with glue, you can raise the load frequency by shorting a single turn that can be moved by sliding the bar along the turns of the load winding. Screwing the turn to the center of the load will raise the frequency a maximum amount. Screwing it to either end will raise the frequency a minimum amount. Lengthening or shortening the hang-down stubs will have maximum effect on the highest antenna frequency but slight effect on the other frequencies. Raising or lowering the ends of the antenna will have maximum effect at the antenna's lowest frequency but some effect at all frequencies.

The most sophisticated approach to tweaking the design of the antenna is to build and install the antenna exactly as specified by the computer. High accuracy in fabrication of the antenna is a requirement if this approach is to be successful. Then measure the exact minimum SWR frequencies during antenna performance and calculate the design frequency error by taking the differences between the design frequencies and the actual measured frequencies. Then make a second totally new design at frequencies adjusted for these design frequency errors. For example, if your original frequency was 1.9 MHz and the actual minimum SWR was at 1.86 MHz, make a second antenna design frequency 1.94 MHz on 160 m. Similarly, adjust all the other design frequencies.

Making Double Coax Loads

The load elements may be either double coax loads or open inductors in parallel with fixed weatherproof capacitors. However, the inherent ruggedness and weatherproof characteristics of the double coax loads is very

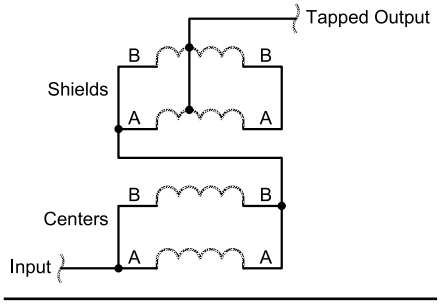

Fig 12—A schematic diagram of double coax loads.

desirable despite their somewhat greater losses. Both approaches require a tapped output to provide the necessary L/C ratios. The required value of capacitance seldom fits those available in the standard EIA capacitor values. However, the transformation capability provided by the output tap eliminates the difficulty. The transformation equations for the *L*s and *C*s referred to the output tap, sufficiently accurate for our purposes, are based on the usual square of the turns relationship. They are embedded in the computer design for both categories of loads. Run the floppy disk program, *DOUBCOAX*, for the design of double coax loads. Also, run the conventional load program, *CONVLOAD*, to familiarize yourself with it. The schematic diagram of double coax loads is shown in Fig 12.

The inductors are wound on schedule 40 PVC pipe. The pipe diameter is the builder's choice. Notice the series connection of the inner and outer shield windings constituting the inductance of the load. Also notice the parallel connections of both center conductors and both shield windings. These parallel connections and the tapping of the output permit the increased value of capacitance that is necessary to obtain the low L/C ratio loads required by the dominant-element principle. The capacitance of the load comes from the capacitance between the inner conductors and outer shield conductors, not shown because it is not essential to connection of the load. Solid center conductor, Belden RG-58 (#8240), is the preferred cable. However, stranded-center-conductor cable, Belden RG-58A (#8259), may also be used where the greater ruggedness of the stranded center conductor gives less danger of breaking the connections of the load.

Fig 13 shows the general appearance of a double coax load with wide spacing between turns. Turn spacing is recommended, at least for the higher harmonic bands, to give flexibility in making fine-tuning adjustment of the load resonant frequency. Compressing the turns lowers the frequency, expanding them raises the frequency. However, turn spacing is not a requirement and close spacing may be desirable especially for the low-frequency loads such as those intended for 160/80-m operation, where the frequency tolerance of the loads is easy to meet. Studies of optimum configuration show the diameter-to-length ratio of the loads should be close to one.

Run the *DOUBCOAX* program before studying the next few figures to get a feel for the details of double coax loads. The two coaxial cables are first laid out flat together and cut to length according to the layout in Fig 14. The dimensions marked A and B, calculated by the computer run, determine the overall length of the cable and the location of the output tap. The tabulation above the cables is for the loads of the eight-band 160/80/40/30/20/17/15/10-m DEP dipole.

Make the tap and apply the cable ties while the winding is still laid out flat in accordance with Fig 15. The taps are made from a short cannibalized length of the shield braid from the same kind of coax. Be sure the tap makes a taut encirclement of the double coax holding the tap in tension as you crimp the connector about the tap.

The tap connection is tinned copper pressing tightly on tinned copper and therefore no solder is required. If you chose to solder the tap, you may damage the polyethylene dielectric of the

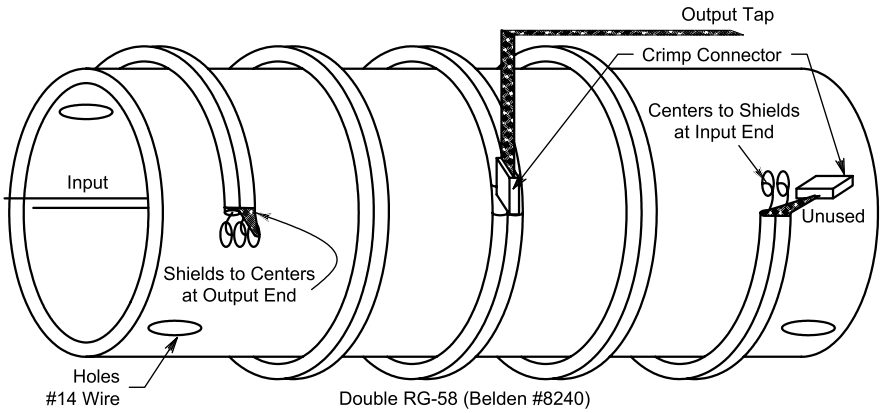

Fig 13—A double coax load (not to scale).

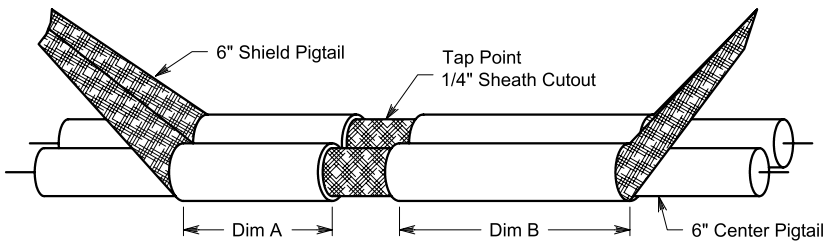

Fig 14—Layout of double coax loads. Forms are Schedule 40 PVC pipe. Coaxial cable is Belden #8240. Cable ties are not shown. Not to scale.

	Form Diameter (Inches)		*Form Length*	F_0	*Dim A*	*Dim B*
Load	*OD*	*ID*	*(Inches)*	*(MHz)*	*(ft)*	*(ft)*
160/80	3.5	3.0	5.6	2.73	7.7	1.96
40/30	2.378	2.0	5.0	8.55	2.1	1.95
20/17	1.875	1.5	4.33	15.9	1.8	0. 65

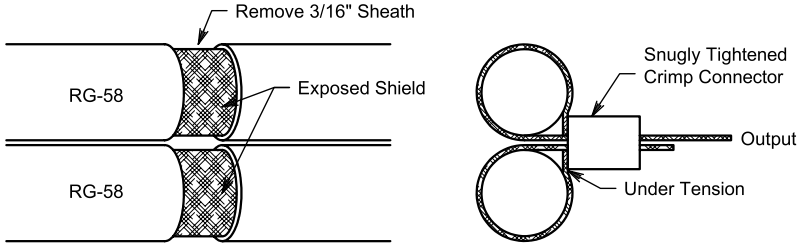

Fig 15—Details of the tap connection. The tap is made by tightly wrapping each exposed cable shield with a length of braid take from the same cable and securing the wrap ends with a crimp connector.

double coax or at least degrade the breakdown voltage of the load. I chose not to apply solder and the taps continue to make good contact after nearly two years of service. Inspection shows no corrosion or other problems developing at the tap connection. After the double cables are joined at the output tap point, lace the two cables together with plastic cable ties every few inches. You may wish to regard the cable ties as temporary aids. You can remove them after construction of the load is complete and the load windings have been stabilized by application of PVC glue to the windings and PVC-pipe coil form. If you want greater confidence in maintaining a low tap contact resistance, make the tap encircle the two cables two or more times for greater surface contact area.

Fig 16 shows the details of the forms. The tabulation applies to the forms for the eight-band DEP dipole. Notice that there are three $^3/_{16}$-inch holes in the forms at the left, or input, end of the load and only two holes at the right end. These holes are reamed into an oval shape for appearance.

Fig 17 shows the loads as they should be installed in the antenna. Notice that the input-end, consisting of the two inner conductors of the double coax leads, is toward the feedpoint of the antenna, and the output tap leads are toward the far end of the antenna. The antenna will be slightly detuned if the load terminals are reversed during installation because of the asymmetry of the load stray capacitance. Check the resonant frequency of the loads with a dip meter, and fine-tune them to within 0.5 percent accuracy by varying the spacing between turns before application of stabilizing PVC glue to the turns and forms. If you measure the Q of the loads on a Q meter, be sure to multiply the indicated Q by the factor (1 + *Cload* / *CQmeter*) to get the true Q of the load. This factor may be rather large, approaching as much as five or six for double coax cable loads. This multiplying factor must be applied because the current in the load capacitor bypasses the Q-meter current sampling resistor. It is probable that coaxial traps and loads have a bad reputation because people put them on a Q meter and were unaware of this multiplying factor.

Making Conventional Loads

Some amateurs may prefer the use of open inductors and fixed capacitors for the loads because they may have lower losses than double coax loads. However, they are significantly less rugged and are susceptible to rain, ice and snow problems causing frequency change and possible detuning of the antenna in inclement weather. Moreover, coax loads are considerably less costly. High voltage and high accuracy fixed capacitors are very expensive.

Conventional loads may be used in place of double coax loads providing their primary *L* and *C* values are equal to those of the coax loads as well as having an equivalent stray capacitance to ground. The latter equivalence means that the outer dimensions of the conventional load must be roughly equivalent to those of double coax loads. The *CONVLOAD* program may design conventional loads. Make a trial run of the program using your selected type of open inductors and fixed, high-voltage weatherproof capacitors.

The nomenclature for the design program is given in Fig 18. Fig 18A shows the loads as the maker of the

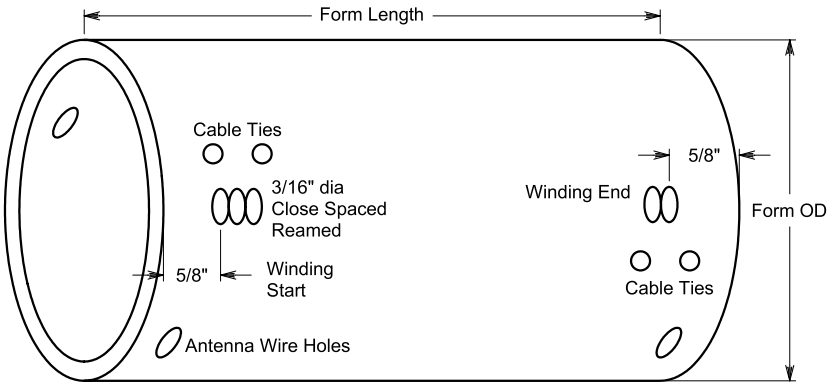

Fig 16—Load form details.

Load	F_0 MHz	Form OD Inches	Form Length Inches	Number Turns	Tap Turns	Spacing Inches
160/80	2.73	3.5	5.6	10	8	0
40/30	8.55	2.378	5.0	6	3.1	0.16
20/17	15.9	1.875	4.33	4.5	4.5	0.195

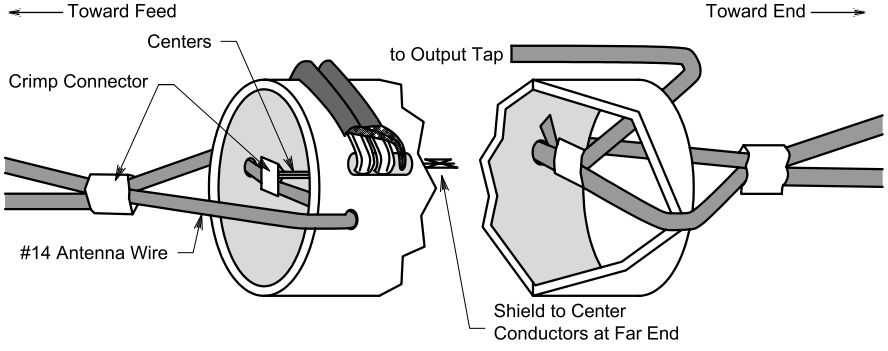

Fig 17—Load installation.

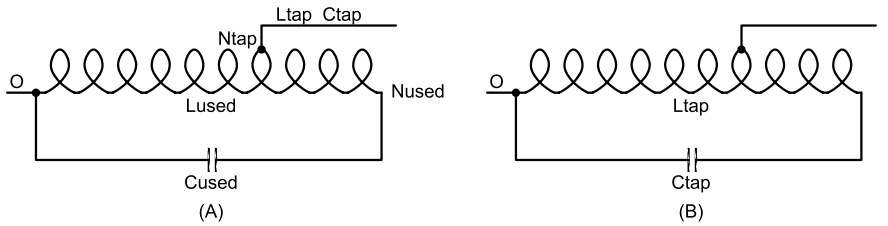

Fig 18—Nomenclature of conventional loads: (A) as built. (B) as shown in diagrams. *Lused* = total inductance (µH); *Ntap* = turns to tap; *Ltap* = Inductance referred to tap, µH. *Cused* = external capacitance, pF; *Nused* = total turns used; *Ctap* = capacitance referred to tap, pF.

loads would see the values of L and C with which he works. Fig 18B shows how they appear in the figures of the various DEP diagrams of this article, specifying the L and C values referred to the output tap. Since output is taken at a tap on the inductor, the tapped output inductance will always be smaller than the total inductance used for load. In addition, you must select a capacitor whose capacitance value is less than the required C of the load. The inductance is stepped down by tapping whereas the capacitance is stepped up by tapping.

Load-Element Stray Capacitance

Stray capacitance of the load elements is a very important consideration vitally affecting the accuracy of the analytical model of the antenna. Fig 19 shows the analytical model of stray capacitance of the loads. The combined effect of the stray capacitances of all the load elements can contribute a substantial increase to the effective electrical length of the antenna. It must therefore be accurately represented in the antenna analytical model. The load-element stray capacitance is the self-capacitance caused by the rather large bulk size of the loads. First, there is the ordinary distributed self-capacity associated with the outside dimensions of the loads. The 160/80-m loads of the *DEP8BD* dipole have a self-capacity of about 4.3 pF without considering parasitic resonance of the loads. There is a dynamic increase in this self-capacitance to 5.3 pF when it resonates in series with the distributed self-inductance of the outside shield windings of the loads. The parasitic resonance may be observed with a dip meter at a frequency perhaps 20 to 25 times higher than the primary load-element frequency. For instance, the aforementioned 160/80-m load element of the *DEP8BD* antenna has a primary resonant frequency of 2.72 MHz and a parasitic resonance at 59 MHz. The effective stray capacity of the 160/80-m loads at 28.6 MHz thus becomes[3]:

$$C_{stray} \quad \frac{1.05\left(diam^2 \times len\right)^{0.333}}{1-\left(\frac{f_{MHz}}{f_{parasitic}}\right)^2} \quad \text{pF}$$

$$\frac{1.05\left(3.695^2 \bullet 4.35\right)^{0.333}}{1-\left(\frac{28.6}{59}\right)^2} \quad 5.3 \text{ pF} \qquad \text{(Eq 15)}$$

where:

$diam$ = center diameter of cable on the form, in inches

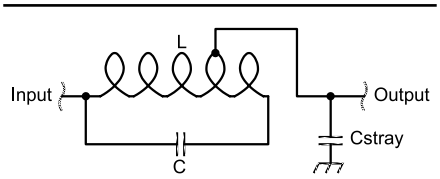

Fig 19—The load equivalent circuit.

Table 2

GW-BASIC programs for designing DEP dipoles

DEP4BD
DEP5BD
DEP6BD
DEP7BD
DEP8BD
DEP9BD
SINGCOAX
DOUBCOAX
CONVLOAD
LOADZ

len = length of the winding on the form, inches

C_{stray} = stray capacitance of the load to ground, pF

f_{MHz} = operating frequency, in megahertz

$f_{parasitic}$ = parasitic resonance frequency, in megahertz

This stray capacity is the approximate equivalent of that of a two-foot stub of #14 AWG wire hanging from the end of each of the 160-m load elements. These equivalent stubs thus have the potential to make a significant contribution to the 28.6-MHz antenna resonant frequency, depending on their proximity to voltage maximums on the antenna. The stray capacitance will have a similar, but lesser, effect on lower frequencies. The stray capacitance effects of all load elements at all frequencies are appropriately accounted for in the analytical model of all the antennas in the DEP series.

DEP Dipole Programs

The computer programs listed in Table 2 are available from ARRL (see Note 1). These programs are in *GW-Basic* 3.12,[4] otherwise known as *BASICA*, permitting the easiest and most rapid dissemination of the DEP technology. Hams are free to revise and upgrade the programs as they see fit. Leaving the programs in common *BASICA* gives immediate access to the source code and listing of the programs. Six different programs permit designing DEP dipoles of varying complexity, from the simplest four-band to the most complex nine-band dipoles. All six programs may be run using default data to demonstrate the dominant-element principle very quickly and dramatically. Programs for the design of both single and double coax load elements as well as conventional parallel inductor/capacitor load elements are supplied. A program for the calculation of the impedance of load elements is also included.

Notes

[1]Look for *DEP9BD* in the software package. You can download the package from the ARRLWeb at **www.arrl.org/qexfiles/**. Look for **0403Buxton.ZIP**.

[2]A. Buxton, W8NX, "An Improved Multiband Trap Dipole Antenna," *QST*, Jul 1996, p 32.

[3]From Fig 16, *diam* = (3.5 + 0.195) = 3.695 (0.195 inches is the diameter of Belden #8219), and *len* = 5.6 – 0.625 – 0.625 = 4.35 because the winding begins 0.625 inches in from each end of the 5.6-inch form.

[4]*GW-BASIC* is available on the Web. One source is **www.geocities.com/KindlyRat/GWBASIC.html**. □□

Boxkite Yagis

Arrays of Twin C elements provide gain at the fundamental frequency and its third harmonic.

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The elements used in the "Boxkite" Yagi are based on a derivative of the basic Twin C element. The derivation is probably easier to illustrate and understand if we back into it from a different direction. Fig 1 shows one version of a classic "Lazy H," which consists of four half-wave dipoles end fed in phase. The arrows show the current direction on each dipole; the currents are a maximum at the dipole centers. If we consider the top two dipoles, they are end fed in series via a λ/4 balanced transmission line that transforms the high impedance of the dipoles down to a low impedance at the feed point. The lower two dipoles are fed the same way, and the upper and lower halves are fed in parallel by the source. The horizontal and vertical stacking distances are both λ/2, and the element produces a bidirectional horizontally polarized field with a gain of close to 8 dBi.

If we now put a source in series with one of the feed lines and put a phase reversal in the transmission line to preserve the correct phases, we arrive at Fig 2. Notice from Fig 1 that the total length of wire in each half of the element is 3λ/2 and that the total length of the transmission-line segment is λ/2. This means that at one-third of the design frequency the transmission-line section is λ/6 long and the total length of wire in each

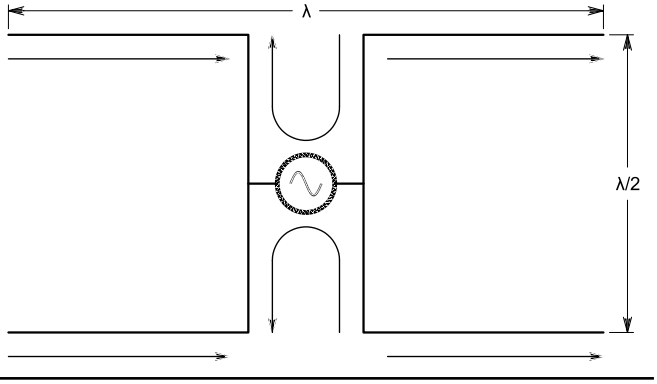

Fig 1—Lazy H antenna.

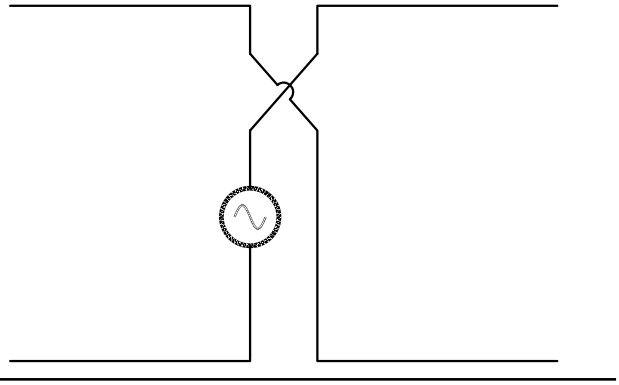

Fig 2—Boxkite element arrangement.

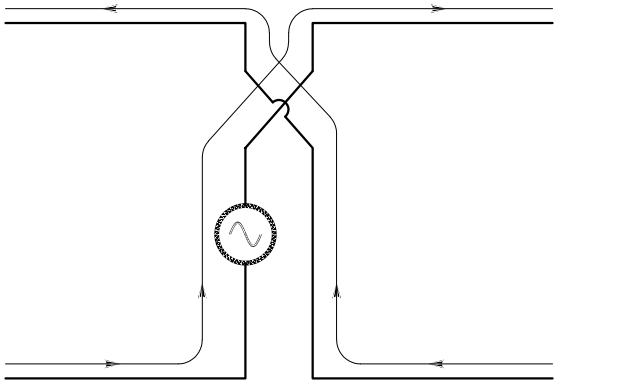

Fig 3—Boxkite element currents at *F1*.

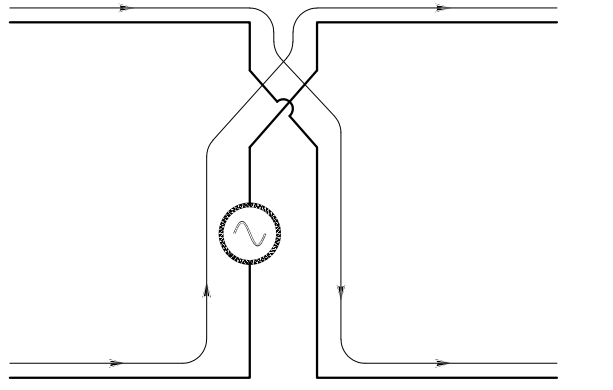

Fig 4—Boxkite element currents at *F2*.

half is λ/2. Does that sound familiar? At this frequency, the element behaves exactly like a Twin C, although the transmission-line section has been transposed and the wings straightened out. So, we end up with an element that behaves as a vertical Twin C at the lower, or fundamental, frequency and as four stacked horizontal dipoles at the third harmonic. The connection of the source in series with one leg of the transmission line raises the resonant resistance at the third harmonic to four times that of the equivalent Lazy H and permits operation of the element at the fundamental. The current flow in the Boxkite element is shown in Figs 3-5. Fig 3 shows operation at the fundamental frequency, *F1*. The currents in the horizontal sections are in antiphase, and those in the vertical transmission-line segments are in phase, so the element behaves as a vertical radiator. Fig 4 shows the current phases at *F2*. The currents in the transmission lines are now in antiphase, but the horizontal-section currents are now all in phase, so the element produces a horizontally polarized field. Fig 5 shows the current phases at the third harmonic, which we will call *F3*. Here again, the vertical fields cancel and the element produces a horizontally polarized field.

We will only concern ourselves here with operation at *F1* and *F3*, although operation at *F2* is intriguing since the models show that optimizing at *F1* and *F3* also produces excellent characteristics at *F2*, both in terms of pattern, gain and SWR. I have spent no time trying to analyze or utilize this phenomenon. It is possible that a Boxkite antenna operating at *F1* and *F2* could be very useful, since the two frequencies need not be harmonically related. The difference in frequency between *F1* and *F2* is controlled by the coupling coefficient, which we can vary over a wide range. Investigation of this must wait until I have finished other urgent projects!

There is an important point to remember about how operation on *F1* and *F3* is possible, since *F1* and *F3* can be exactly harmonically related. We know that a λ/2 dipole resonant at *F1* will exhibit third harmonic resonance at a slightly lower frequency than *F3* because the element diameter at *F3* is a larger fraction of a wavelength than at *F1*. Conversely, this means that, if the element length is reduced so that resonance is achieved at *F3*, then the element will resonate at a higher frequency than *F1*.

You will recall that the natural resonant frequency of the subelements in a Twin C needs to be somewhat

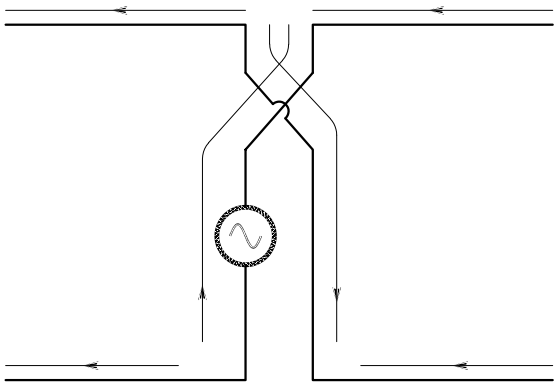

Fig 5—Boxkite element currents at *F3*.

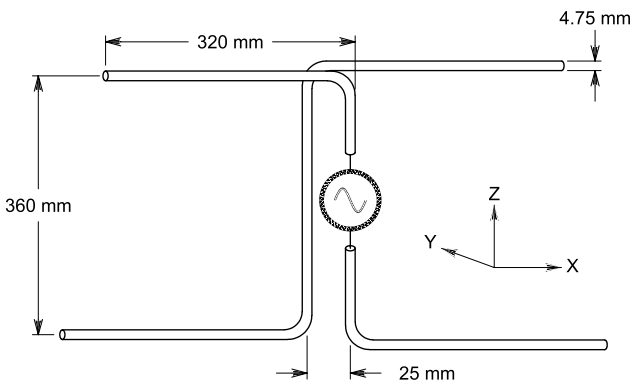

Fig 6—Physical Boxkite driven element for 2 m and 70 cm.

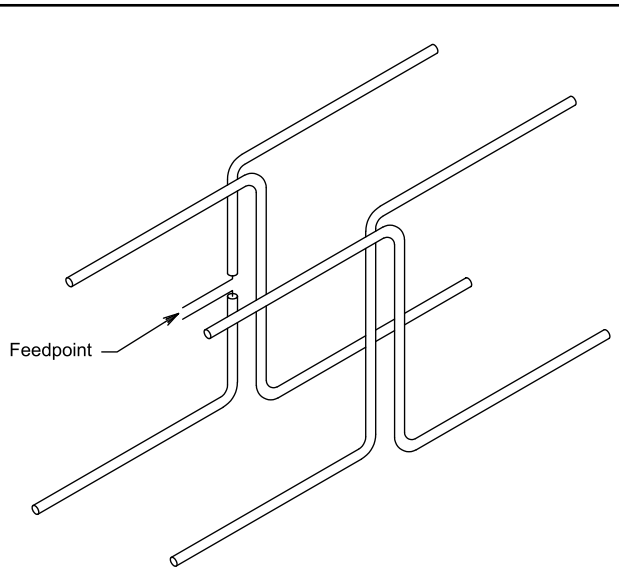

Fig 7—Prototype two-element Boxkite for 2 m/70 cm.

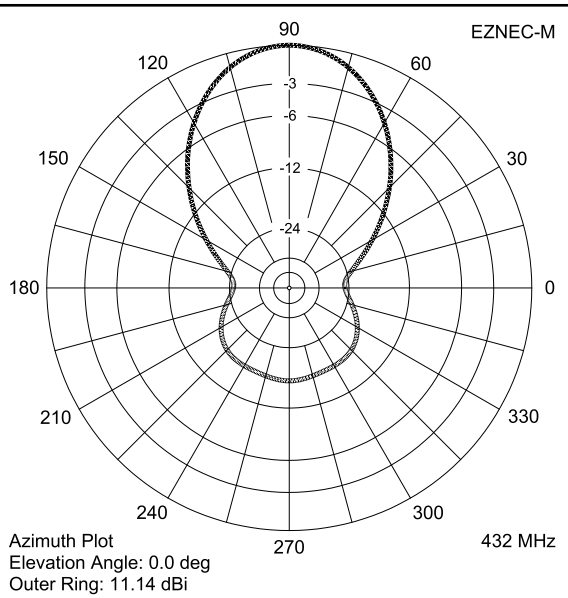

Fig 8—E-plane pattern for two-element prototype Boxkite at 432 MHz.

higher than the operating frequency, because the effects of coupling reduce the coupled resonant frequency somewhat. This effect allows the Boxkite element to resonate precisely at the fundamental and third harmonic. It is remarkable that the element-diameter effect allows this to happen and that the coupling coefficient is correct for spacing of the parallel sections that allows the correct impedance transformation ratio at *F3*.

I found that it is not only possible to adjust the element dimensions for operation on two harmonically related frequencies (for example 2 m and 70 cm), but also to equalize the feedpoint resistance at each frequency. The prototype Boxkite driven element dimensions for 2 m/70 cm are shown in Fig 6. It is fabricated from $^3/_{16}$-inch-diameter aluminum rod. Its feedpoint resistance at both 144 MHz and 432 MHz is 125 Ω, and it has 2:1 SWR bandwidths of 12.5 MHz and 55 MHz, respectively, which makes it very useful for use as the driven element of a Yagi-like beam. Notice that the close parallel wires are not arranged as in the "lazy H," but are spaced as shown

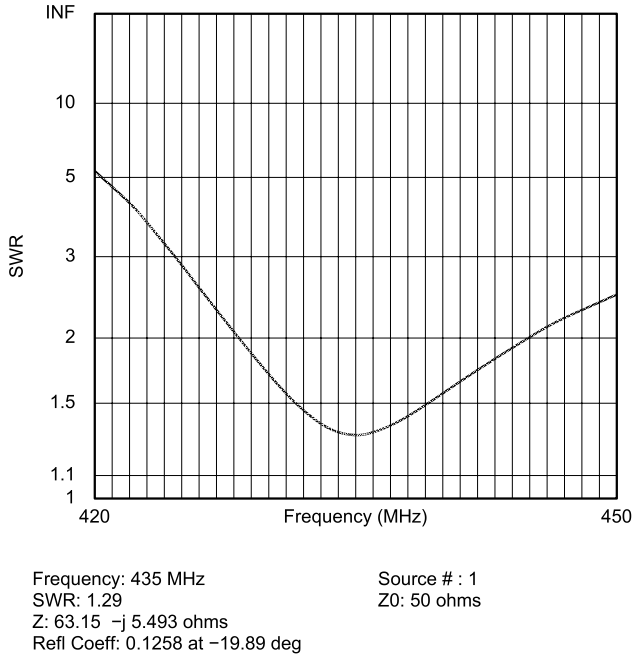

Fig 9—Two-element prototype Boxkite SWR on 70 cm.

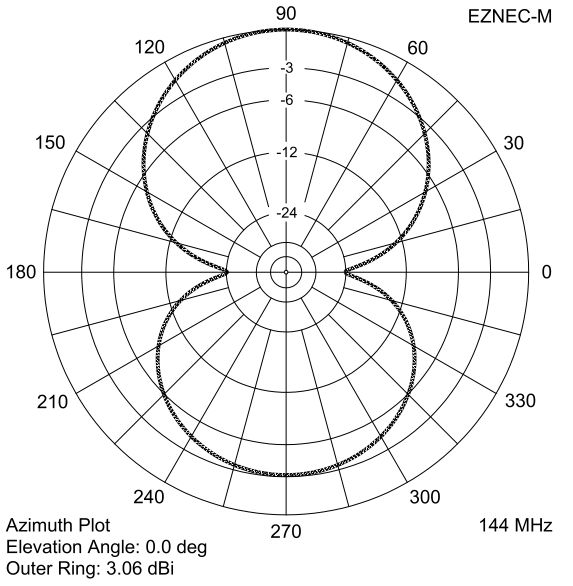

Fig 10—E-plane pattern for two-element prototype Boxkite at 144 MHz.

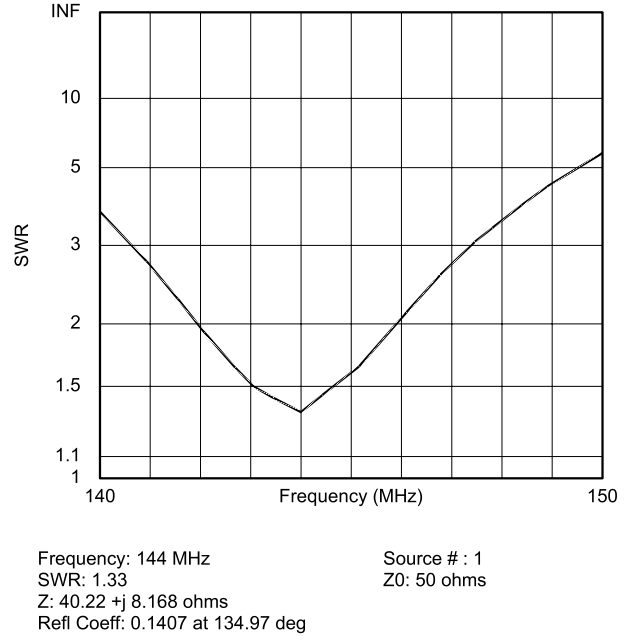

Fig 11—Two-element prototype Boxkite SWR on 2 meters.

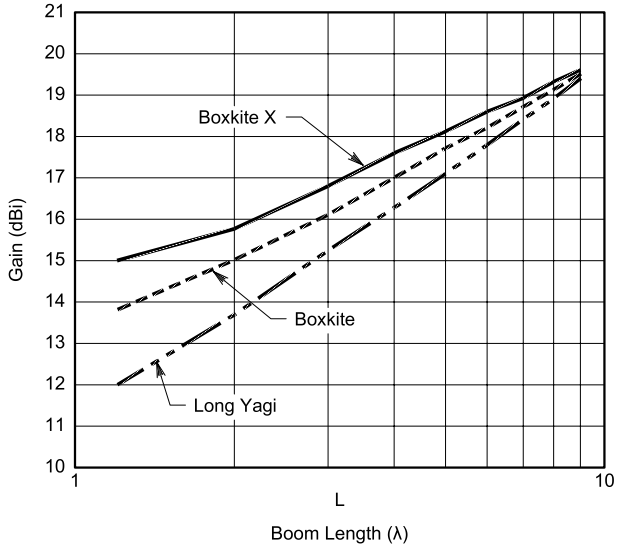

Fig 12—Yagi and Boxkite gain versus boom length.

in Fig 6, along the axis of the boom. This arrangement avoids the awkward cross over needed to maintain correct phases. One might worry about unequal coupling into the two halves of the element because of the offset between them along the Y axis. This does indeed occur but does not appear to affect the behavior of the antenna in any significant way, except as noted later.

Adding Parasitic Elements

It just so happens that the parasitic elements in a Boxkite beam can be of exactly the same form as the driven element. At *F1*, the element behaves as a short, end-loaded dipole. At *F3*, the currents in the four dipoles that make up the driven element induce currents in the four dipoles in the parasitic elements. The transmission-line sections of the parasitic elements behave as pairs of back-to-back λ/4 lines that present relatively high impedances to the ends of the four dipoles. One simplified way to look at this is that the λ/4 sections act as insulators at the third harmonic, so the four dipoles are isolated from ground and from each other. The spacing and lengths of the elements at *F3* roughly follow those of the excellent Yagis designed by K1FO, DL6WU and others. That is, there is a log taper of the element lengths and of the element spacings.[1, 2] This provides excellent gain, minimal side lobes and very good SWR characteristics. As it happens, the simulations show that these characteristics are maintained, albeit to a lesser extent, at *F1*. I was very surprised to find the feedpoint resistance at *F1* is close to 50 Ω, since the spacing of the parasitic elements is a very small fraction of a wavelength. For full- sized elements, this would mean a very low feedpoint resistance.

I have done some preliminary modeling work to compute the mutual impedance between two identical Boxkite elements as a function of the spacing between them. So far, I have no results to show, but I've noticed that the behavior of coupled Boxkite elements is notably different—and more complex—than that of coupled dipole elements, as might have been predicted. Although it is not easy to adjust a beam such as this for optimum performance in terms of gain, side-lobe level and SWR bandwidth on two bands, it is possible, as the following results will show.

During development, I was concerned that the staggered elements would cause asymmetric patterns and reduce the gain at *F3*. To resolve this, I modeled four Yagis stacked in the same way that the four sets of horizontal elements of the Boxkite are stacked. The models showed that staggering the elements does have an effect on the gain and pattern, but it is negligible. Two conventional Yagis offset along the boom axis do produce an asymmetric pattern; but here, the top pair is asymmetric in one direction and the lower pair in the opposite direction, so the resultant pattern is symmetrical. The models also showed, as expected, that increasing the horizontal stacking distance would increase the gain substantially, but this is difficult to do while maintaining enough coupling for operation at *F1*. See some remarks later on this issue.

For the prototypes, I insulated all the elements from the boom to avoid intermittent contact and boom screening problems. In theory, the centers of each of the subelements that comprise the parasitic elements can be connected together, but there is no advantage in doing this.

Prototype 2 m/70 cm Beams

I started by optimizing a two-element beam. By elements, I mean Boxkite elements, where each element has four dipoles operating at *F3*. The antenna is illustrated in Fig 7. Pattern and SWR data are shown in Figs 8 and 9 for 70 cm, and Figs 10 and 11 for 2 m. Notice that, unlike a conventional Yagi, where all elements are in the E plane, the Boxkite has elements lying in the H plane, so there are both vertical and horizontal components in the pattern because of a small amount of radiation from the transmission-line sections. To avoid confusion, the pattern plots show the total field only. This antenna has a gain of over 11 dBi at 432 MHz: The antenna behaves as a square array of four two-element Yagis stacked vertically and horizontally by 1/2λ. Although a spacing of 1/2λ is far from optimum from a gain standpoint, it does produce a very clean pattern with weak side lobes, as can be seen from Fig 8. On 2 m, the antenna is two reduced-length dipoles with very close spacing, so the gain of a little more than

[1]Notes appear on page 45.

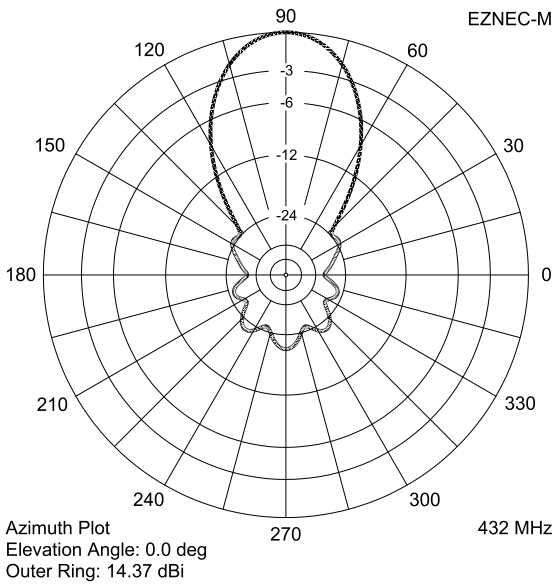

Fig 13—E-plane pattern for nine-element 1.65 λ Boxkite at 432 MHz.

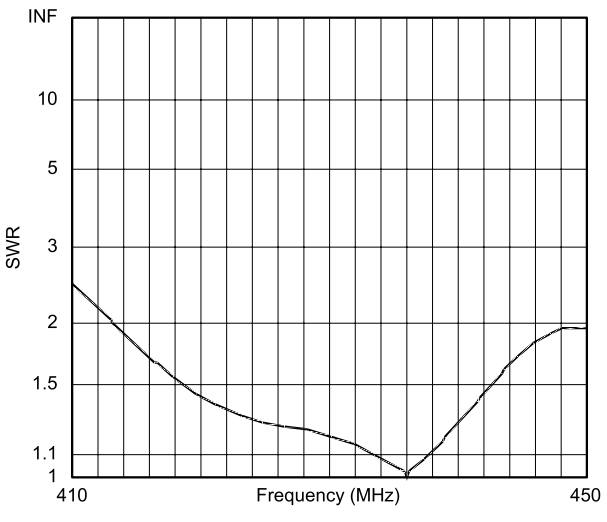

Fig 14—SWR for nine-element 1.65 λ Boxkite on 70 cm.

a dipole is expected. As can be seen from Figs 9 and 11, the SWR plots look reasonable on both bands. With Boxkites having longer booms, the SWR can be flattened substantially by tapering the directors, as is common with high-performance long-boom Yagis.

To build longer beams, elements are added in exactly the same way one would extend a Yagi, with dipoles replaced with Boxkite elements. In developing these Boxkites, I used relatively wide element spacing to provide wide SWR and gain bandwidth on 70 cm. This reduces the gain a little for a given boom length, but provides very broadband operation. Increasing the element spacing produces higher feedpoint impedances, so all the long Boxkites are designed for a feedpoint impedance of 112 Ω. (This does not apply to the two-element prototype, which has a 50-Ω feedpoint impedance.) This choice was made so that a simple balun using 75-Ω cable could be used as described later under "Baluns." I have modeled Boxkite Yagis for 2 m/70 cm for 2 through 29 elements and have measured the performance (SWR and pattern) of prototypes of most of them up to 14 elements (3.4 λ boom).

Theory says that if the stacking distance stays constant as the boom length increases, the antenna gain (as a function of boom length) will be asymptotic to that of a single Yagi. This appears to be the case; but for practical boom lengths, there still seems to be a clear gain advantage on 70 cm for the Boxkite. Fig 12 shows that the Boxkite maintains a constant length advantage of about 1.0 λ over a Yagi of the same gain. This is almost independent of the boom length. (The

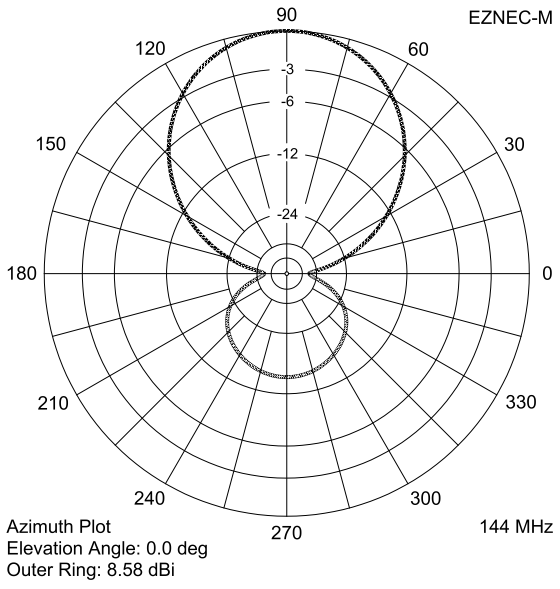

Fig 15—E-plane pattern for nine-element 1.65 λ Boxkite at 144 MHz.

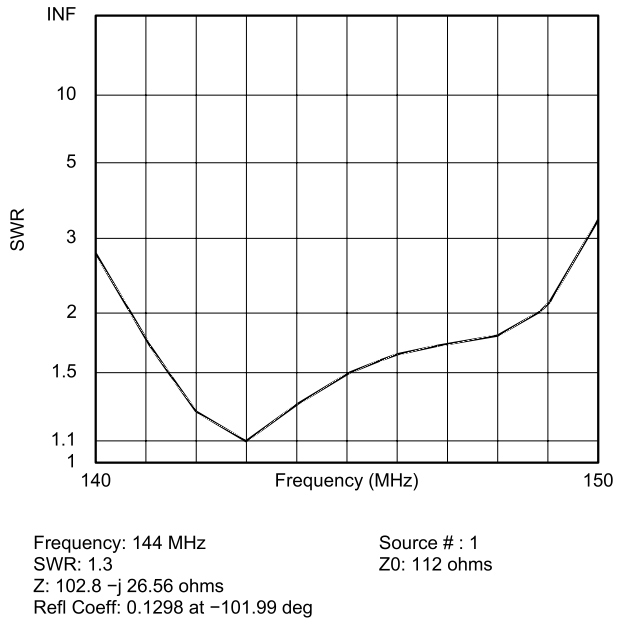

Fig 16—SWR for nine-element 1.65 λ Boxkite on 2 m.

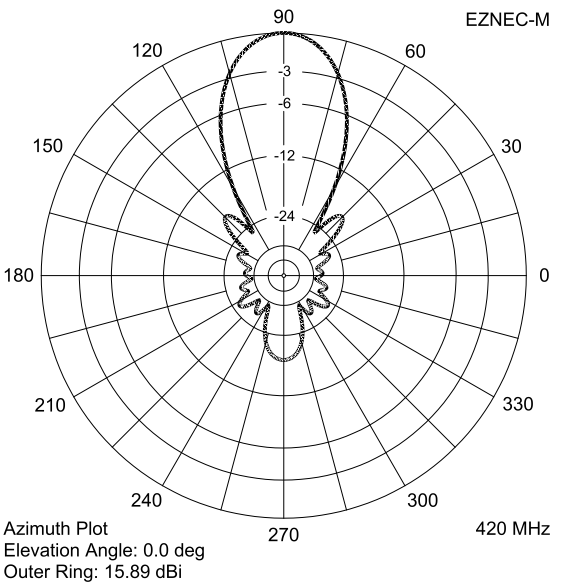

Fig 17—E-plane pattern of 14-element 3.4 λ Boxkite at 420 MHz.

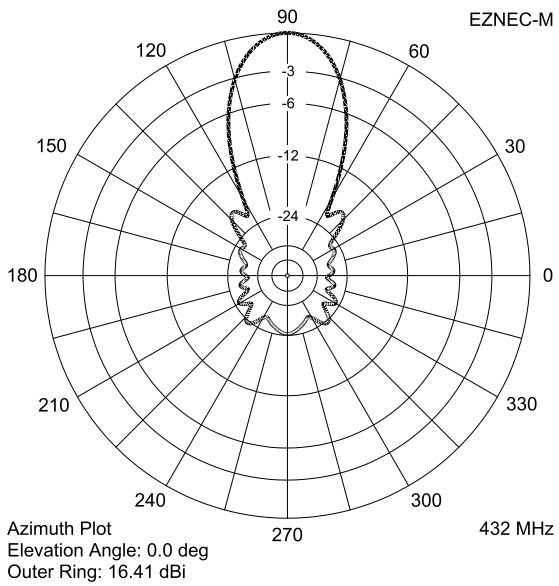

Fig 18—E-plane pattern of 14-element 3.4 λ Boxkite at 432 MHz.

Boxkite X plotted in Fig 12 is discussed later.)[3] Thus, the Boxkite gain is given approximately by:

$$G \approx 10\log[10(L_\lambda + 1)]\ \text{dBi} \qquad \text{(Eq 1)}$$

For a contemporary, high-performance long Yagi, gain is:

$$G \approx 10\log[10L_\lambda]\ \text{dBi} \qquad \text{(Eq 2)}$$

On 2 m, as expected, the gain for a given boom length is less than that of a Yagi of similar length. Plots of the pattern and SWR for the nine-element Boxkite are shown in Figs 13-16. Although not shown, the pattern has low sensitivity to frequency changes, which is important because it gives an idea of the design's dimensional tolerance. One other concern is tolerance to wet weather, especially because transmission-line sections are important parts of the antenna. The approximately 1-inch spacing of the transmission-line sections is big enough so that serious detuning does not occur. All VHF/UHF Yagis detune to some extent when wet, but I have found this a minor problem with Boxkites.

Notice that all my long Boxkites have double reflectors. At first, this may seem a little odd, but the addition of the second reflector makes it much easier to optimize the SWR without affecting the F/B ratio.

A 14-element Boxkite is of considerable interest because it gives excellent performance on both 2 m and 70 cm with a very practical eight-foot boom length. Figs 17-22 show pattern and

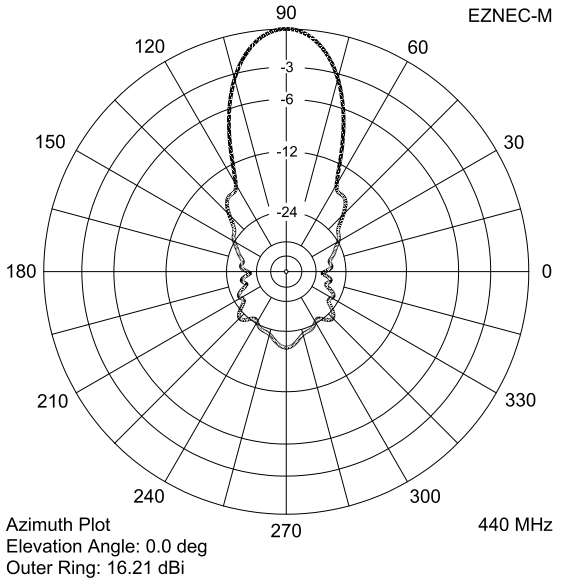

Fig 19—E-plane pattern of 14-element 3.4 λ Boxkite at 440 MHz.

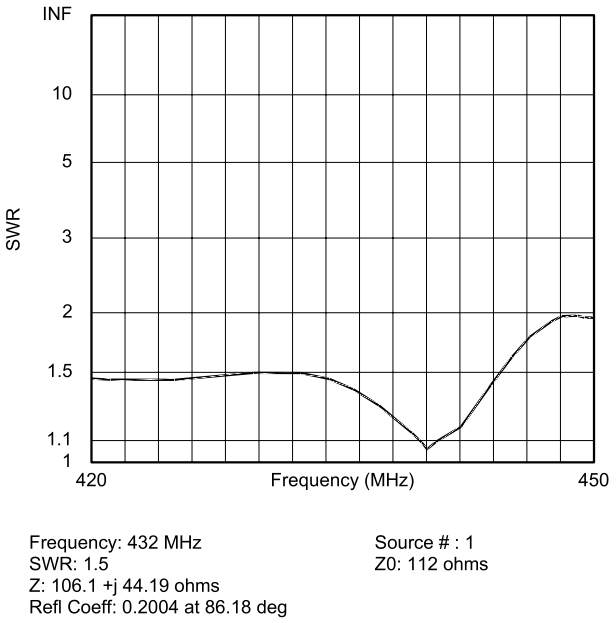

Fig 20—SWR plot for 14-element 3.4 λ Boxkite on 70 cm.

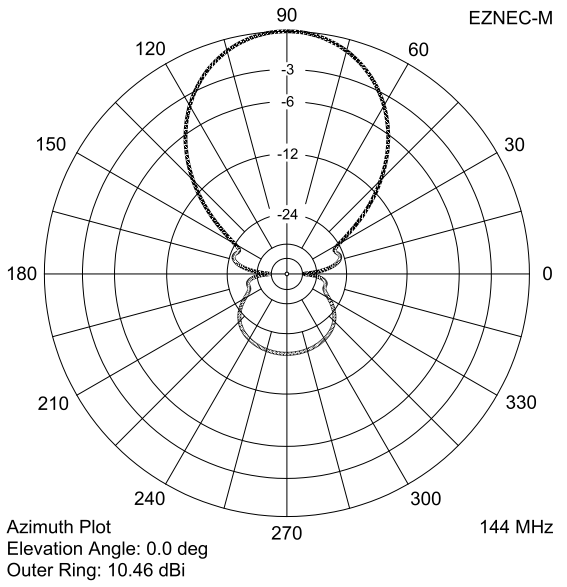

Fig 21—E-plane pattern of 14-element 3.4 λ Boxkite at 144 MHz.

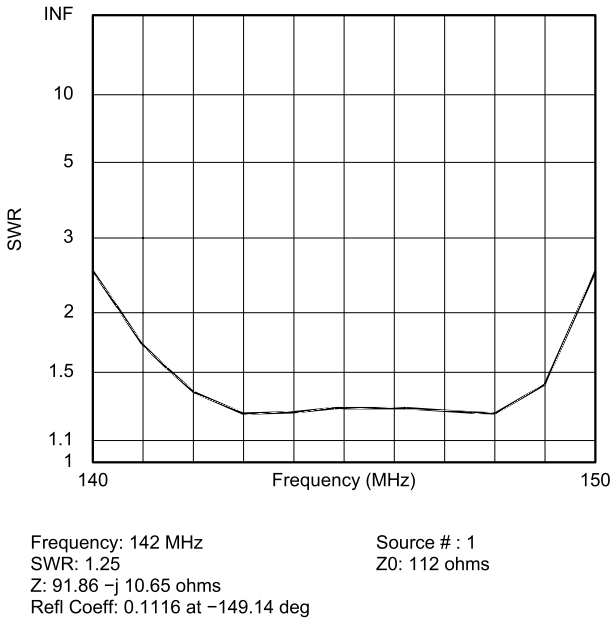

Fig 22—SWR plot for 14-element 3.4 λ Boxkite on 2 m.

SWR data. Figs 17, 18 and 19 show the E-plane patterns at 420, 432 and 440 MHz, respectively. The gain bandwidth on 70 cm at the –1 dB level is 30 MHz, or 7% of the center frequency. The 70 cm SWR plot in Fig 20 shows a 2:1 SWR bandwidth in excess of 30 MHz. Fig 21 shows the E-plane pattern at 144 MHz. Gain bandwidth on 2 m is 11 MHz, or 7.5% of the center frequency at the –1 dB level.

One might argue that a Boxkite VHF/UHF beam having polarization that is different at the two operating frequencies is of little practical value, because of cross-polarization effects in contacts with horizontally polarized antennas conventionally used for weak-signal work. However, the fact is that the Boxkite provides greater gain on a shorter boom than a conventional Yagi on the third harmonic, *and the performance on the fundamental is a bonus!*

Dimensions for the long Boxkites for 2 m/70 cm are shown in Table 1. The key to the dimensions of each subelement is shown in Fig 23. I will give some construction tips later in this article. Notice that these data are universal: The element dimensions and spacings are independent of the final boom length. Just decide what gain or boom length you want and build the antenna using the dimensions shown.

I have also modeled a nine-element Boxkite for 6 m and 2 m. This antenna has a gain of 8.6 dBi on 6 m and

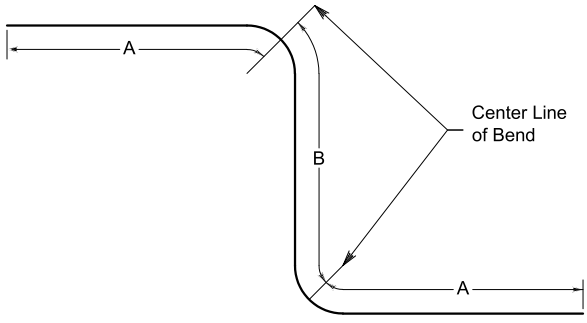

Fig 23—Key to subelement dimensions given in Table 1.

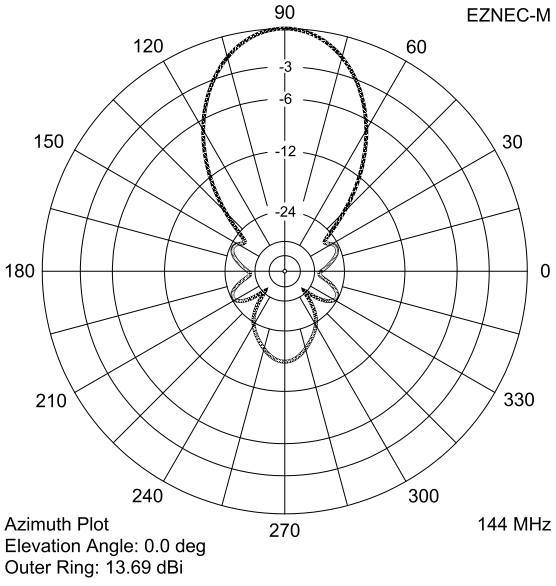

Fig 24—Nine-element 6 m/2 m Boxkite E-plane pattern at 144 MHz.

Table 1

Dimensions for 9- through 19-element Boxkites for 2 m/70 cm.

											Gain		Boom
Element	*Pos*[n] *(mm)*	*A (mm)*	*B (mm)*	*B/2 (mm)*	*S (mm)*	*Pos*[n] *(inches)*	*A (inches)*	*B (inches)*	*B/2 (inches)*	*S (inches)*	*70 cm (dBi)*	*2 m (dBi)*	*Length (ft)*
Ref 1	0	320	366	183	25	0	12.6	14.4	7.2	1.0			
Ref 2	140	345	366	183	25	5.51	13.6	14.4	7.2	1.0			
Driven	247	306	374	187	20	9.72	12.05	14.7	7.35	.80			
Dir 1	300	290	366	183	25	11.81	11.4	14.4	7.2	1.0			
Dir 2	410	270	366	183	25	16.14	10.65	14.4	7.2	1.0			
Dir 3	550	255	366	183	25	21.65	10.05	14.4	7.2	1.0			
Dir 4	720	250	366	183	25	28.35	9.85	14.4	7.2	1.0			
Dir 5	910	245	366	183	25	35.83	9.65	14.4	7.2	1.0			
Dir 6	1120	243	366	183	25	44.1	9.55	14.4	7.2	1.0	14.3	8.5	3’10”
Dir 7	1340	240	366	183	25	52.75	9.45	14.4	7.2	1.0	14.8	8.9	4’7”
Dir 8	1570	237	366	183	25	61.8	9.33	14.4	7.2	1.0	15.3	9.3	5’3”
Dir 9	1810	234	366	183	25	71.26	9.21	14.4	7.2	1.0	15.7	9.8	6’
Dir 10	2060	231	366	183	25	81.1	9.1	14.4	7.2	1.0	16.1	10.2	6’10”
Dir 11	2320	228	366	183	25	91.34	8.98	14.4	7.2	1.0	16.4	10.5	7’9”
Dir 12	2590	226	366	183	25	101.97	8.90	14.4	7.2	1.0	16.7	10.8	8’8”
Dir 13	2860	223	366	183	25	112.6	8.78	14.4	7.2	1.0	17.0	11.1	9’7”
Dir 14	3130	221	366	183	25	123.2	8.70	14.4	7.2	1.0	17.4	11.4	10’6”
Dir 15	3400	219	366	183	25	133.9	8.62	14.4	7.2	1.0	17.6	11.6	11’3”
Dir 16	3670	217	366	183	25	144.5	8.54	14.4	7.2	1.0	17.8	11.8	12’2”

13.7 dBi on 2 m—all on an 11-foot boom (see Figs 24-27). A conventional long Yagi would require an 18-foot boom to achieve the same gain on 2 m. I have not fully established the synthesis procedure for not-quite-harmonically-related beams, but clearly this looks promising.

Does it Work?[4]

SWR measurements of the prototype antennas agree excellently with the models. These measurements were made with an AEA SWR 121. Pattern measurements were made on my beach antenna range by (and sometimes in!) the beautiful Matanzas Inlet on the coast of Northeast Florida near St Augustine. For these measurements, I used either my trusty FT-847 or my AEA SWR 121 as the source, feeding a small Boxkite for 2 m/70 cm. The receiver was a Boonton 42BD Microwattmeter. The range was set up in accordance with guidelines given by Dick Turrin, W2IMU.[5] The measured patterns of the prototype 2, 9 and 14-element Boxkites on 2 m and 70 cm bear a very close resemblance to the simulation results, as can be seen from Figs 28-33.

The only plot that shows significant deviation from the simulation is the H-plane plot of the 14-element Boxkite on 144 MHz. I found this pattern particularly difficult to measure simply because I am a close-to-one-wavelength-long vertical element near the antenna under test! I had no such

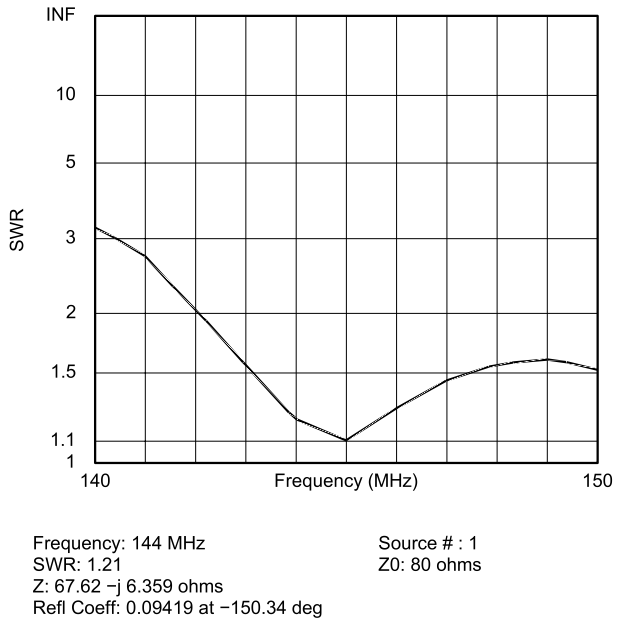

Fig 25—Nine-element 6 m/2 m Boxkite SWR on 2 m.

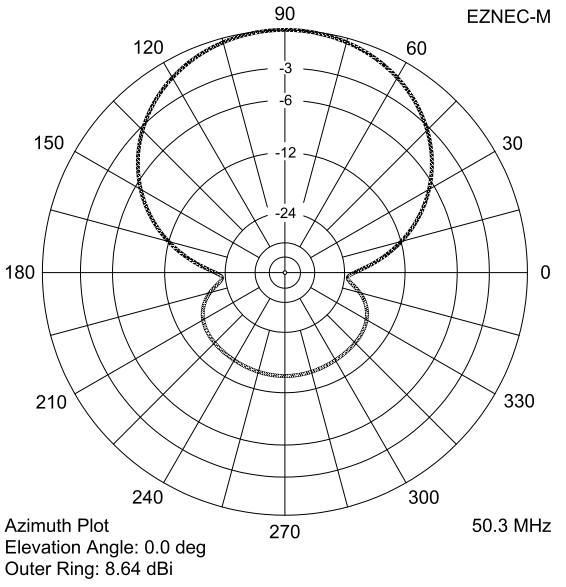

Fig 26—Nine-element 6 m/2 m Boxkite H-plane pattern at 50.3 MHz.

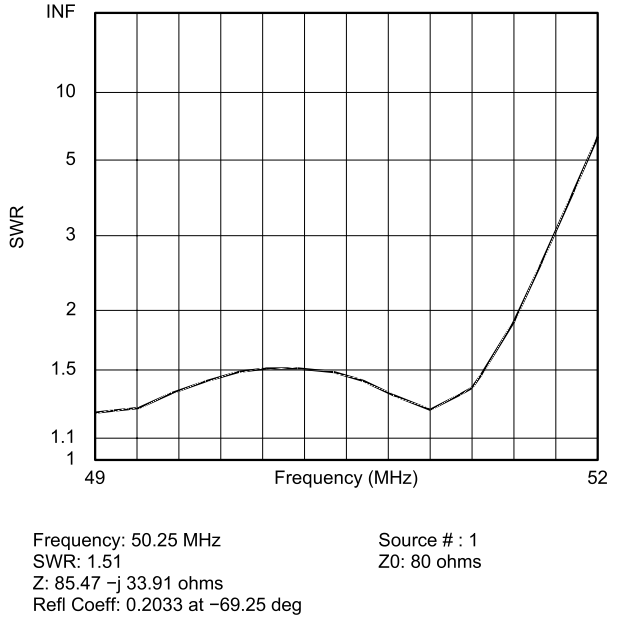

Fig 27—Nine-element 6 m/2 m Boxkite SWR on 6 m.

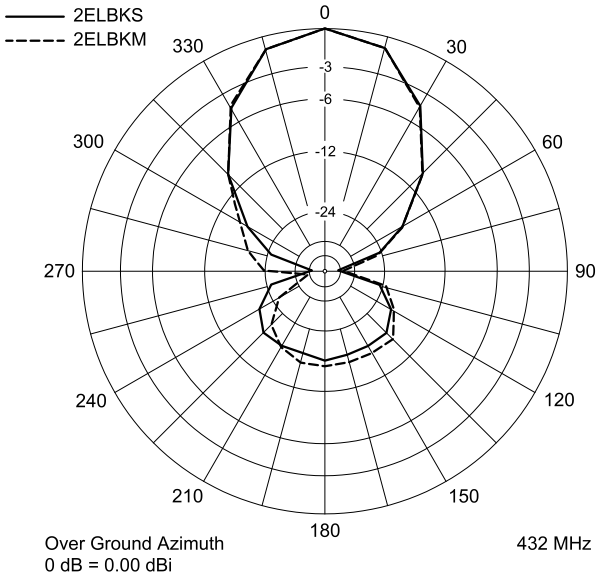

Fig 28—Simulated and measured E-plane pattern for two-element prototype Boxkite at 432 MHz.

problems with the E plane pattern on 144 MHz or either E or H plane patterns on 432 MHz.

The antennas were fed with a simple balun described later. Figs 34 and 35 show the simulated and modeled SWR plots for the 14-element Boxkite on 2 m and 70 cm, respectively. Notice the quite remarkable 2-m SWR plots!

Odd and Ends

Modeling

During the development period, I have tried to be extremely careful to check that the models produce very accurate results. I use the excellent *EZNEC pro* 3.0 software available from Roy Lewallen, W7EL. My biggest concern was that the close-spaced wires forming the transmission-line sections were being modeled accurately, so I ran some tests based on balanced twin-wire transmission-line theory. My conclusion is that, provided that an appropriate number of segments are used, the accuracy of the models for the wire diameters and spacings used in the antennas is excellent. This has been born out by the quite remarkable agreement between simulations and measurements on a wide variety of antennas.

I should point out that the 2 m/70 cm Boxkites have radius bends, and that I carefully measured the effects of this on the pattern and SWR. My conclusion is that the pattern is virtually unaffected by the 1/4-inch radius of the bend, and SWR is controlled more by the total length of each subelement, rather than by how the

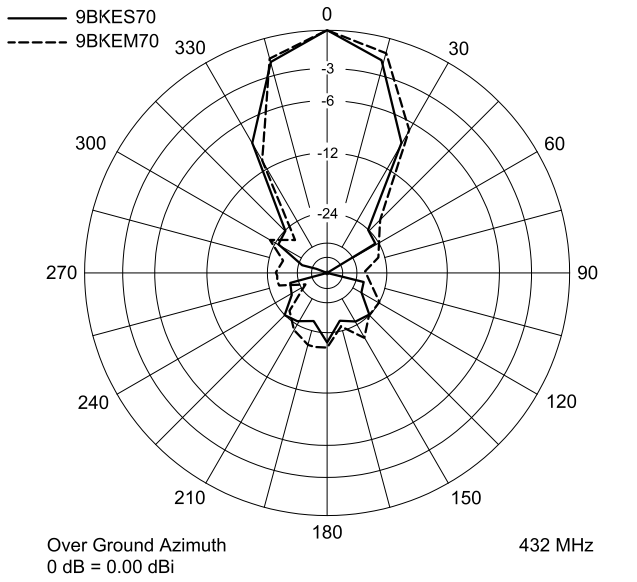

Fig 29—Simulated and measured E-plane pattern for nine-element prototype Boxkite at 432 MHz.

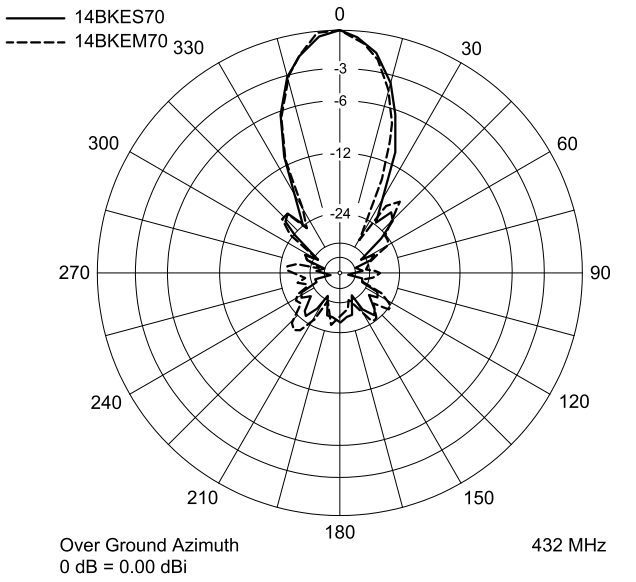

Fig 30—Simulated and measured E-plane pattern for 14-element 3.4 λ Boxkite at 432 MHz.

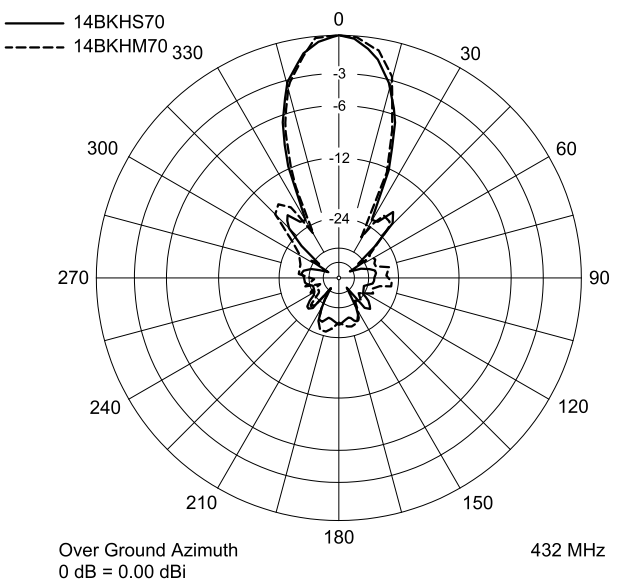

Fig 31—Simulated and measured H-plane pattern of 14-element 3.4 λ Boxkite at 432 MHz.

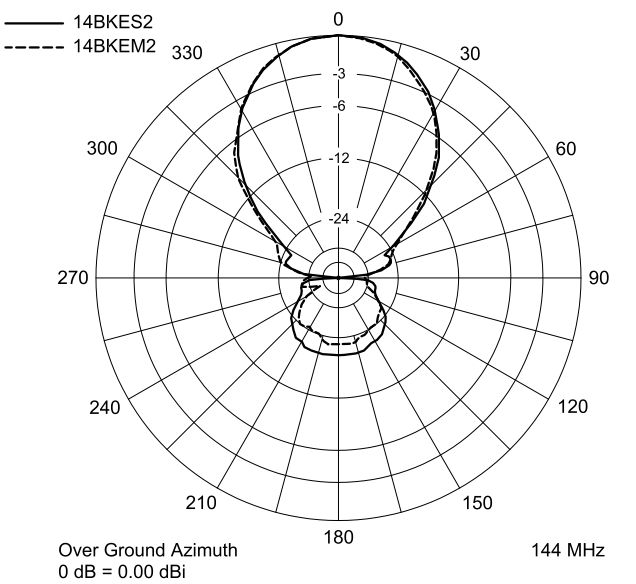

Fig 32—Simulated and measured E-plane pattern of 14-element 3.4 λ Boxkite at 144 MHz.

sector lengths are distributed. The center of a $^{3}/_{16}$-inch diameter aluminum rod bent around a $^{1}/_{4}$-inch radius stretches by a fraction of a millimeter: The inside of the bend contracts and the outside stretches. This means that the bend has very little effect on SWR. Hence, the prototype antennas were built by cutting the subelements exactly to the modeled length and measuring the horizontal section lengths from each subelement end to the center of the radius. This has proved a very simple and accurate way to make the subelements.

Construction Tips

Twin C dipoles can be made from any conventional antenna material, such as wire or tubing. Wire dipoles can be strung up between any convenient supports such as trees or poles. My prototypes were suspended from deck supports that are tall enough to accommodate them. Be sure that the wires in the parallel section cannot move relative to each other—otherwise, the tuning will vary.

Twin C beams can be made using any normal Yagi construction techniques, with the difference that the wings of the elements should be supported on insulators near the boom. For HF through 6 m, any reasonably sized boom will probably not cause boom-screening problems. The centers of all the nondriven subelements can be mounted without insulators directly on the boom, if desired. However, problems associated with boom screening and unreliable connections between aluminum elements and boom make this practice undesirable for antennas for 2 m and above.

The prototype Boxkites were built using readily available materials. The following is a description of how they were put together (omitting all the mistakes, of course!). The parasitic elements are mounted in polypropylene blocks cut from kitchen cutting boards available from any department store. The boom was a 1-inch square aluminum section available from most

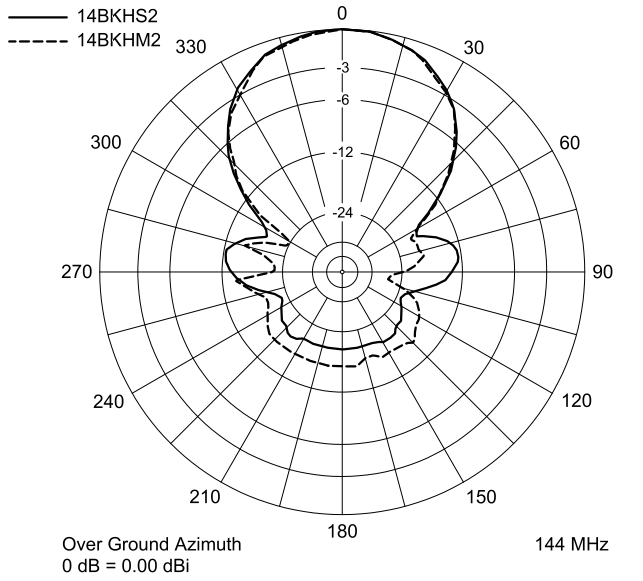

Fig 33—Simulated and measured H-plane pattern for 14-element Boxkite at 144 MHz.

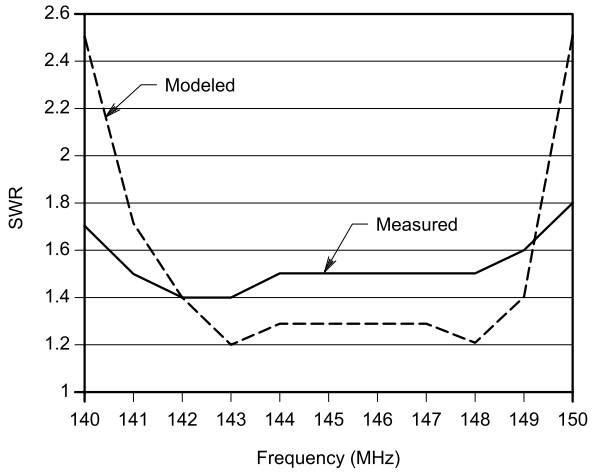

Fig 34—Simulated and measured SWR of 14-element 3.4 λ Boxkite on 2 m.

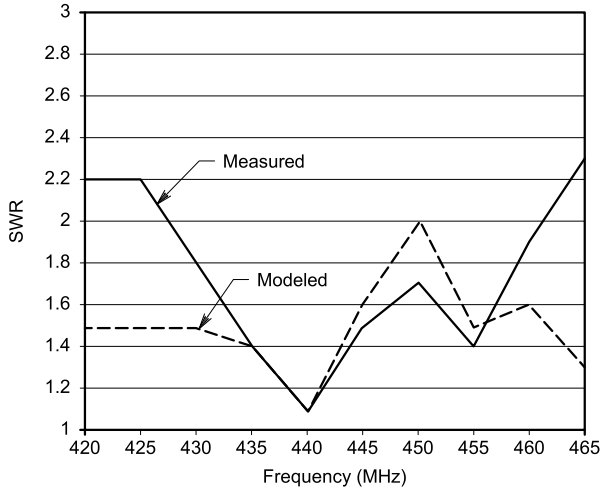

Fig 35—Simulated and measured SWR of 14-element 3.4 λ Boxkite on 70 cm.

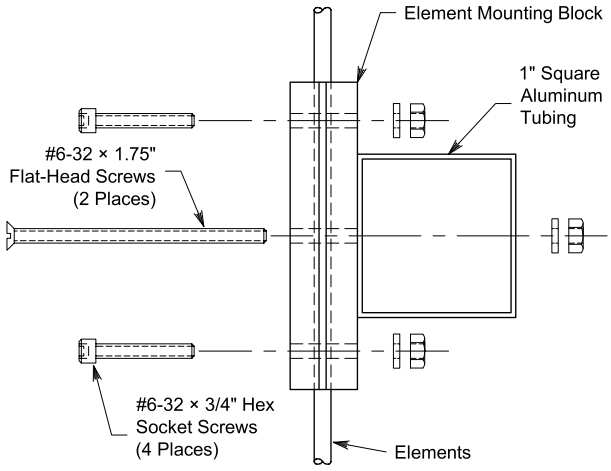

Fig 36—Method of mounting the parasitic elements.

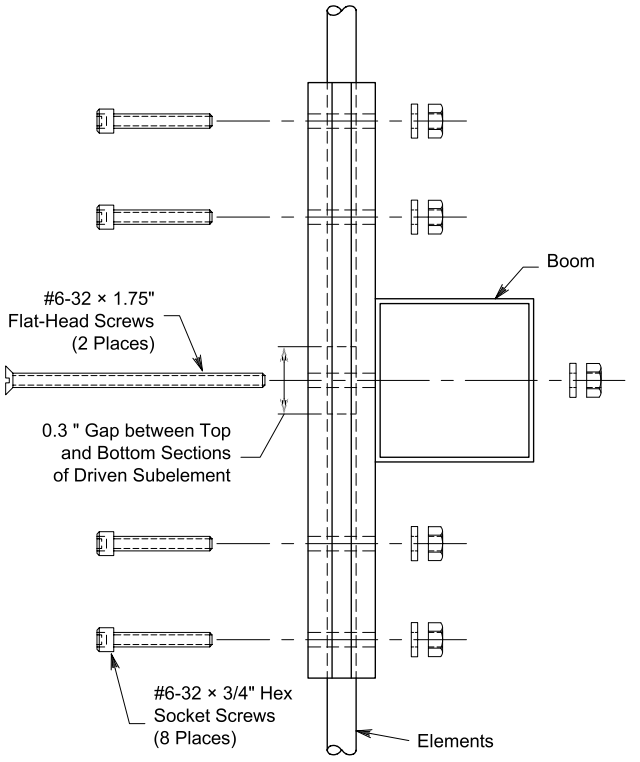

Fig 37—Method of mounting the driven element.

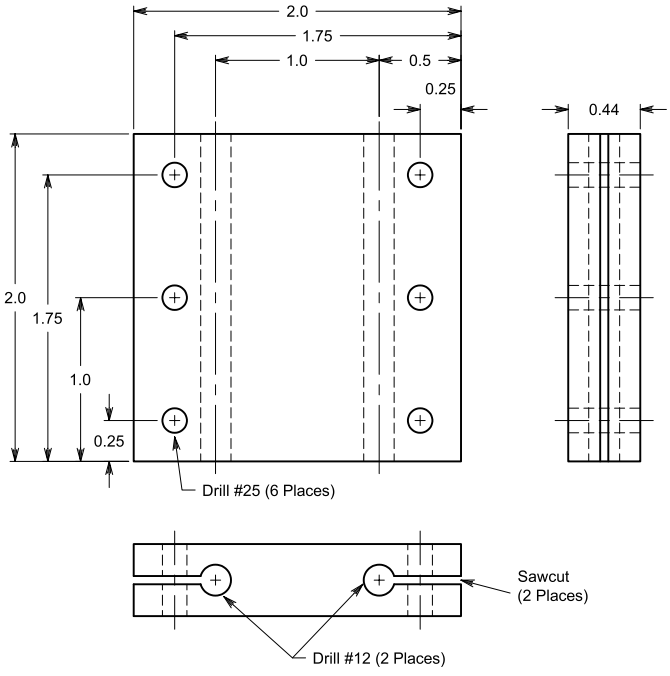

Fig 38—Parasitic-element mounting block.

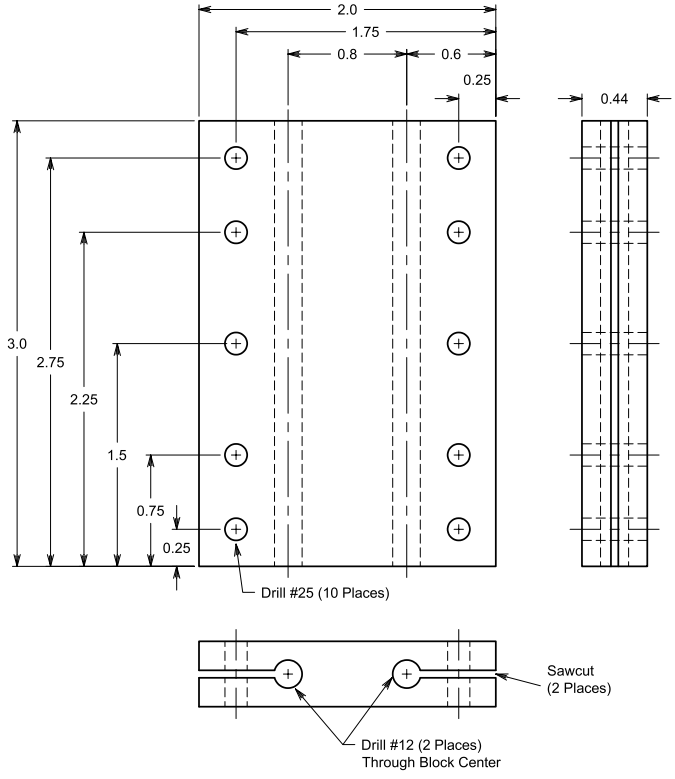

Fig 39—Driven-element mounting block.

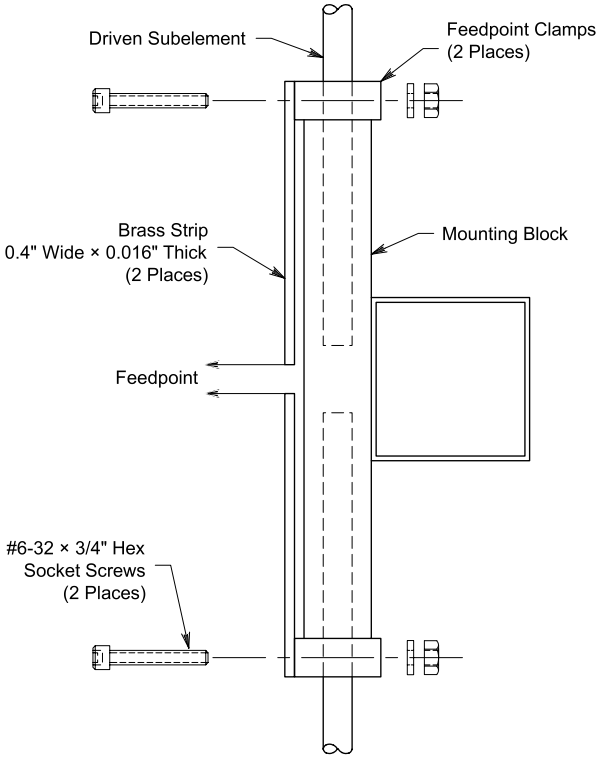

Fig 40—Feedpoint arrangement.

hardware stores. The element material is 3/16-inch aluminum rod. The bends in the elements can be formed accurately by hand-bending them around a 1/2-inch diameter mandrel (aluminum rod or tube, or even a wooden dowel, is just fine). The elements must be mounted so that they do not rotate, and this is achieved by clamping via a saw cut through the plastic blocks into the element-mounting holes. Screws through the plastic blocks then grab the elements tightly. This has worked fine for the prototypes, but they have not been exposed to the weather. If you are worried about the elements rotating, after assembling the elements to the blocks, run a suitable drill through both and install 1/16-inch tension pins.

The methods of mounting the parasitic and driven elements are shown in Figs 36 and 37, respectively. Fabrication details for the mounting blocks are shown in Figs 38 and 39. They may look a little complicated but they are easy to make. Cut out the blocks using a tenon saw: A regular hacksaw tends to produce non-square edges in this material. True up the edges with a file, and carefully mark all the holes. The vertical-element holes should be drilled using a drill press if possible to ensure that they are true. Notice that the center-to-center spacing of the driven subelements is different from that for the parasitic elements. Drill the clamping holes next, then make the saw cuts with a tenon saw. Clean up all the holes and remove any plastic burrs.

For the parasitic elements, mark out the element dimensions as shown in Table 1. Mark the positions of the block edges, equally spaced around the element center and the centers of the corner radii. Double check the total length and cut the subelement to length. Clean up the cut end with a file. Push the element through its mounting hole in the block, and locate the block roughly in the center of the element. Clamp the 1/2-inch mandrel tightly in a bench vise so that the axis of the mandrel is horizontal, and draw a short line parallel with the axis along

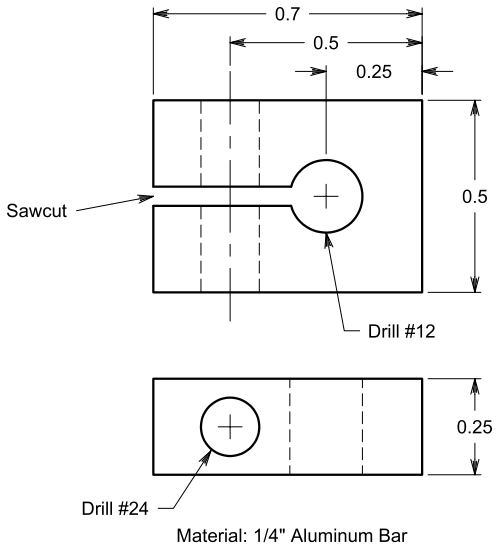

Fig 41—Feedpoint clamps.

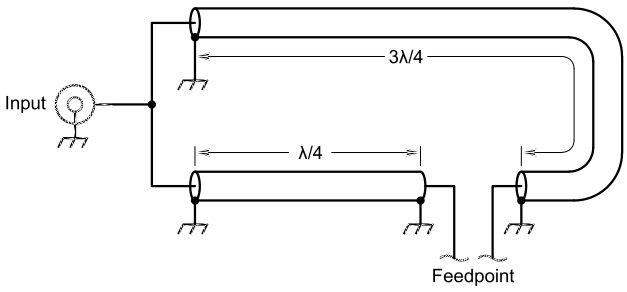

Fig 42—Dual-band balun for 2 m/70 cm Boxkites. Cut the phasing cables to the electrical length shown at 144 MHz. Use 75 Ω cable such as RG-59 or RG-6.

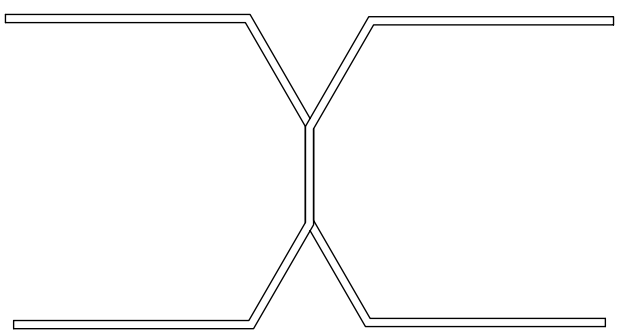

Fig 43—Boxkite X element. The two subelements are spaced along the boom by 20 mm.

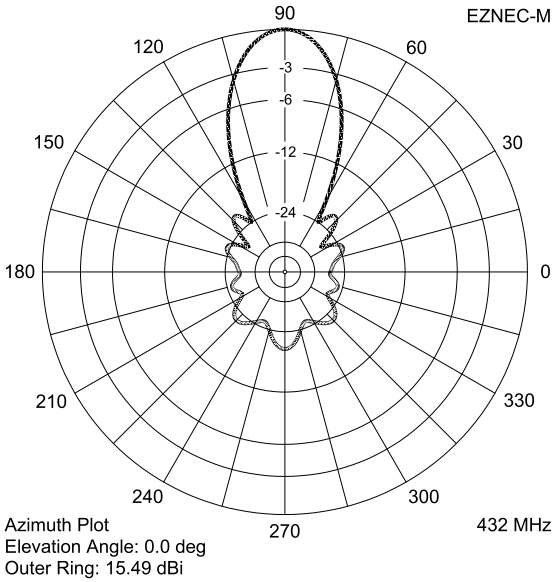

Fig 44—E-plane pattern for eight-element 1.5 λ Boxkite X at 432 MHz.

the top length of the mandrel. This provides a reference point for bending the elements. Hold the elements with your hands placed either side of the element radius center. Place the element on the mandrel so that the radius mark coincides with the reference mark on the mandrel. Check that the bend will be roughly perpendicular to the block face, and gently bend the element so that the radius mark stays in the center of the bend. Now do the same with the second bend, making sure that you bend it in the opposite direction from the first bend. Any slight error in bending can be corrected by slightly twisting the elements.

Push the second subelement rod through its mounting hole and repeat the bends. Make sure that the subelements face away from each other in the right way and that they will be square with the boom, then clamp them tightly with the #6-32 cap screws. This whole procedure sounds complicated, but it is very easy once you get the hang of it. The bends and

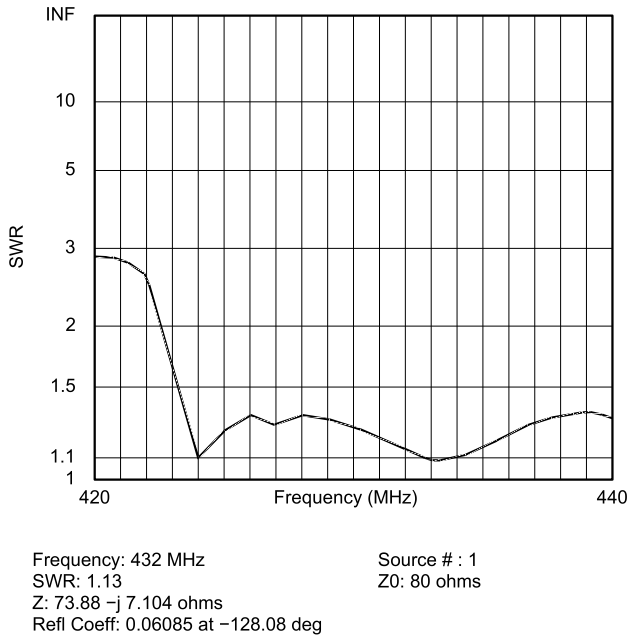

Fig 45—SWR plot for eight-element 1.5 λ Boxkite X.

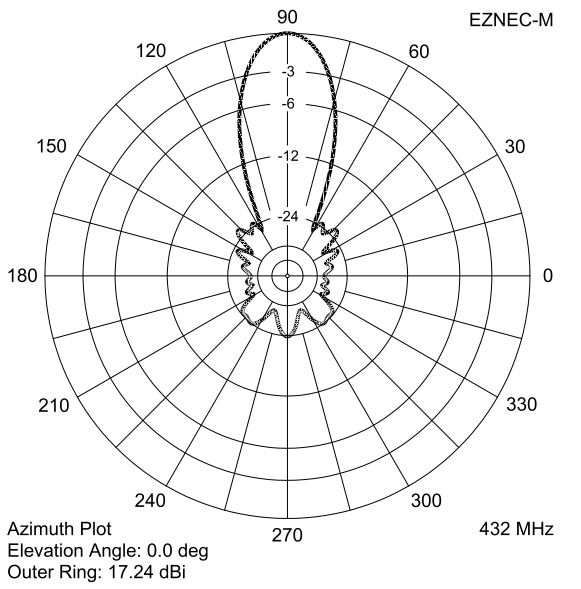

Fig 46—E-plane pattern for 13-element 3.45 λ Boxkite X.

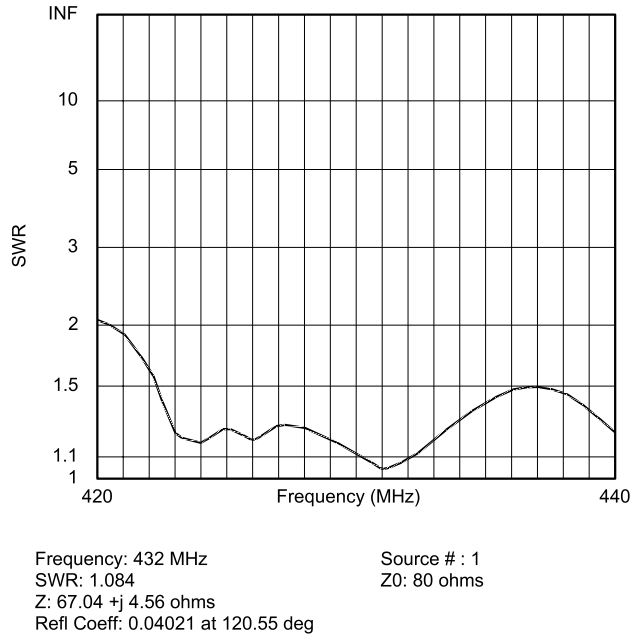

Fig 47—SWR plot of 13-element 3.45 λ Boxkite X.

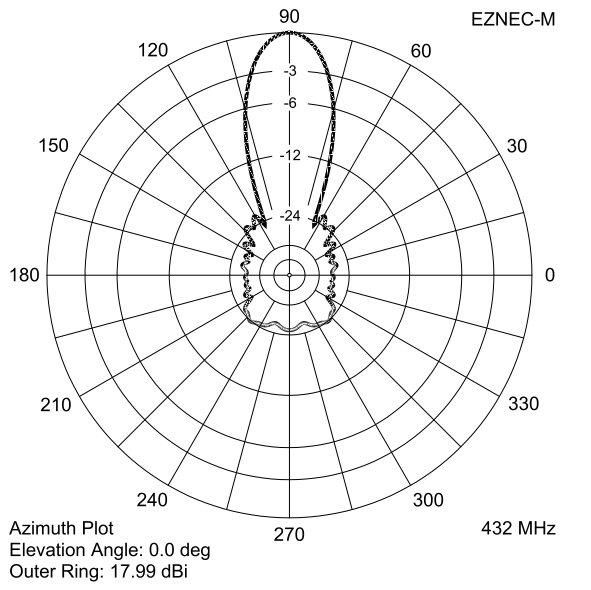

Fig 48—E-plane pattern for 17-element 4.8 λ Boxkite X.

lengths all seem to come out with sufficient accuracy.

The driven element is mounted in almost the same way, with the exception that the driven subelement is split in its center (see Fig 40). The two brass strips connect the feedpoint to the element via the element clamps (details are in Fig 41). The balun cables (see later) connect directly to the feedpoint, with their shields grounded to the boom. The lead lengths should be no more than a few millimeters. The method of mounting the driven element allows some adjustment of its length to minimize the 2 m SWR. Simply loosen the driven subelement clamp screws and move the subelement halves one way or the other to adjust for minimum SWR. This adjustment will have a minor effect on the 70-cm SWR.

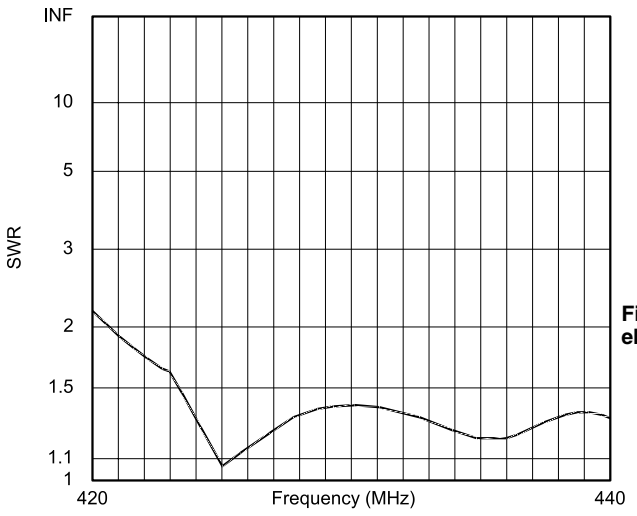

Fig 49—SWR plot of 17-element 4.8 λ Boxkite X.

Boxkites for Higher Frequencies?

Preliminary models show that scaling the 14-element 2 m/70 cm Boxkite for operation on 70 cm/23 cm works just fine. However, the devil is in the details at this frequency, so I won't believe that it is practical until I make one and verify that it works!

Baluns

The driven element is a balanced load and therefore it is preferable that it be driven via a balun. For the HF Twin C antennas, any proven 1:1 current balun will do a good job. Try to lead the feed cable away from the feed point at right angles to the plane of the antenna to reduce the current coupled into the shield of the cable. Such currents can also be reduced substantially by looping the coax through suitable ferrite toroids, which form choke baluns and reduce coupling from the antenna to the coax outer shield.

For the VHF/UHF antennas detailed here, the balun is a simple dual-band system that uses a pair of 75-Ω phasing lines cut to provide equal-amplitude, opposite-phase drive to the driven-element terminals. The principle is illustrated in Fig 42. The lines are λ/4 and $^3/_4$λ long at the fundamental. The phase difference between the outputs is 180°, and the impedance looking into the input is 50 Ω. A little thought will show that this is also true at the third harmonic. The bandwidth is adequate for both bands.

This type of balun gives a subtle theoretical advantage over the λ/2 4:1 balun that is conventionally used with a T feed for high-performance VHF/UHF Yagis. With the λ/2 balun, the SWR is sensitive to load imbalance, but with the balun used here the SWR is completely independent of load imbalance. I used a good quality RG-6 for the prototype 2 m/70 cm beams, although the loss on 70 cm is too high if you are looking for the absolute maximum gain. If you only need to use the beam on 70 cm, then the phasing lines may be reduced to one third of the lengths shown and the balun loss will be reduced. In the prototypes, the balun cables were dressed along the boom and taped to it. Be careful not to bend foam-dielectric cable too sharply.

Boom Effects

As with most VHF/UHF Yagis, a metallic boom affects the feedpoint impedance and, to a lesser extent, the pattern. For the 2 m/70 cm two-element beam, I found that the two bands are affected differently. With the elements mounted through the center of 0.4-inch-thick insulators on top of the 1-inch square boom, the resonant frequency on 2 m was shifted up by about 2%. (The distance from the centers of the elements to the boom is only 0.2 inch.) I finally tracked this down to a reduction of the coupling coefficient caused by boom screening, and as pointed out earlier this increases the resonant frequency. It does not materially affect the pattern or gain, so any correction for boom effect need be applied to the driven element only. On 70 cm, the combined screening effect and the extra capacitance from the feedpoint to the boom also increase the resonant frequency by a little less than 2%, but has a beneficial effect of flattening the SWR curve somewhat.

The boom effect appears to be a problem only for Boxkites using few elements, such as the two-element beam. This is because the SWR bandwidth is narrow and the boom effect primarily affects the SWR center frequency: Any changes can easily produce an unacceptably high SWR. The gain bandwidth is wide enough that pattern and gain changes caused by boom effect seem to be quite small. For the longer beams, where conventional broadband techniques adapted from Yagi design allow a much wider SWR bandwidth, the effect appears to be negligible, unless you are looking for the perfect 1:1 on your favorite frequency!

I must confess that the boom effect on my prototype two-element 2 m/70 cm beam caused me more aggravation than it should have. My prototype eight-element Boxkite for 2 m/70 cm has elements mounted through the boom and the effects are negligible.

Mounting to the Mast

When a Boxkite is oriented to produce horizontal polarization on the fundamental, there appears to be no problem using a conventional metallic mast and clamp. The mast is not close to, or in line with, the vertical elements, so there is very little interaction between mast and antenna.

When oriented for vertical polarization on the fundamental, a metallic mast is problematic. A solution is to use a short plastic or fiberglass mast. Don't forget that the feed cable, if dressed down the mast, will affect antenna operation unless decoupled every few inches with ferrite toroids to suppress braid currents.

Wind Load and Weight

To compare the weight of a Boxkite to that of conventional Yagis, I added the weights of K1FO Yagi designs for 70 cm and 2 m that would produce the same gain as a 14-element, 3.4-λ Boxkite on the two bands. My quick calculations of the relative weight of a Boxkite show that, for the same boom and element materials and sizes, the Boxkite weighs approximately 11% less than the two Yagis combined.

As for wind load, the advantage again lies with the Boxkite. I assumed the two Yagis were horizontally polarized, and that the Boxkite was horizontally polarized on 70 cm. According to my sums, again when using similar size and shapes for the boom and elements, a 14-element, 3.4 λ Boxkite has a wind load that is 88% of the Yagis'. This is mostly because the Boxkite has a significantly shorter total boom length, and the boom is a major contributor to the wind load.

Boxkite X

As a final note before I summarize, while I was developing the Boxkite, I recalled the "Multibeam" that was produced by J-Beam in the United Kingdom a few years back. It has some resemblance to the Boxkite, with the exception that the driven element and reflector appear to be skeleton slots. Each director consists of four separate directors insulated from each other. I have not seen any reports on the antenna performance, so I modeled an "X beam" for 70 cm based on a stretched out Boxkite element (see Fig 43). All elements have the same form. The total length of each subelement is about the same as for a Boxkite, but the **X** shape moves the dipole sections further apart in the horizontal plane, while shifting them slightly closer together vertically. I expected that the wider horizontal spacing would improve the gain over that of a Boxkite. It does this nicely, with a very good pattern, but the coupling between the subelements is too small to allow operation on 2 m. The pattern and SWR plots of 8, 13 and 17-element versions of this antenna, which I call the Boxkite X (for want of a better name) are shown in Figs 44-49. The eight-element antenna has a boom length of 3 feet 6 inches and the gain of a conventional Yagi that is over 7 feet long. Boxkite X performance versus length is shown in Fig 27. For all practical boom lengths, it maintains a length advantage over a conventional long-boom Yagi of about 1.8 λ, or about 4 feet on 70 cm and over 12 feet on 2 m. The gain of a Boxkite X is given approximately by:

$$G \approx 10\log\left[10(L_\lambda + 1.8)\right]\text{dBi} \qquad \text{(Eq 3)}$$

Gain bandwidth for all practical Boxkite X antennas for 70 cm is about 20 MHz, and the SWR bandwidth is over 20 MHz.

The feedpoint impedance of the Boxkite X series is about 80 Ω, and a simple **T** match and λ/2 balun combination is probably the easiest way to feed them. I have not yet built a Boxkite X prototype, so I won't give dimensions here. If there is sufficient interest, I will write a follow-up article on Boxkite X construction.

Summary

These articles have introduced a wide range of antennas that are based on a novel basic dipole element. The element has applications from the low HF bands up through UHF and even higher. Since I finished these articles, I have completed more development of Boxkites. I have built and tested an 18-element Boxkite for 23 cm/70 cm with excellent results. I have also learned how to provide identical polarization on the two bands and have modeled Boxkites using this method for operation on 2 m/6 m, 70 cm/2 m, 23 cm/70 cm and 9 cm/23 cm. I have also built and tested prototypes for 2 m / 6 m, 23 cm / 70 cm and 9 cm / 23 cm having the same polarization on both bands. The results of this further development will be reported in a follow-up article, I hope in the not-too-distant future.

Notes

[1]G. Hoch, DL6WU, "Yagi Antennas for UHF/SHF," *ARRL UHF/Microwave Experimenter's Manual*, ARRL, 1990.

[2]S. Powlishen, K1FO, "An Optimum Design for 432 MHz Yagis," ARRL UHF/Microwave Experimenters Manual, ARRL 1990.

[3]Using data from reference 5 as representative, and from Zack Lau, W1VT, "RF, A Small 70-cm Yagi," *QEX*, Jul/Aug 2001, pp 55-59.

[4]This is what my mother says a lot when rooting around in garage sales.

[5] R. Straw, N6BV Ed, *ARRL Antenna Book*, 19th edition, (Newington, Connecticut: ARRL, 2000). □□

Tapped-Capacitor Matching Design

A fresh look at a common matching technique with a downloadable spreadsheet.

By Randy Evans, KJ6PO

When designing RF circuits, it is often necessary to match one impedance to another over a limited bandwidth. A common circuit often used is the tapped capacitor matching circuit as shown in Fig 1, where a high source resistance is matched to a lower load resistance (or a low source resistance is matched to higher load resistance). Unfortunately, there are a number of different approaches published to calculate the circuit values needed. Just as unfortunately, most of them are incorrect. This article describes a technique that has been validated by both analysis and experiment. A simple *Excel* spreadsheet is also presented to ease the design of these circuits.[1] The experimental and analytical results are described in detail.

The genesis of this article occurred when I was trying to match the 800 Ω input/output impedance of a 10 MHz crystal filter to a 50 Ω circuit. I decided to use a tapped-capacitive matching circuit because of its simplicity (compared to tapped or multilink inductors). In researching the design of the circuit, I came across several articles that purported to solve the problem. Unfortunately, each gave a radically different answer, which was confusing to say the least. The best article, in my opinion, is one by Andrzej B. Przedpriski (see Reference 1).

However, I found that it has a critical error in the derivation of the inductor reactance. Unfortunately, I did not come across the article until after I had done my own derivations, but the approach taken in that article is very similar to the one in this article.

I then took each design approach and analyzed the results using a circuit-analysis program: *GENESYS* from Eagleware Corporation (**www.eagleware.com**). Even more confusing, none of them gave me acceptable results. I then wrote my own circuit-analysis programs using *Matlab* (**www.mathworks.com**) to try and understand the problem. In the end, I was able to synthesize a design approach that gives exact results that agree with *GENESYS*, *Matlab* and experimental results.

I will describe one common design approach for tapped capacitive matching circuits that can give very inaccurate results. This is described by:

$$R_{load} \quad R_{source}\left(\frac{C_s}{C2}\right)^2 \qquad \text{(Eq 1)}$$

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[1]Notes appear on page 52.

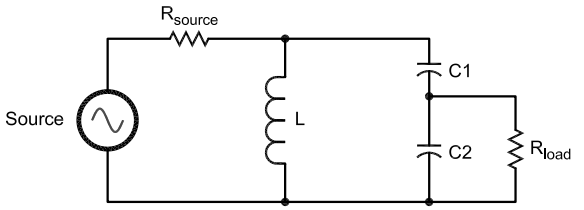


Fig 1—Tapped capacitor matching circuit.

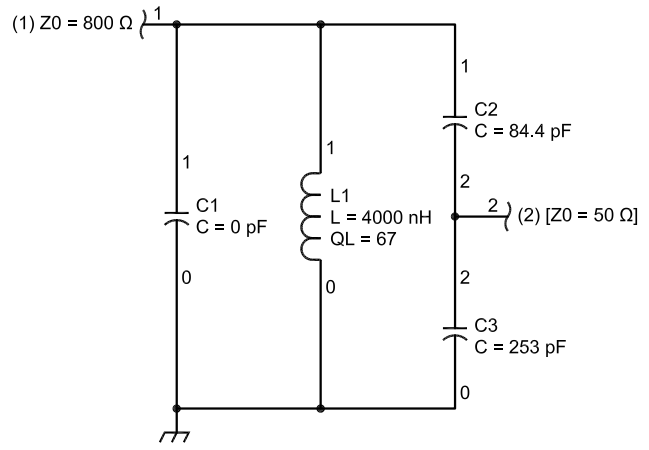


Fig 2—Schematic of circuit 1.

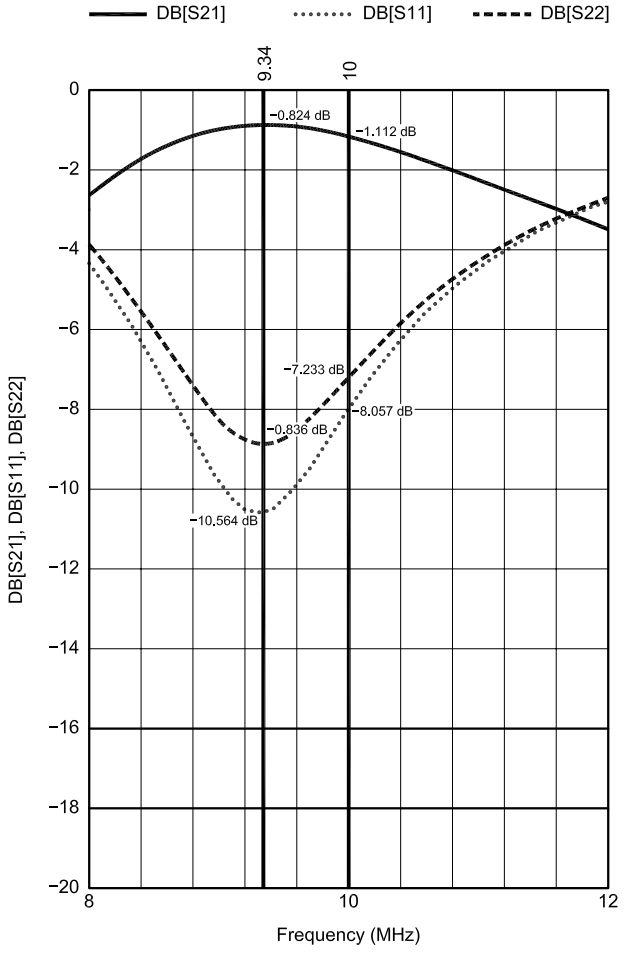


Fig 3—Circuit response of circuit 1.

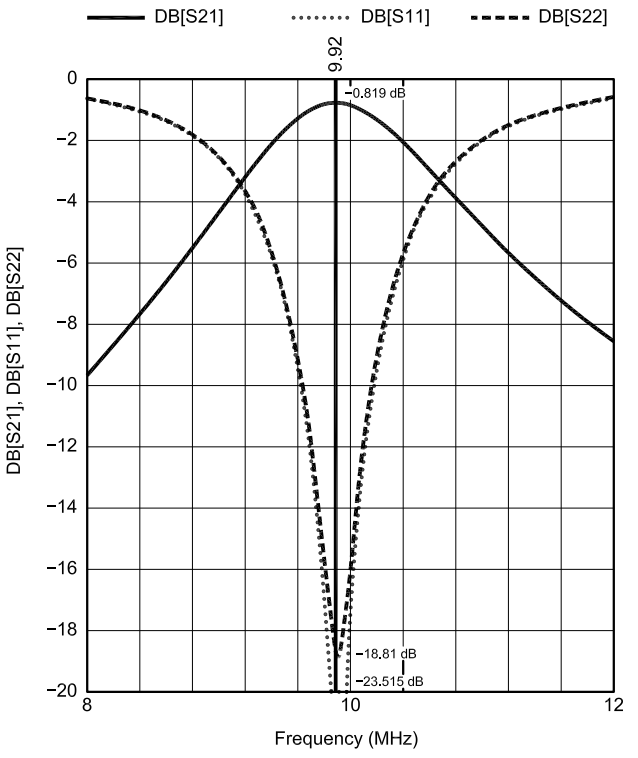


Fig 4—Modified circuit 1 response.

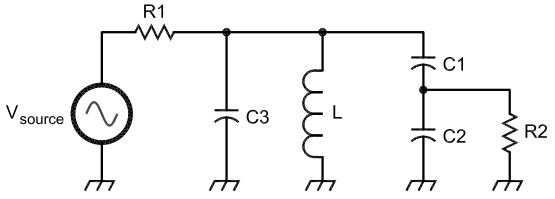


Fig 5—Tapped capacitance matching circuit.

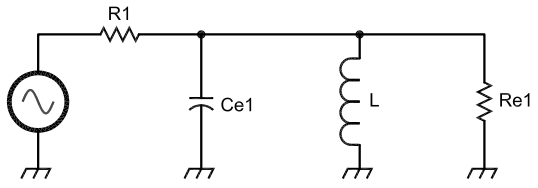


Fig 6—Circuit analysis step 1.

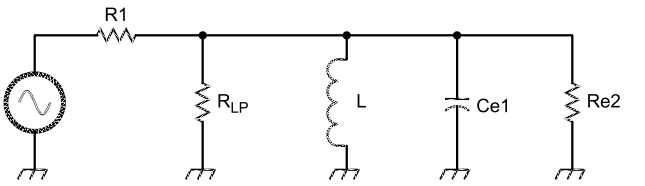


Fig 7—Circuit analysis step 2.

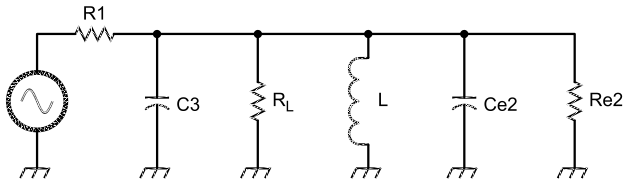


Fig 8—Circuit analysis step 3.

Where C_s equals the series capacitance of *C1* and *C2*. Therefore:

$$C2 = \sqrt{\frac{R_{source} \times {C_s}^2}{R_{load}}} \quad \text{(Eq 2)}$$

and

$$C1 = \frac{C_s \times C2}{C2 - C_s} \quad \text{(Eq 3)}$$

Now, let's assume the center frequency is 10 MHz and the inductor is 4 µH. Resonating capacitor, C_s, would be 63.3 pF. Therefore, for R_{source} = 800 Ω and R_{load} = 50 Ω, *C2* = 253.3 pF and *C1* = 84.4 pF as shown in Fig 2 (notice that capacitor *C1* is shown with a value of 0 pF. This generic circuit was used for further analysis and is ignored for now). However, if the circuit response is plotted as shown in Fig 3 (as depicted by the S21 curve), we can see that the center frequency is 9.34 MHz, not the 10 MHz expected. The transformed impedance at 10 MHz is far from the desired 800 Ω (as depicted by the S11 curve). Clearly, this is not a very accurate solution.

If the inductor value chosen was 1 µH, which implies *C1* = 338 pF and *C2* = 1013 pF, a much more accurate solution occurs as shown in Fig 4. In this case, the center frequency is 9.92 MHz, much closer to the desired value of 10 MHz. This is not yet perfect, but it's much better. In general, Eq 1 is more accurate with low L/C ratios, but it becomes increasingly sensitive to component-value variations. Clearly, a better approach is required for accurate results.

An Exact Solution

The derivation of an exact solution to the design of tapped capacitive matching circuits is now presented for those interested in the nitty-gritty details. The analysis is based upon the circuit in Fig 5.

The analysis assumes the source is on the higher-resistance side of the circuit and the load is in on the lower-resistance side, but the results are applicable to either direction. *C3* is included to allow for any residual capacitance that may be in the circuit, such as may occur in a transistor collector or filter circuit.

For the first step of the analysis, the circuit with respect to the source can be modeled as shown in Fig 6. In this case, *R1* is the source resistance that we are trying to match to; *Re1* is the equivalent parallel resistance and *Ce1* is the equivalent parallel capacitance of the remainder of the matching

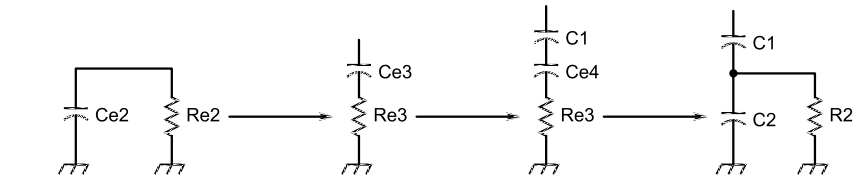


Fig 9—Series/parallel conversion steps.

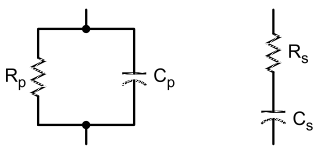


Fig 10—Series and parallel RC circuits.

$$X_p = \frac{1}{\omega C_p} \qquad X_s = \frac{1}{\omega C_s}$$

$$Q_p = \frac{R_p}{X_p} \qquad Q_s = \frac{X_s}{R_s}$$

$$R_{se} = \frac{R_p}{1 + {Q_p}^2} \qquad R_{pe} = R_s\left(1 + {Q_s}^2\right)$$

$$X_{se} = X_p \frac{{Q_p}^2}{{Q_p}^2 + 1} \qquad X_{pe} = \frac{X_s\left({Q_s}^2 + 1\right)}{{Q_s}^2}$$

$$C_{se} = \frac{C_p\left({Q_p}^2 + 1\right)}{{Q_p}^2} \qquad C_{pe} = C_s \frac{{Q_s}^2}{{Q_s}^2 + 1}$$

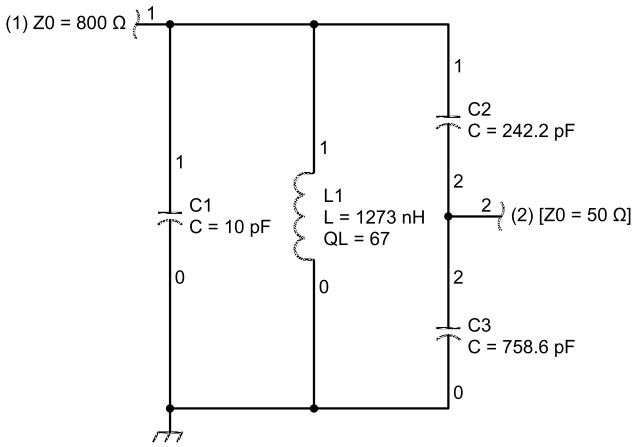


Fig 11—Final tapped capacitor circuit.

circuit.[2] L is the inductor used in the circuit.

Since it is a resonant circuit, the loaded Q equals:

$$Q_{loaded} = \frac{f}{Bandwidth}; \quad f = Center\ Frequency \qquad \text{(Eq 4)}$$

For maximum power transfer, $Re1 = R1$, therefore:

$$Q_{loaded} = \frac{\left(\frac{R1}{2}\right)}{\omega L} \qquad \text{(Eq 5)}$$

where $\omega = 2\pi f_{center}$
and the loaded Q also equals:

$$Q_{loaded} = \frac{(Re1 \| R1)}{X_L} \qquad \text{(Eq 6)}$$

where $X_L = \omega L$
or,

$$L = \frac{\left(\frac{R1}{2}\right)}{\omega \times Q_{loaded}} \qquad \text{(Eq 7)}$$

Therefore, if we define the center frequency, the bandwidth of the matching circuit and the source impedance, we can calculate the required inductor value.

Since the inductor has a finite unloaded Q (this is the Q of the inductor, not the circuit as was presented before), its equivalent parallel resistance is equal to:

$$R_{Lp} = Q_{unloaded} \times X_L \qquad \text{(Eq 8)}$$

since $Q = R_{Lp} / X_L$ for the parallel resisto-inductor circuit $Re1$ can now be broken up into two parallel resistors, with one being R_{Lp} and the other being the equivalent parallel resistance $Re2$ of the circuit due to $C1$, $C2$ and $R2$. The circuit now looks like that shown in Fig 7.

At the resonant frequency, $X_L = X_{ce}$, or $\omega L = 1/\omega Ce1$. Therefore:

$$Ce1 = \frac{1}{\omega^2 L} \qquad \text{(Eq 9)}$$

$Ce1$ can be decomposed into $C3$ and the remainder of parallel capacitance due to $C1$, $C2$ and $R2$ as shown in Fig 8. Therefore, $Ce2 = Ce1 - C3$.

At this point, we have decomposed the circuit down to its final component values for $C3$ and L and the $R2$–$Ce2$ parallel equivalence of $C1$, $C2$ and $R2$. As can be seen in Fig 9, the parallel combination of $Ce2$–$Re2$ can be converted to the series form of $Ce3$–$Re3$. $Ce3$ is the result of the series combination of $C1$ and $Ce4$. $Re3$ and $Ce4$ are the result of the series conversions of the parallel combination of $C2$–$R2$.

To understand this series of steps, it is necessary to understand how to do series-parallel conversions of RC circuits. The conversions of one to the other is shown in Fig 10.

Using the equations in Fig 10 and the steps shown in Fig 9, the final circuit values can now be obtained. First $Re3$ and $Ce3$ are determined from the known values of $Re2$ and $Ce2$.

$$\mathrm{Re3} = \mathrm{Re2}\left(1 + Qs^2\right), \text{ and } Qp = \frac{Re2}{\left(\frac{1}{\omega \bullet \mathrm{Ce2}}\right)} \qquad \text{(Eq 10)}$$

Next, the value of $C2$ is obtained

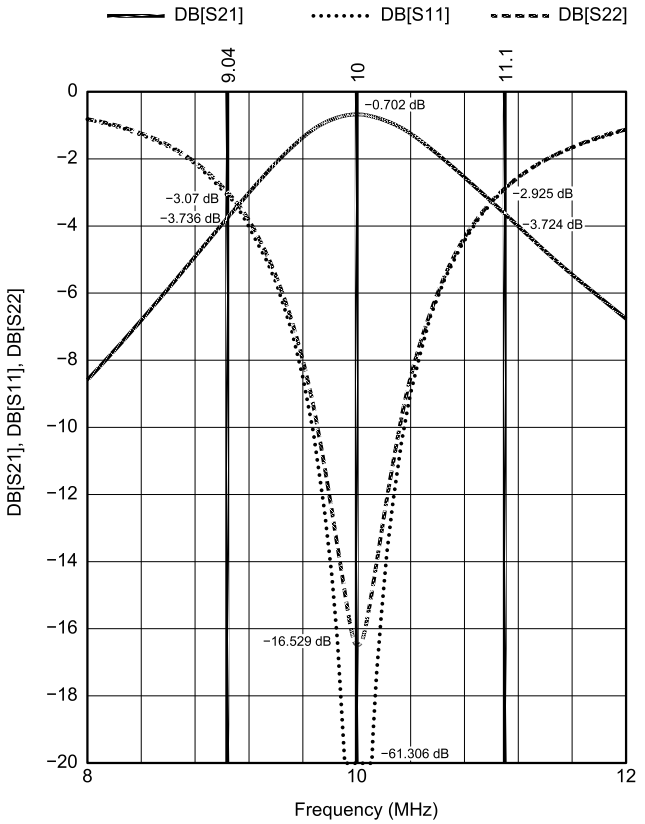


Fig 12—Simulation results for final circuit.

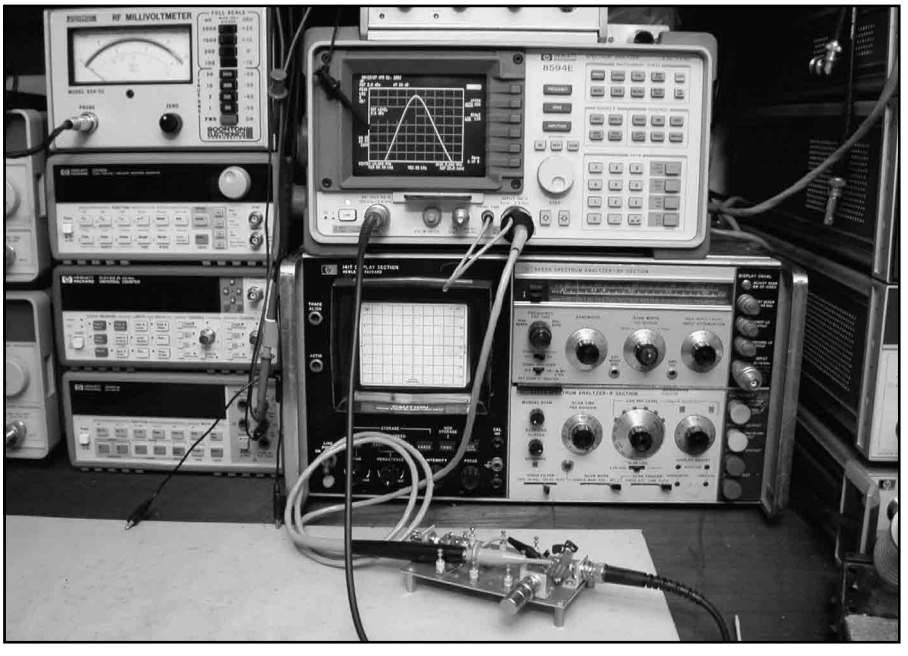


Fig 13—Final circuit breadboard.

from the conversion of *Re3* from *R2* by the parallel to series conversion equation:

$$Re3 \quad \frac{R2}{1+Qp^2}; Qp \quad \frac{R2}{\frac{1}{\omega C2}} \qquad \text{(Eq 11)}$$

and solving for *C2* gives:

Since the series combination of *C1* and *Ce4* must equal *Ce3*, and solving for *C1* gives:

$$C1 \quad \frac{Ce4 \bullet Ce3}{Ce4 - Ce3} \qquad \text{(Eq 12)}$$

Now all values are known.

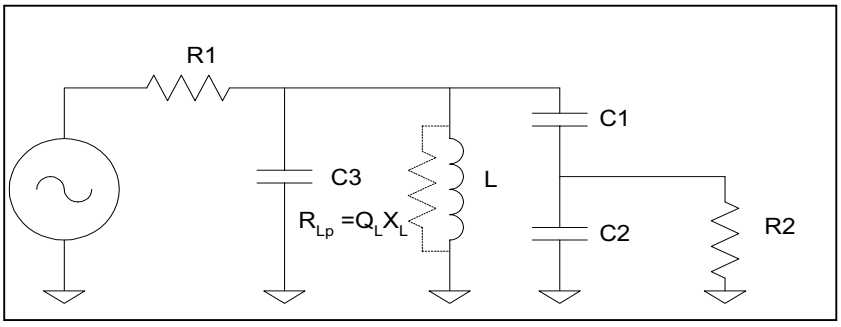
Finally, we want to calculate the insertion loss of the circuit. Since maximum power is delivered at resonance when *R1* = *Re1*, the voltage across *R1* and *Re1* is equal at resonance. The output power is divided between *Re2* and R_{Lp} (assuming all other components are lossless—a reasonable assumption, since the *Q*s of the capacitors are much higher than the inductor), but the voltage across them is the same. If we assume this voltage is *E*, then the power dissipated by *Re2* is $E^2/Re2$. Similarly, the total available power dissipated in both *Re2* and R_{Lp} is the same as that in *R1* since

Appendix A

Excel Spreadsheet for Tapped Capacitive Matching Circuit Design:

Input Parameters:

Fo	**10 MHz**	**Center Frequency**
B	**2 MHz**	**Bandwidth**
R1	**800 Ω**	**Transformed Impedance**
C3	**10 pF**	
R2	**50 Ω**	
QL	**67**	**Inductor unloaded Q**
Qo	**5**	**Circuit Q**
L	**1.273 uH**	
C2	**758.6 pF**	
C1	**242.2 pF**	
Insertion Loss	**0.70 dB**	



Qo	**5**	Qo = Fo/B
X_L	80 Ω	((R1)/2)/Qo
ω	62831853.07 rad/s	ω
Re1	800 Ω	Re1 = R1 for maximum power transfer
L	**1.2732 µH**	L = (R1/2)/(ω*QLoaded)
RLp	5360 Ω	RLp = XL*QL
X_{Ce1}	80 Ω	$X_{Ce1} = X_L$ @ Fo
Ce1	198.94 pF	Ce1 = $1/(\omega^2 L)$
Ce2	188.94	Ce2 = Ce1 – C3
Re2	940.35 Ω	Re1*RLp/(RLp - Re1)
Qp(Re2||Ce2)	11.16	Qp= Re2/(1/(ω*Ce2))
Re3	7.49 Ω	Re3 = Re2(1 + Qs^2),
Ce3	190.46 pF	Ce3 = Ce2(Qp^2 + 1)/Qp^2
C2	**758.60 pF**	C2 = (1/ω)*sqrt((R2 - Re3)/(R2*Re3))
Qp(R2||C2)	2.38	Qp= R2/(1/(ω*C2))
Ce4	892.16 pF	Ce4 = C2(Qp^2 + 1)/Qp^2
C1	**242.16 pF**	C1 = Ce4*Ce3/(Ce4-Ce3)
Loss	**0.70** dB	Loss = 10*log10(R1/Re2)

Re2 in parallel with R_{Lp} is *R1*. Therefore the total available power is $E^2/R1$ and the insertion loss is equal to:

$$Loss_{dB} \quad 10\log\left(\frac{Power\ Out}{Power\ In}\right) \qquad \text{(Eq 13)}$$

or

$$loss_{dB} \quad 10\log\left(\frac{\frac{E^2}{R1}}{\frac{E^2}{Re2}}\right) \qquad \text{(Eq 14)}$$

or finally

$$Loss_{dB} \quad 10\log\left(\frac{Re2}{R1}\right) \qquad \text{(Eq 15)}$$

In order to ease the calculations, an *Excel* spreadsheet was developed and is shown in Appendix A. The user inputs the center frequency, 3 dB bandwidth, source resistance, residual capacitance, load resistance and the unloaded *Q* of the inductor. The spreadsheet then calculates the circuit *Q*, the inductor value, the values for the capacitors *C1* and *C2* and the loss of the circuit.

The example spreadsheet shows the calculated values for transforming 800 Ω to 50 Ω at a frequency of 10 MHz with a 3 dB bandwidth of 2 MHz and an unloaded inductor *Q* of 67. The results are shown in Appendix A and are summarized here:

Q_o, circuit *Q* of 5
L, inductor value of 1.273 µH
C2, capacitor value of 758.6 pF
C1, capacitor value of 242.2 pF
Insertion Loss of 0.7 dB.

Putting the values into *GENSYS*, the circuit is shown in Fig 11. Of course, the question is how accurate are the results of this design?

Simulation and Experimental Results

The simulation results for the final circuit are shown in Fig 12 using the values calculated in the spreadsheet. Notice that the insertion loss of the simulation is 0.7 dB, the same value that the spreadsheet calculates. In addition, the center frequency is exactly 10 MHz and the input and output impedances are very close to the ideal values of 800 Ω and 50 Ω, respectively.

As a last verification step, the circuit was breadboarded as shown in Fig 13 (the breadboard is a generic PC board with ceramic standoffs and BNC connectors mounted to facilitate the testing of various circuit designs). The inductor used had a measured *Q* of 67 @ 10 MHz using an HP-4342A Q-Meter. The load resistor used was an accurate 50 Ω BNC termination. The source resistor was a 750 Ω resistor in series with a 50 Ω termination for a net source resistance of 800 Ω. If the circuit worked as calculated, the measured impedance across the inductor should be exactly 400 Ω at 10 MHz (800 Ω source resistor in parallel with the 800 Ω transformed impedance). Using an HP-4815A Vector Impedance meter, the circuit was measured as shown in Fig 14. The measured impedance was exactly 400 Ω, at a phase angle of 0°, indicating a transformed impedance with no reactance, exactly as predicted. Next the bandwidth was measured as shown in Fig 15 using an HP-8594E Spectrum Analyzer with tracking generator along with a high input impedance FET probe for the spectrum analyzer. The FET probe was required so that the circuit was not loaded down. The measured 3 dB bandwidth was 1.82 MHz, essentially as specified.

Conclusion

The purpose of this article was to present an accurate technique for designing tapped-capacitor matching circuits. I hope that I've convinced you that this technique is a proven and accurate method. While some relatively sophisticated test equipment was used to validate the design technique, it is not necessary to design and use this design method. The only test equipment that may be required is a method to measure capacitance (if accurate capacitors are not available) and a level meter to peak the inductor (assuming it is variable) for maximum power transfer. For example, in my case, the capacitors were measured to an accuracy of ±1% using an inexpensive capacitance meter and an inductor was used that varied between 0.8 and 1.6 µH. The capacitors and inductor were installed on both sides of the 10 MHz filter and the inductors were adjusted for minimum loss through the 10 MHz filter. That's it, no sophisticated test equipment is required. You can be assured the circuit

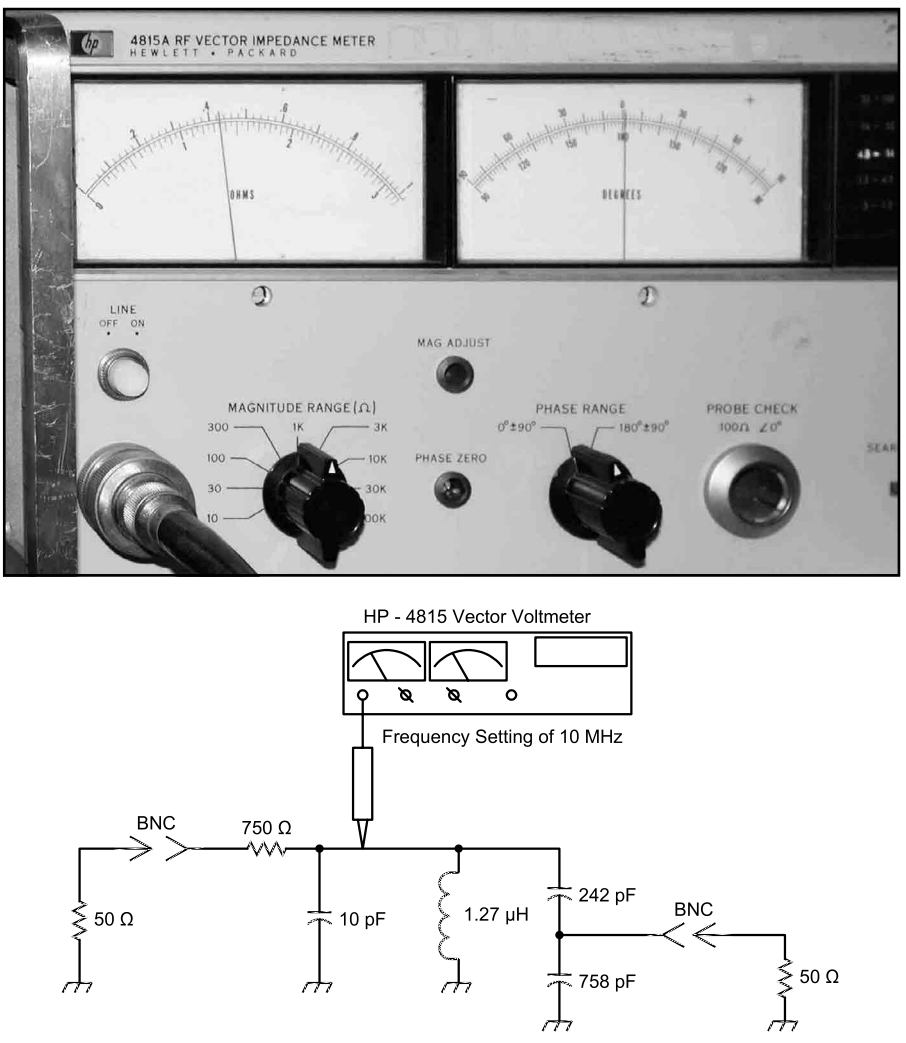
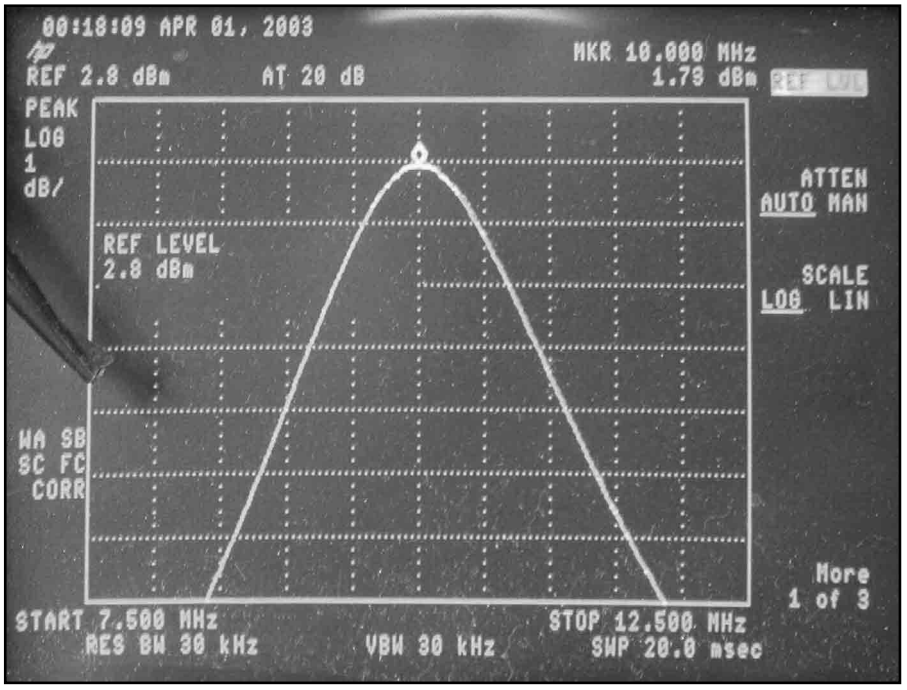


Fig 14—Impedance measurement test setup.



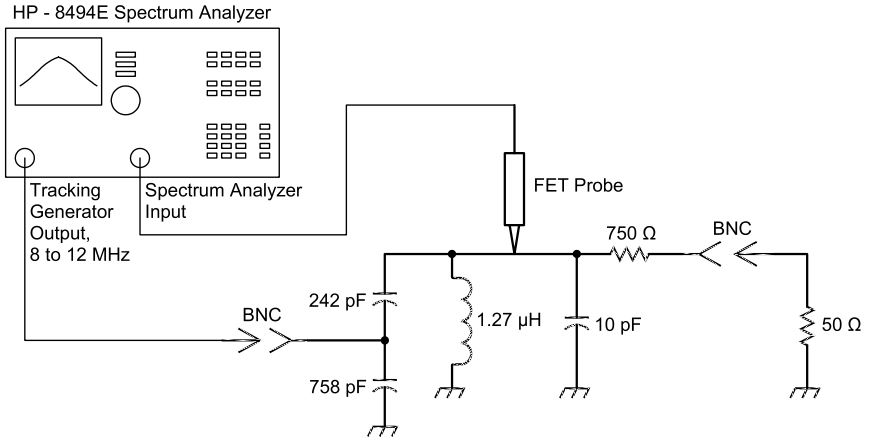


Fig 15—Bandwidth measurement test setup.

will work as calculated if the capacitors are accurate and the inductor can be adjusted for a clear minimum-loss condition. (Be careful, if the loss is minimum at either end of the adjustment range, the inductor may not be adjustable to the required value.) I hope you will find this design method useful for your future designs.

Notes

[1]You can download this package from the ARRL Web **www.arrl.org/qexfiles/**. Look for 0304Evans.zip.

[2]Any single-port network consisting of Rs and Cs, no matter how complex, can be simplified down to either a parallel RC pair or a series RC pair.

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3. H. Krauss, C. Bostian, F. Raab, *Solid-State Radio Engineering*, (Hoboken, New Jersey: John Wiley & Sons, 1980) pp 78.
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Testing Receivers—Some Thoughts

Read about this new method. What are your thoughts?

By Rod Green, VK6KRG

When a receiver has a great dynamic range, it becomes increasingly difficult to make certain measurements for the entire receiver. A good example of this is the third-order intercept (*IP3*). This is so because higher intercept points require a test oscillator with a lower noise floor to make a correct measurement by conventional methods. The receiver's own local-oscillator noise also becomes important and can mask the true reading. As the level of the test oscillator rises, its own noise floor may have a significant component on the received frequency. If so, the noise component of the receiver's own oscillator will mix with the test oscillator in a process called reciprocal mixing.

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These products combined can—and almost certainly will—be amplified by the receiver's high gain stages as an input signal. This will mask the true *IP3* reading because the background noise floor will rise and distort the reading.

I have only been seriously testing receivers for a few years, so I am open to constructive criticism of any information presented here. I almost exclusively build and design my own equipment and sometimes need to measure a parameter for which I am not properly equipped. For instance, in measuring the *IP3* of the Dirodyne series (see Reference 1)—now at revision 7—I measure the *IP3* before the receiver main gain block, or before its selective filter. Thus I can use noisier oscillators to do the work without the danger of upsetting the reading. To do this, I simply measure the levels of the two interfering signals (converted to the IF), read the level of the intermodulation product and calculate *IP3* from that. The assumption is made here that the passive crystal filter will have higher *IP3* performance than most active devices. In some receivers, the *IP3* is determined by several stages and most amateurs would not be likely to do *IP3* measurements on their equipment because, it being commercial, they are unlikely to want to disturb the circuitry.

There are other tests that are easier to do and perhaps an amateur standard specification could be tried. May I suggest that a series of "blocking" tests may be of more value than the *IP3* test? Incidentally, I measured the *IP3* of the Dirodyne 7 to be +30 dBm.

Definitions and Terms

SCF: Suppressed carrier frequency (zero beat)

MUS: Maximum useable sensitiv-

ity, for a 20 dB SINAD.

SNR: Signal to noise ratio.

Test Conditions

The test setup should be as shown in Fig 1. The receiver is set to upper sideband and tuned to any desired frequency. The weak signal generator is set to SCF +1.0 kHz with its level at 20 dB SNR.[1] The strong signal generator has its output switched off.

Proposed Test

The tests described below will be useful in comparing the performance of different receivers under strong-unwanted-signal conditions. Some receivers will suffer actual blocking from the strong signal causing gain compression in an early stage of the receiver. This was the limiting factor when testing the R-1000 receiver, the one I compared with the Dirodyne 7.

The other factor limiting receiver performance is reciprocal mixing, wherein the receiver's local oscillator noise becomes the signal and the strong unwanted signal becomes the local oscillator. This is the case in the more robust receivers designed for strong signal handling. This happens because the early stages of the receiver just don't overload at the higher test levels. The Dirodyne 7 is such a receiver.

Thus one test can be used for both strong and weak front-end checks, but the mechanism for performance limitation may be by blocking or reciprocal mixing. In either case, the receiver's signal handling can be checked against another directly. One could determine the why of performance limitation later if desired. Of course, both blocking *and* reciprocal mixing can occur simultaneously.

A single low-noise test oscillator such as the HP-8640 generating a strong unwanted signal and any other good-quality test oscillator generating a weak signal could be summed with a hybrid combiner and applied to the antenna connection of the receiver under test.

The receiver should be tuned to the weak signal and the strong signal generator should be turned off. Adjust the weak signal generator for a signal level that gives a SNR of 20 dB. This is ideally measured with a distortion and noise meter. However, if you are certain that the receiver's AGC is inactive at this level, you can just use signal-to-noise by comparing the ratio of signal on to signal off audio levels as your reading. The SNR (in decibels) is calculated from the formula SNR = 20 log (signal/noise). If you use a noise and distortion meter, the chances are good that it will display the ratio in decibels, directly. Note the input level in either dBm or dBμV—I prefer dBm, as it is an absolute power level—according to units used for your oscillator calibration. Remember to account for the loss of the combiner you use (normally 6 dB).

Once the MUS above has been determined, the strong-signal performance can be measured.

Adding the Blocking Signal

Adjust the high-level oscillator frequency to SCF +5 kHz, assuming you have a SSB filter narrower than 5 kHz: 2.4 kHz is typical. Adjust and record the level of this oscillator to bring the SNR from 20 dB to 10 dB. Call this the +5 kHz level.

Re-adjust the frequency to SCF +10 kHz and change the level to once again give an SNR of 10 dB. Call this the +10 kHz level and record the level.

Re-adjust the frequency to SCF +15 kHz and change the level to once again give an SNR of 10 dB. Call this the +15 kHz level and record the level.

Repeat this process for SCF +20 kHz, SCF +40 kHz and SCF +500 kHz. You may for some specific reason want other frequencies, but be careful to avoid spurious response frequencies.

Set Out the Results

Set the results of the test in some easy to read format such as shown in Tables 1 and 2 below. These tables show actual measurements taken on both the Dirodyne 7 and a Kenwood R-1000. The difference between the two receivers can be clearly seen. Table 1 shows the measured readings as described above, and Table 2 shows the blocking dynamic range. The dynamic range (*DR*) is found by calculating the difference between the specified MUS and the level where the SNR becomes 10 dB.

There is no reason to prevent taking, say, the 10-dB SNR point for MUS and the 3-dB point for the blocking

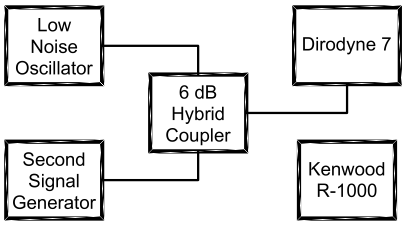

Fig 1—Comparative blocking test setup.

Table 1

Measured Blocking Signal Levels

	DIRODYNE MODEL 7	*KENWOOD R-1000*
MUS	–110 dBm	–109 dBm
+5 kHz	–18 dBm	–54 dBm
+10 kHz	–12 dBm	–44 dBm
+15 kHz	–6 dBm	–36 dBm
+20 kHz	–4 dBm	–34 dBm
+30 kHz	–2 dBm	–30 dBm
+40 kHz	–4 dBm	–25 dBm
+500 kHz	–13 dBm	–6 dBm

Table 2

Measured Blocking DR.

	DIRODYNE MODEL 7	*KENWOOD R-1000*
+5 kHz	92 dB	55 dB
+10 kHz	98 dB	65 dB
+15 kHz	104 dB	73 dB
+20 kHz	106 dB	75 dB
+30 kHz	108 dB	79 dB
+40 kHz	106 dB	84 dB
+500 kHz	97 dB	103 dB

[1]If AGC is active, the signal will push the noise down and it will rise again when the signal is disconnected to check the noise. This will make the receiver seem less sensitive than it really is. In such a case it will be necessary to use a noise and distortion meter to remove the 1 kHz tone, thus enabling the signal to be present whilst the signal and noise are read.

reading. However you must test the compared receivers in the *same* manner and with the same levels. This will, however, make the results differ from those above for the same receivers. Yet, it will still show the difference between the two. Therefore, if you wish to compare your receiver to the Dirodyne, for instance, you would need to set it up under the same conditions, which are quoted in full above.

As can be seen from the above, the specification sheet for a receiver should have—but seldom does—the exact conditions and method of testing written down. This of course does not apply to *IP3*, which is a fixed quantity for all intents and purposes. However, as we have also seen, *IP3* can be excellent, but performance can be spoiled by local oscillator noise. The above or similar multiple-frequency blocking test will pick this up.

A Word of Caution

When testing in the above manner, it will be important that the effects of sharp front-end filters are taken into account. Keep clear of the band edges as this can make a receiver look better than it really is, especially when test points are hundreds of kilohertz apart. About the only exception to the above is where the receiver has a tunable preselector. It is legitimate to include this because it will normally be peaked at the operating frequency and is an integral part of the receiver.

Alternative Test Methods

An alternative test procedure for local-oscillator noise testing is discussed in Reference 2. In this instance, a single off-frequency oscillator is used to raise the noise level of the receiver. I found that this test worked very well for strong receivers such as the Dirodyne7. This is because the strong signal of –30 dBm at 10 kHz away from SCF only raised the noise floor by 0.5 dB. This is well below the onset of AGC, and thus the readings taken were accurate. There was also no front-end compression to influence the readings. However, such was not the case when I tested the comparison R-1000 receiver. The main reason was that the meter readings were telling me that the AGC was active in suppressing the true change noise reading. Thus, by using the method shown in Reference 2, it was not possible to directly compare the two receivers. This is why I like the idea of having a low-level reference tone to get a true and verifiable SNR change, rather than a noise change only. For interest, the results of the above test done on the Dirodyne 7 are shown in Table 3.

Table 3

Test results for the Dirodyne 7 when tested as described in Reference 2.
Test Oscillator: HP-8640.
Noise and distortion meter: HP-334A.
Output level: –30 dBm
Test frequency (SCF): 7010 kHz
Offset for LO noise test: +10 kHz
AGC: Off (not active)
Increase in background noise level @ +10 kHz offset (–30 dBm): 0.5 dB
Level required for equal RMS audio level at SCF +1 kHz: –140 dBm
Difference –30 – (–140) = 110 dB
Normalized for 2.4 kHz (measured) bandwidth (10 log 2400)+ 110 dB = 144 dB
At SCF +10 kHz, the result was 144 dB
At SCF +6 kHz, the result was 143 dB
At SCF +3.5 kHz, the result was 132 dB

Observations and Conclusions

The main reason I did these tests was to find a simple objective test for my new Dirodyne designs. This, in turn, led me to start a discussion on a de-facto receiver-testing regime that is cost effective for amateurs. Personally, I think the above tests clearly show a receiver's performance limitations, regardless of whether it's caused by compression or phase noise. In future, it seems that development of low-noise synthesizers will be more important than increasing *IP3*, because the local oscillator noise floor is currently the limiting factor in receiver design. This means that tests more meaningful than *IP3,* alone, are needed because this no longer limits receiver performance. Tests such as those shown above, if adopted universally as a standard, could be a valuable radio tool.

Tables 1 and 2 show clearly that the Dirodyne 7 close-in dynamic range is superior to that of the R-1000. The difference tapers off and the R-1000 becomes a little better than the Dirodyne when the unwanted signal is 500 kHz away. Beyond this, the front-end filter on the Dirodyne causes its performance to improve.

At the time of writing, I don't know why the Dirodyne strong-signal performance drops off as the unwanted frequency is far removed from the wanted signal. Perhaps it is because it uses a transmission-line local oscillator, and it may have a noise profile that increases away from resonance. If so, this goes against the norm (LC oscillator). One thing is certain however: It is a reciprocal mixing rather than a compression problem. This has been observed because the SNR falls with increasing level from the strong-signal oscillator without affecting the actual level of the output tone. If it were blocking the mixer, the output level of the wanted signal would fall, due to gain compression, causing SNR reduction.

Alternatively, I wonder if this phenomenon is due to a noise-canceling ability of the modified Tayloe mixer? It is certainly something that needs further investigation.

The Dirodyne is to be accepted commercially by at least one and possibly two manufacturers, so it is now commercially sensitive. I feel that this field is still wide open for other amateurs to develop independently. It's a bit like a gold rush: Get in and stake a claim on something new!

References

1. R. Green, VK6KRG, "The Dirodyne: A New Radio Architecture?" *QEX*, Jul/Aug 2002, pp 3-12.
2. W. Hayward, W7ZOI; R. Campbell, KK7B; R. Larkin, W7PUA, "Evaluating Noise in Local Oscillator Systems," *Experimental Methods in RF Design*, (Newington: ARRL, 2003) pp 7.40 and 7.41.

Rod's technical background dates back to 1968 when he trained to specialize as a technician in radio communications and in the TV and broadcast areas of the Commonwealth government. He became a licensed amateur in 1976. He has been in the industry ever since, but became involved in design and engineering over a decade ago. He has published radical designs in this magazine on two previous occasions and feels that he hasn't reached the zenith of his profession yet. He is current employed at Barrett Communications as an analog design engineer, and Barrett company has opted to adopt the Dirodyne technique for their next transceiver. An early version of the Dirodyne was published in QEX previously. Another company wants to use this technique in its future designs. Rod hopes to keep on developing new variations of the Dirodyne, and has at least three more unique versions to build. He has enough to keep him busy for at least another decade! □□

RF

By Zack Lau, W1VT

Generating a 1296 MHz Signal

A clean 1296 MHz signal is often needed for testing homebrew designs—many signal generators don't cover this band. Here are two techniques for extending a lower frequency signal generator to cover this band—frequency multiplication and heterodyning. It is useful to have both techniques—they are superior in different ways.

The multiplying technique is usually simpler, needing just one signal source. A mixer needs two sources. This is quite useful when you need a lot of signal sources. A good example is measuring the two-tone input intercept of a mixer. For this you need three high-quality signal generators: two input signals and another for the local oscillator. The disadvantage is that you can't put an amplitude-modulated signal through a multiplier and expect to get a frequency-shifted version at the output. For that you need to use a mixer to heterodyne your signal to the proper frequency.

The linear-frequency-translation feature of mixers is their biggest advantage. You can generate whatever modulation you like at a much more convenient lower frequency and move it up to a microwave band. It is even useful for moving signals down in frequency. Signal generators are often limited in the amount of deviation they can generate at low frequencies—they may not be able to generate a WBFM signal at 30 or 10.7 MHz for testing a detector. A disadvantage of mixers is that they generate lots of signals—not just the sum and difference products but sum and difference products of multiples of the input frequencies.

$$f_{out} \quad n \bullet f1 \pm m \bullet f2 \qquad \text{(Eq 1)}$$

Where n and m are whole numbers (...,–3, –2, –1,0 , 1, 2, 3, ...) and $f1$ and $f2$ are the input frequencies.

Filtering out just the one you want can be a lot of work. If you aren't careful, the task might not even be possible. Suppose you wanted to mix 432.001 MHz with 864.00 MHz to get 1296.001 MHz. The spur at 1296.003 is too close for removal with a band-pass filter. Fortunately for most applications, the unwanted signals get smaller as the m and n coefficients get bigger. With that in mind, one might wonder why people use a 144 MHz IF to generate a 1296 MHz signal, since

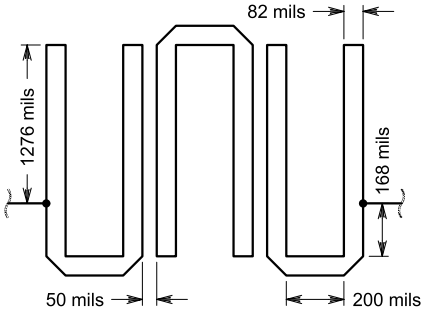

Fig 1—Dimensions of the 1296 MHz microstrip band-pass filter on 30-mil-thick ε_r = 2.55 Teflon board.

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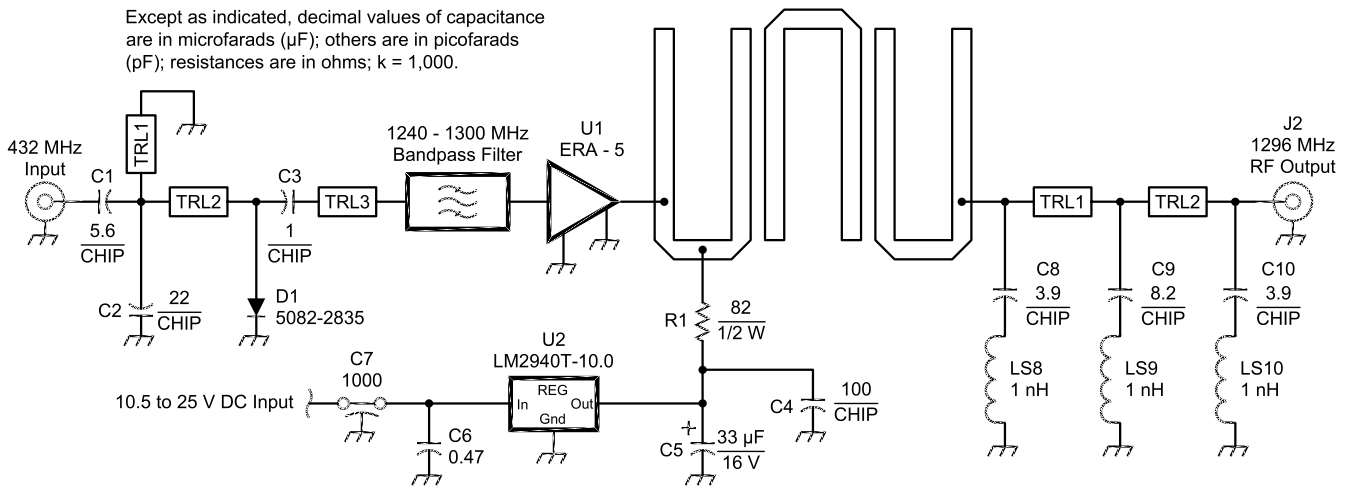

Fig 2—Schematic of the 432 MHz to 1296 MHz multiplier.

C7—Feedthrough capacitor, value not critical.
C8, C9, C10—1206 cased chip capacitors. Substituting a different size may change the filter cutoff frequency.
D1—Agilent 5082-2835 Schottky diode.
J1, J2—SMA female connectors, panel mount.
LS8, LS9, LS10—1 nH parasitic inductance of the capacitors.
TRL1, TRL2—60-mil-wide, 380-mil-long microstrip on 30-mil thick ε_r = 2.55 Teflon board.
U1—Mini-Circuits ERA-5 MMIC.
U2—National Semiconductor LM2940T-10.0 low-dropout voltage regulator.

the ninth harmonic of the 144 MHz signal can't practically be filtered out. Historically, there have been many 2-meter radios available for use at the IF. In contrast, 222 MHz SSB radios are quite rare. From an operating standpoint, 50 MHz is a poor choice—it can magically come to life at any time, so many serious operators like to have it available at all times. In practice, the ninth harmonic of the IF signal is usually quite weak for two reasons. First, the 2-meter signal level is kept quite low to reduce intermodulation distortion (more commonly known as splatter on SSB). Second, high-order mixing products (large values of m or n) are usually quite weak. Not surprisingly, multiples of the low-level IF signal are much weaker than the multiples of the saturating LO. Thus, this technique often works well for transmit IMD testing, since the mixing spurs are small compared to the distortion being measured.

With sufficiently small signals, mixers are usually linear with regard to amplitude. This can be quite useful for testing receivers—instead of attenuating the output one can attenuate the input and still obtain an accurate variation in signal level. Thus, one can use a low-frequency attenuator at the IF connection, instead of costly microwave equipment at the desired output frequency. At microwaves, it is quite easy for radiated RF to leak around attenuators, making them inaccurate.

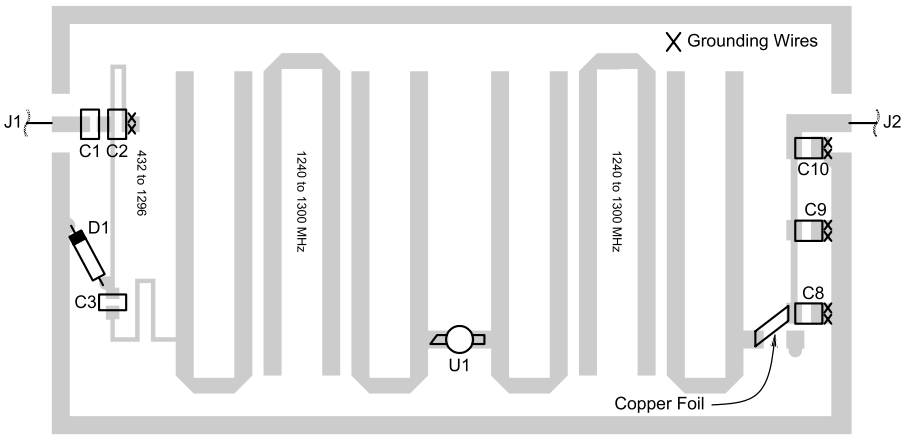

Fig 3—Parts placement diagram for the tripler board.

Frequency Stability

Frequency stability is an important consideration at 1296 MHz and higher frequencies. Vintage signal generators are often lacking in this regard—they often weren't designed for evaluating voice-bandwidth SSB signal-processing systems. Even the popular HP-8640Bs are marginal in the application, if you multiply a 432 MHz signal by a factor of three. There is a phase-locking feature, but it only locks to the nearest kilohertz, so the signal can warble over a 3 kHz bandwidth. The warbling can be quite bad if the generator has just been turned on—the signal sounds a lot better if the generator has been warmed up a while. There is a lot less drift if you use a 144 MHz signal and heterodyne it to 1296 MHz with a stable crystal oscillator.

If you are careful, there are clever techniques for eliminating frequency drift when evaluating microwave systems. For instance, the same LO can be used for both the up converter and down converter, eliminating the drift of the local oscillator. This is useful

Table 1

1296 Low-pass filter with inadequate grounding, notice the significant attenuation in the 23 cm band.

f(MHz)	*IL (dB)*
985	1.83
1086	1.0
1153	1.33
1123	0.66
1248	3.83
1296	9.83
1397	26
1446	34
1480	43
1524	51

Low-pass filter with better grounding

f(MHz)	*IL (dB)*
1249	1.0
1270	0.83
1282	0.83
1290	1.0
1297	1.33
1300	1.50
1311	1.83
1347	3.83
1440	10.83
1496	20.33
1578	30.66
1630	40.33
1715	50.66

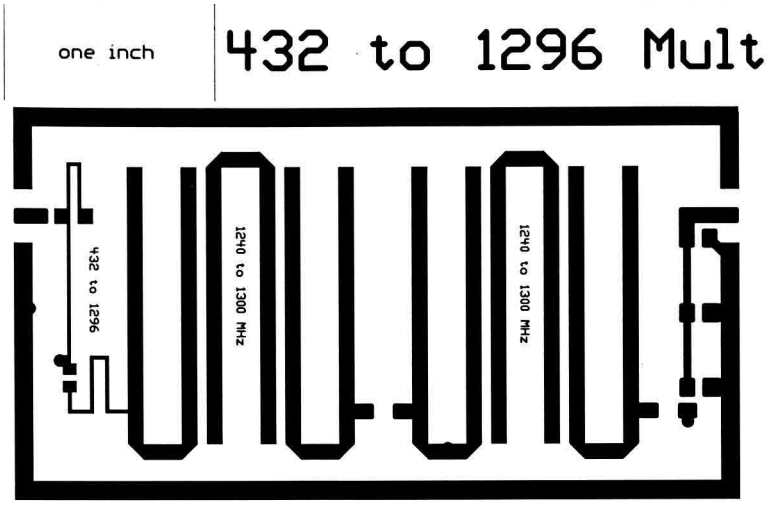

Fig 4—Circuit-board layout for the tripler.

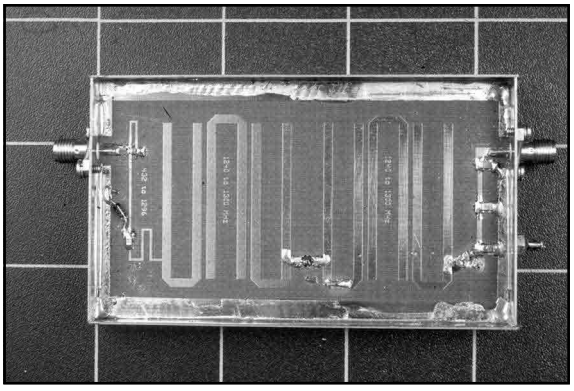

Fig 5—Photograph of the 432 to 1296 MHz tripler.

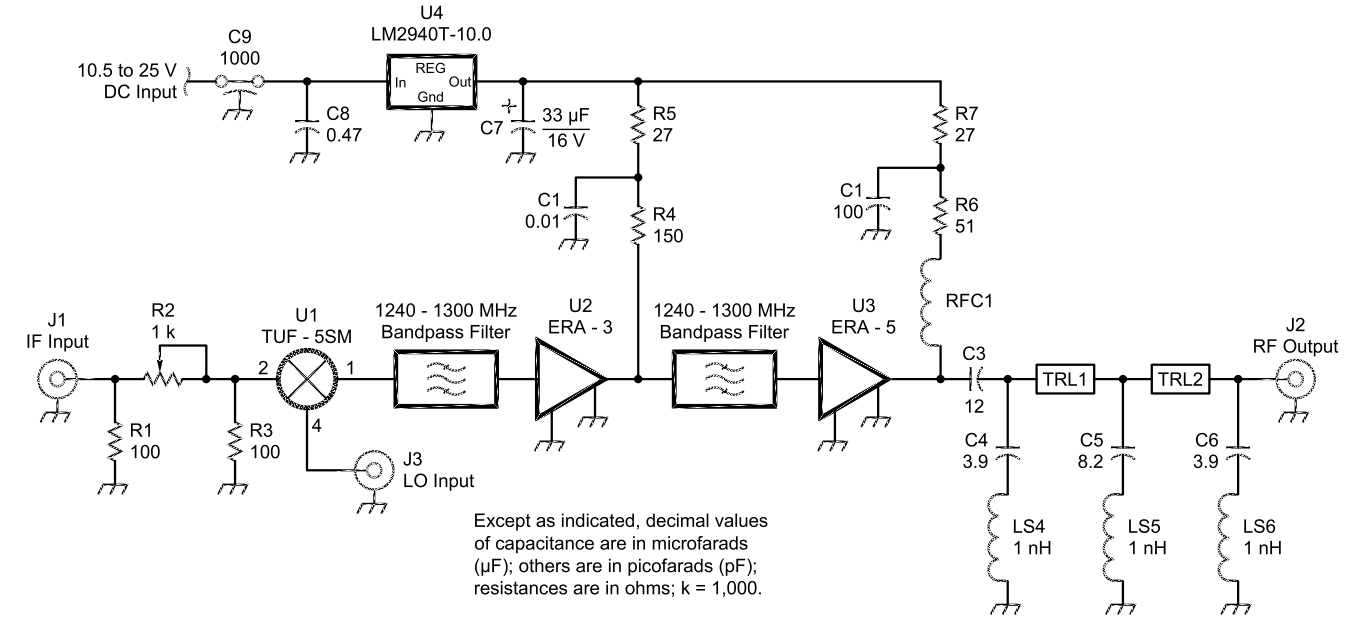

Fig 6—VHF to 1296 MHz upconverter.
C4-C6—1206 cased chip capacitors. Substituting a different size may change the filter cutoff frequency.
C9—Feedthrough capacitor, value not critical.
J1, J2—SMA female connectors, panel mount.
LS4-LS6—1 nH parasitic inductance of the capacitors.
TRL1, TRL2—60-mil-wide, 380-mil-long microstrip on 30-mil-thick ε_r = 2.55 Teflon board.
U1—Mini-Circuits TUF-5SM mixer.
U2—Mini-Circuits ERA-3 MMIC.
U3—Mini-Circuits ERA-5 MMIC.
U4—National Semiconductor LM2940T-10.0 low-dropout voltage regulator.

when measuring two-tone distortion at very narrow offsets. This technique is also useful for sweeping heterodyne systems.

432 to 1296 MHz Tripler

The first step was designing the band-pass filters. I chose to use 30-mil-thick Teflon board instead of the usual glass epoxy. While G-10 or FR-4 works at this frequency, the variation in thickness of the material makes it tough to get repeatable boards, unless you carefully screen the board material. Fortunately, screening can be done easily with an inexpensive dial caliper. More importantly, the loss of G-10 is often 10 times worse, requiring filters be much wider for a given insertion loss. Actually, G-10 would probably work since an ×3 multiplier, or tripler, can accommodate relatively broad filters, but I wanted to use the same filters for both designs. The measured –1 dB bandwidth is from 1258 to 1303 MHz, or 45 MHz. The measured –3dB bandwidth is from 1248 to 1320 MHz, or 72 MHz. The modeled –1 dB and –3dB bandwidths are from 1244 to 1309 MHz and 1233 to 1318 MHz—a bit wider. The filter dimensions are shown in Fig 1.

The board thickness is an important consideration, even though radiation loss isn't likely to be a big factor at this frequency. The newer MMICs have short leads, which makes them tougher to install in $^1/_{16}$-inch-thick board. Actually, this makes some sense, since the newer MMICs designs with more gain probably don't like to see all that lead inductance. Glass-epoxy board is commonly $^1/_{16}$ ″ thick—microwave substrates are usually much thinner.

I designed the low-pass filter next. The filter showed the need for good grounding at the devices. Even though the chip capacitors were only 0.1 inches from the brass walls, it was still necessary to install Z-wires at the chip capacitors to get the desired filtered response. Table 1 shows the severe passband shift. At 1.3 GHz, the series inductance of the chip capacitors becomes significant in determining the cutoff frequency of the filter. Figs 1-5 show details of the multiplier circuit.

The multiplier was then designed using Microwave *Harmonica*, a harmonic-balance program sold by Compact Software. It does the difficult large-signal circuit simulations required for modeling non-linear circuits. It features advanced microstrip

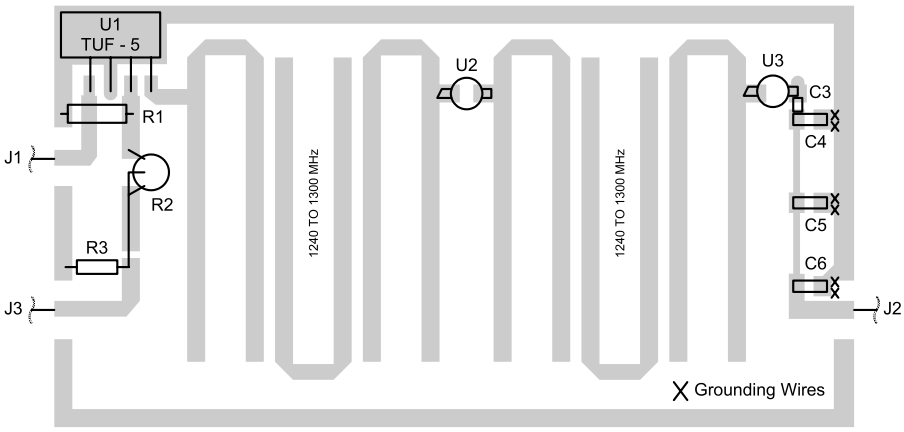

Fig 7—Parts placement diagram for the mixer board.

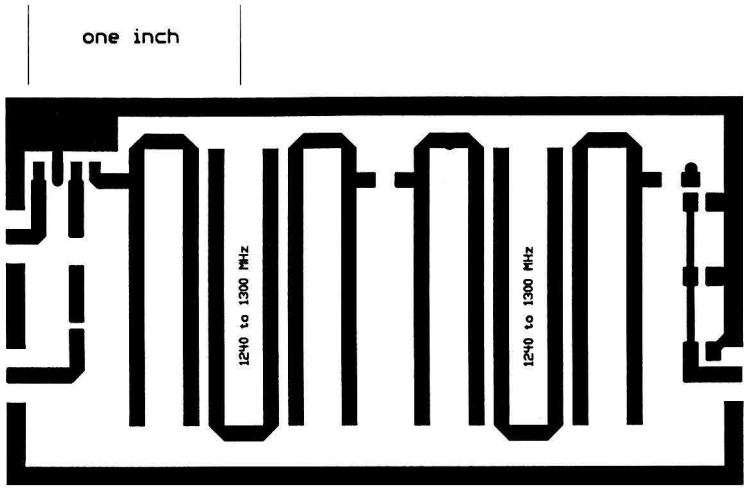

Fig 8—Circuit-board layout for the mixer board.

Table 2—Multiplier Spectral Purity

(+10 dBM input and ERA-5 amp)

f(MHz)	*Output level (dBc)*
432	–55
864	–50
1296	+11.67 dBm
1728	–57
2160	–47
2592	–55

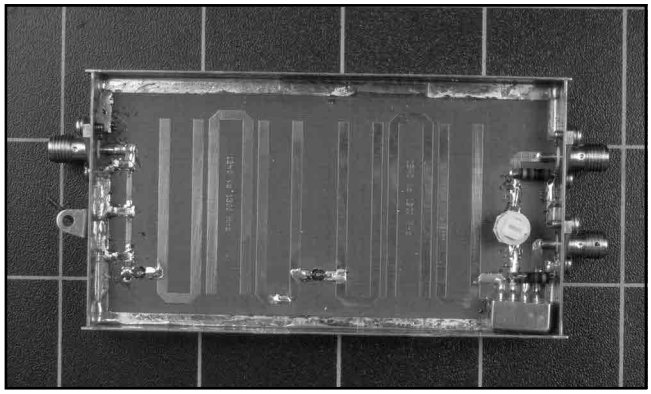

Fig 9—Photograph of the mixer board.

models, such as bends and T connections. Compact Software is no longer in business—Ansoft acquired it. While their full-featured simulator is too expensive for most amateurs, Ansoft does offer a student version of its programs on CD and via Internet download.[1] CDs are more practical for hams with slow Internet connections.

VHF to UHF Transverter

Converting the multiplier to a mixer is quite simple, now that packaged mixers are readily available from Mini-Circuits. At one time, it was common for amateurs to "push" Mini-Circuits SBL-1X 1-GHz mixers to work at 1.3GHz, but these days it is relatively easy to get mixers that work all the way to 6 GHz. At 10 GHz, it may be easier to make your own mixer, although surplus mixers can be located if you have the right connections. *The ARRL UHF/Microwave Projects Manual*, volume 2, has a simple X-band mixer design. It uses a 6/4-λ microstrip hybrid combiner to feed a series diode pair. It is bilateral, unlike the branch line or 90° hybrid, which is only useful as a receiving down converter.[2] Details of the upconverter are shown in Figs 6-9. The Mini-Circuits TUF-5SM mixer works well with +4 to +10 dBm of local-oscillator drive. According to the manufacturer, this mixer is designed to work well with LO and RF signals between 20 and 1500 MHz. The IF should be between dc and 1000 MHz.

Construction

The circuit-board layout package[3] includes a mirror image of the board. This allows easy fabrication using "iron on" photocopy techniques that work best if you have a mirror image. You can go straight from the print to the desired transfer material. Mirror imaging isn't a problem with the multiplier—it may be a problem with the mixer. I've not tested whether mounting the mixer on the ground plane and bringing the leads through the board has any significant effect on performance.

I punched holes in the board for the MMICs—this allows the leads to lie flat against the board, reducing lead inductance. The MMIC ground leads are bent against the body of the MMIC, and then folded against the copper foil after being placed in the punched hole. It is necessary to install additional grounding wires at the grounded ends of the capacitor. These can be discarded 1/4-W resistor leads or #24 tinned wire. The locations are marked with Xs on the parts placement diagram.

Before any components are installed in the punched board, I install the board in a frame made out of 25-mil × 1/2-inch brass strip. This reduces the chance of board flexure breaking the chip capacitors. The coax connectors are first mounted on the strips, and then tack soldered to the board for proper alignment. Then the two sidewalls are tacked on. Finally, the top and bottom ground foils are soldered to the walls.

I usually mount the surface-mount parts first, and then assemble the power-supply parts on the other side of the board. This insures easy access to the entire ground plane. The power supply is assembled with ground-plane or "ugly" construction techniques.

Notes

[1]Ansoft Corp, Four Station Square, Ste 200, Pittsburgh, PA, 15219-1119; tel 412-261-3200, fax 412-471-9427; e-mail **info@ansoft.com**; **www.ansoft.com/downloads.cfm**.

[2]P. Wade, W1GHZ, "Mixers, Etc, for 5760 MHz," *The ARRL UHF/Microwave Projects Manual*, volume 2, (Newington: ARRL, 1997) pp 3-28 to 3-29.

[3]You can download this package from the ARRLWeb at **www.arrl.org/qexfiles/**. Look for 0403RF.zip. □□

Letters to the Editor

Crystal Parameter Measurement and Ladder Crystal-Filter Design (Sep/Oct 2003)

Doug,

I sent an e-mail a few months ago regarding the *Excel* spreadsheets for the article on crystal filter design published in Sept 2003 *QEX*. They are not on the *QEX* software download section and I keep getting requests for the spreadsheets. I had included them in the article submission but they never made it to the Web site. Is there a reason they were not put on the Web site? If not, could they be added so people don't need to contact me to get the spreadsheets? Thanks.—*Randy Evans, KJ6PO, 2688 Middleborough Cir, San Jose, CA 95132-2113;* **randy@stratalight.com**

Randy,

It is done! Navigate to our file area and look for ***0309evans.zip—****Doug Smith,* QEX *Editor,* ***kf6dx@arrl.org****.*

Letters to the Editor (Chadwick, Sep/Oct 2003)

Doug,

Just a note to let you know how much I appreciate *QEX*. I read all the articles with great interest and have learned so much from the different authors.

I encourage all readers to submit their thoughts and experiences even if it is just a note to the editor. Case in point: In Sept/Oct 2003, Letters to the Editor, Peter Chadwick, G3RZP, wrote about patents and relays. The part about relays really sparked my interest as I had been having trouble with the relays used to switch the input RF filters in my homebrew transceiver. Every once in a while one of the relays began to show signs of what I thought was a relay failure but as Peter pointed out in his letter, it was due to oxidation of the contacts.

I have since modified my transceiver so that about 0.7 mA dc flows through all the relay contacts when they are engaged. At first, this didn't work as some of the contacts were already oxidized. By increasing the current to about 100 mA (about 80% of the total current capabilities of the relay contacts) and switching the relays on and off many times (50 to 100 times worked for me), the higher current as the relays make and break cleaned the contacts. When the contacts were clean, I reverted back to the lower-current circuits.

I have had no trouble with intermittent relay contacts since making the above mentioned changes. So please keep the good ideas coming! Thanks to Peter for the timely advice and to Doug for printing it in *QEX*!—*Markus Hansen, VE7CA, 674 St Ives Cres, North Vancouver, BC V7N 2X3, CANADA;* **ve7ca@rac.ca**

Markus,

Thanks for the note. The business of putting dc through relay contacts is much older than I am. Telephone people were doing it 100 years ago! It's one of those technology items that get lost occasionally.—*Peter Chadwick, G3RZP, Three Oaks, Braydon Swindon, SN5 0AD, Wiltshire, Great Britain;* **peter.chadwick@zarlink.com**

A 200-W Power Amplifier (Jan/Feb 2004)

Hi Doug,

The switching FET amplifier is great idea, but the graphics and figure editing are a mess. I think in the Fig 4 photograph, T2 is the item labeled L2 in the Fig 3 schematic. The data for T1 is ambiguous in that it says 1:2 [turns] ratio and then just says two turns on a RF400-0 core. The schematic suggests that it has a center-tapped secondary or a bifilar secondary—or is it a trifilar device? The text says inductors are wound on various forms, but they appear to be air wound. Perhaps the text should be "form factor"?

The photograph (Fig 4) is confusing in that the primary and secondary of T2 seem to be soldered to the same PC-board trace structure and the center-tapped feed is blocked by the coils themselves Also L3 and L4, the adjustable coils on the gates are not visible in the picture. Great idea, great theory, marginal presentation. I expect a bit more from *QEX* and its editors.—*Bob Miller, KE6F, 9655 Appalachian Dr, Sacramento, CA 95827-1110;* **BMiller@smud.org**

Dear Bob,

You are right about those mix-ups and you are not alone in finding them. We apologize. We have been trying to put together a proper correction and clarification with the assistance of the authors, but it is not yet ready. The moment it is, we shall post it either to ***www.neoamateur.org*** *or to our file area at* ***www.arrl.org/qex*** *and we shall run it in the next issue—Doug Smith*

A Cascade Regenerative Receiver (Jan/Feb 2004)

Mr. Smith:

In recent years a number of articles about regenerative receivers have appeared in radio amateur publications.[1-8] These articles mention two notorious qualities of regenerative receivers: (1) sensitive and unstable tuning, and (2) a characteristic noise ("mush") that these receivers add to a detected signal.

It occurred to me that such behavior might be due to the presence of what physicists and mathematicians have dubbed "chaos" in these receivers: The positive feedback that's used in these receivers might drive their active devices to behave nonlinearly, which in turn might cause the circuits to behave chaotically.

A search of the Internet revealed that I wasn't the first person to consider this conjecture.[9-10] Domine Leenaerts of Philips Research Laboratories in Eindhoven, the Netherlands, had discovered the presence of chaos in his computer models of super-regenerative receivers. He found that the tuning of super-regenerative receivers is sensitive and unstable because the receiver's gain is greatest just before the receiver begins to oscillate. At this point the receiver is behaving chaotically. The characteristic noise ("mush") of superregenerative receivers is the sound of this chaos.

Perhaps radio amateurs might try to verify the presence of chaos in *real* superregenerative receivers—as opposed to mere computer models of such receivers.—*Chris Kirk, NV1E, 40 Westwood Road, Shrewsbury, MA 01545;* **Cwkmail@aol.com**

Notes about Ref 10:

1. On the first page of the PDF file (which is page 169 of the original article), near the top of the right-hand column:

Although the basic operation of the [superregenerative receiver] *circuit was understood, there was still the problem of the* characteristic noise *generated in those circuits. One assumed that the characteristic noise, which could be heard in the earphones, was caused by the noise from the circuit's components (e.g., tubes) and amplified during the start-up of oscillation. In this paper we will show that the behavior of a simplified model of the detector is chaotic… It turns out that the detector also has the maximal amplification factor when it operates chaotically.*

[1]Notes appear on page 62.

2. On the third page of the PDF file (which is page 171 of the original article), about half-way down the left-hand column:

From [equation] *(21) it can be noted that for weak incoming signals, i.e., A<<1* [where *A* is the amplitude of the incoming signal]*, the* gain is extremely large.

3. On the sixth page of the PDF file (which is page 174 of the original article), at the bottom of the left-hand column:

From the computer simulations above, we can see that the behavior of the oscillator current is irregular during the first few moments when the total resistance of the circuit is negative. After this small period, the resistance is such that the circuit behaves like an oscillator… The quench mechanism controls *the total resistance and in that way [the quench mechanism also controls]* the chaotically operating mode.

4. On the sixth page of the PDF file (which is page 174 of the original article), near the bottom of the right-hand column:

From the figures it turns out that the start-up conditions are indeed irregular for this type of oscillator. It is exactly this chaotic behavior that in the literature is described as "heavy spots" and [has] *been heard and seen during experiments as* characteristic noise.

References

1. C. Kitchin, "Superregeneration: The Lost Technology," *Communications Quarterly*, Fall 1994, pp 27-40.
2. C. Kitchin, "Regenerative Receivers," *Communications Quarterly*, Fall 1995, pp 7-24.
3 C. Kitchin, "An Ultra Simple Receiver for 6 Meters," *QST*, Dec 1997, pp 39-41.
4 C. Kitchin, "High Performance Regenerative Receiver Design," *QEX*, Nov/Dec 1998, pp 24-36.
5 C. Kitchin, "New Superregenerative Circuits for Amateur VHF and UHF Experimentation," *QEX*, Sep/Oct 2000, pp 18-32.
6 B. Young, "A Mathematical Model for Regenerative RF Amplifiers," *QEX*, Jul/Aug 2001, pp 53-54.
7 B. Young, "A Homebrew Regenerative Superheterodyne Receiver," *QEX*, May/Jun 2002, pp 26-35.
8 B. Young, "A Cascade Regenerative Receiver," *QEX*, Jan/Feb 2004, pp 7-11.
9 D. M. Leenaerts, and W. M. van Bokhoven, "Amplification via Chaos in Regenerative Detectors," *Proceedings of SPIE* [International Society for Optical Engineering], volume 2612 (*Chaotic Circuits for Communication*, SPIE conference of 23-24 October 1995 in Philadelphia, Pennsylvania), pp 136-145.
10 D. M. Leenaerts, "Chaotic Behavior in Superregenerative Detectors," *IEEE Transactions on Circuits and Systems—part 1*, volume 43, pp 169-176 (March 1996).

Gentlemen,

I now have my copies of the Jan/Feb *QEX*. There are some discrepancies between the schematic and the parts list on pp 8 and 9 of the cascade-regenerative-receiver article. C2 and C4 are the ceramic trimmer capacitors, not C2 and C5 as listed. C3 is the floating-rotor tuning capacitor, not a 140 pF variable capacitor as listed.—*Bill Young, WD5HOH, 343 Forest Lake Dr, Seabrook, TX 77586-510;* **blyoung@ hal-pc.org**

A Simple RF Power Calibrator (Jan/Feb 2004)

Doug,

I have often wondered about the usefulness of the technique in Bob's RF calibrator. The specified limits of most CMOS devices are within 0.5 V of Vcc and GND, although it is often considerably better. The average voltage measurement removes the Vcc error, but does not eliminate the GND error. I suspect an oscilloscope (with adequate bandwidth and a carefully calibrated probe) would be a more accurate way to adjust the device, if available. The one used with his spectrum analyzer should be suitable. Its dc accuracy could be verified with a dc source and a DMM. As long as the waveform is square, without rolled corners, the ac accuracy should be close to the dc accuracy.

Bob mentions possible waveform-symmetry concerns and deviation from ideal behavior at higher harmonics. Both can be minimized by using a 20-MHz oscillator driving one-half of a 74AC74 or similar high speed D flip-flop (74FCT, etc) with its D input connected to the Q-not output. The FF will guarantee a 50% waveform, and the high-speed logic will have fast enough rise and fall times to insure good harmonics to several hundred megahertz. —*Wilton Helm, WT6C, 11425 E Caribou Dr, Franktown, CO 80116-8523;* **whelm@compuserve.com**

Hi Doug,

A reader has pointed to some essentially obvious typos in my "A Simple RF Power Calibrator" article in Jan/Feb *QEX*.

Reference p 52, middle column, just above Fig 1, and continuing into the third column, the "0.00995 W" should read "0.00995 mW"; the "10 mW" should be "10 μW"; and the "4.992 mW" should be "4.992 μW". So what's a thousand-times error among friends?!

Because the arithmetic is really okay and because the discussion that follows this general text location is "more of the same" but correct, I don't think this will cause too much reader problem. And to think, I had two knowledgeable friends check the draft....—*Bob Kopski, K3NHI, 25 W End Dr, Lansdale, PA 19446-1927;* **kopskirl@netcarrier.com** □□

Upcoming Conference

The 30th Annual Eastern VHF/UHF Conference

The 30th Annual Eastern VHF/UHF conference will be held on April 16, 17 and 18th, 2004, at the Radisson Hotel in Enfield, Connecticut. The conference has been moved to the spring timeframe to help alleviate numerous conflicts with other ham radio activities and vacation schedules in the August time period. Guest speakers, proceedings articles and overall volunteers are being solicited to help out. Prize donations are also being solicited from vendors and members alike. There is a link is on the NEWS Web site at **newsvhf@qth.net** with further information as it develops. Interested parties can download registration forms and submit them there as well. □□

Next Issue in QEX/Communications Quarterly

In the next issue, Dick Lichtel, KD4JP, has an intriguing piece about implementing USB (universal serial bus) interfaces to your equipment. He is using the Microchip 16C745 PIC microprocessor. That is a relatively new 8-bit device that is certified to support USB 1.1. Some think USB might be a good way to go for those who wish to implement software radios using desktop PCs for most of the heavy number crunching. IF or RF data would be transferred digitally instead of through a sound card. Check it out! □□

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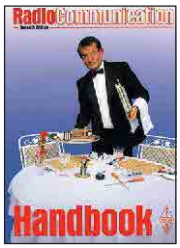

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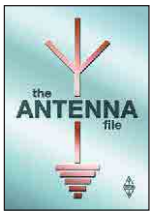

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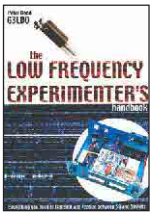

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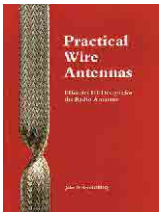

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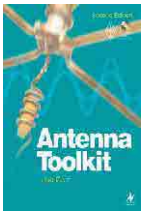

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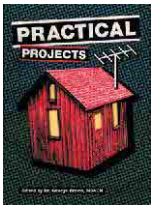

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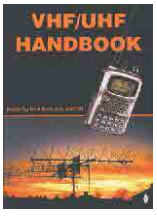

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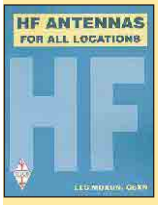

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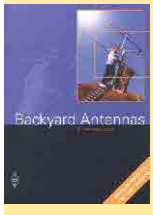

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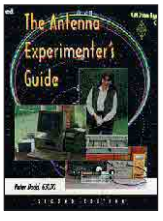

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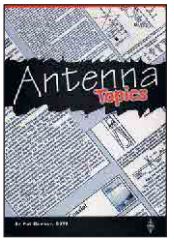

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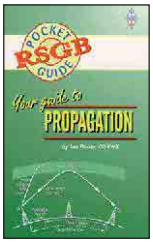

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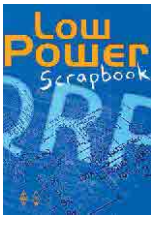

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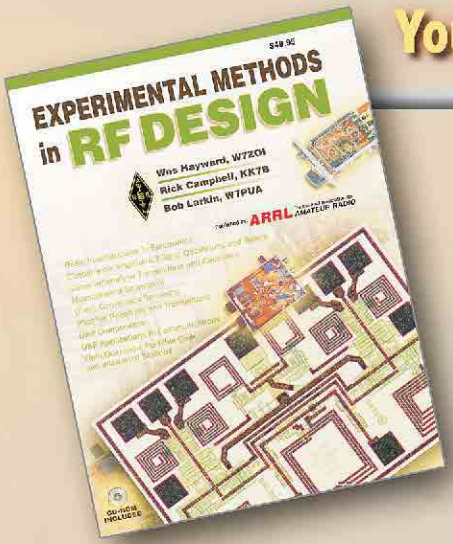

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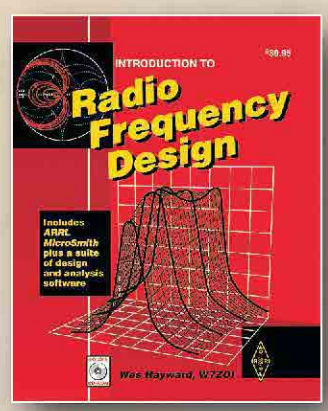

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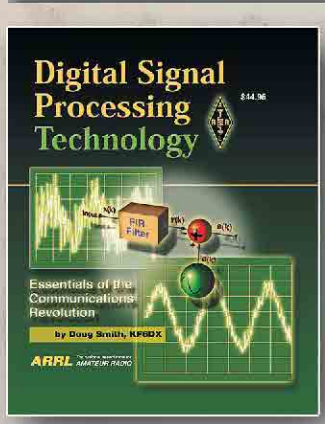

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